High-brightness RGB LED Modules Based on Alumina Substrate

Veli Heikkinen[1], Eveliina Juntunen[1], Kari Kautio[1], Antti Kemppainen[1], Pentti Korhonen[1], Jyrki Ollila[1], and Aila Sitomaniemi[1], Timo Kemppainen[2], Heikki Korkala[2], Terho Kutilainen[2], Hannu Sahavirta[2]

[1]VTT, Kaitoväylä 1, 90570 Oulu, Finland

Phone +358 20 722 2242, Fax +358 20 722 2320, E-mail: veli.heikkinen@vtt.fi

[2]Selmic Oy, Veistämötie 15, 90550 Oulu, Finland

Phone +358 10 820 2907, Fax +358 8 551 1511, E-mail: timo.kemppainen@selmic.com

Abstract

Light emitting diodes (LED) have penetrated into various lighting applications, such as backlighting of keypads and displays in mobile phones, signs, video screens, traffic signals, and exterior and interior lighting for automobiles. A new trend is to use color-tunable light to set or dynamically vary the ambience of the illuminated space. We developed high-brightness RGB LED modules that use bare chips on an alumina (Al_2O_3) substrate. The substrate has dimensions of 14.7 × 25.4 mm^2 and an electrical power consumption of 4.4 W. Thermal simulations were carried out to find the optimum solution among various substrate thicknesses, interface layer materials and geometry of thermal vias in the substrate. Two commercially available plug pastes were experimentally evaluated for making thermal vias. We realized three module series that use a 0.63 mm, 1 mm or 1.27 mm thick substrate. LED chips were die-bonded using electrically-conductive adhesive and wire-bonded with 25-µm Au wire. All chips and bonding wires were protected with UV-curable adhesive. The simulated thermal resistance for the 0.63-mm thick substrate was 6.3 K/W. The optimum solution using one large thermal via and heat distribution layer on top surface of the substrate decreases the resistance down to 2.8 K/W.

Key words: light emitting diodes, alumina, thermal design, thermal vias, module integration

Introduction

Light emitting diodes (LED) have strongly penetrated into mobile phones and other portable devices for backlighting keypads and full-color displays. High-power LEDs are used in signs, video screens, traffic signals, exterior and interior lighting for automobiles, and a variety of niche illumination applications. Solid-state lighting technology is emerging as a cost-competitive and energy-efficient alternative to conventional electrical lighting [1].

There are two approaches for generating white light from solid-state sources, namely phosphor LEDs and multichip LED modules. The phosphor LEDs can be considered as solid-state replacement of fluorescent tubes. The multichip LED lamps offer many advantages, such as chromaticity control, better light quality, and higher efficiency [2].

A new trend is to use color-tunable light to set or dynamically vary the ambience of the illuminated space [3]. One option is to mix the colors of red, green and blue LED chips. We developed prototype series of color-tunable high-brightness RGB LED modules that use bare red, green and blue chips on an alumina (Al_2O_3) substrate. Here one of the key issues was the thermal design of the module. Our overall objective is to realize color-tunable LED modules that can easily be customized to different applications and produced in automated production lines. In this paper we present the details of the thermal design, experiments with the thermal plug pastes, and realized modules together with measurement results.

Module specification

We selected blue and green LEDs manufactured by Cree, USA and red chips made by Epigap, Germany. The blue and green chips had dimensions of 900 × 900 µm^2 and a thickness of 250 µm. The red chips had a size of 1.0 × 1.0 mm^2 with a thickness of 170 µm. The maximum operating current of the chips were 350 mA corresponding to a total power consumption of 4.4 W. The module substrate was specified to be 14.7 × 25.4 mm^2 and it also contained three Zener diodes for ESD protection and a thermistor for temperature measurement.

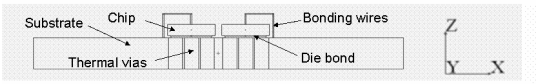
Thermal Design

The thermal conductivity of 96% alumina, k_{Al2O3} is about 25 W/mK. This is much higher than in the epoxy laminate printed circuit boards, such as FR-4, but quite low for high power-density

applications. One method to improve the thermal properties is to make holes to the substrate and fill them with high thermal conductivity material. These structures are called thermal vias. We carried out simulations using Flotherm thermal analysis software to find out the optimum solution among various substrate thicknesses, interface layer materials and geometry of thermal vias.

The thermal model of the LED module used in the simulations shows in Figure 1 and the material values and layer dimensions in Table 1. Blue and green LED chips consisted of the SiC substrate and InGaN active layer. Red chips have Si substrate and AlGaInP epilayers. The heat generated in the chip was assumed to be distributed uniformly in the active layer.

The chip was assumed to be die-bonded either by solder or electrically-conductive adhesive. The outside atmosphere was stagnant air at 25 °C. Flotherm software cannot model cylindrical layers. Therefore, the bonding wire and thermal vias were replaced with hypothetical structures that have square cross-section with equivalent volume.



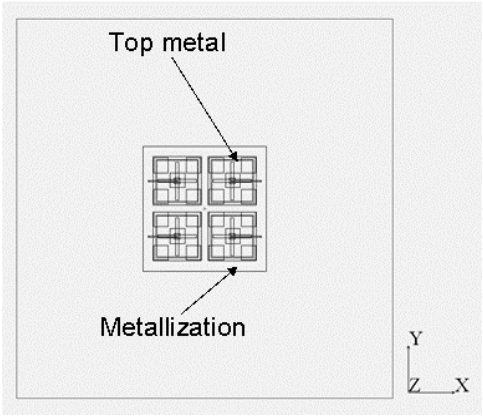


Figure 1: Thermal Model of LED Module.

The interface layers are essential for the thermal resistance of the structure. Thermal simulations were utilized to study the effect of interface material selection. The test structure used in the simulations was otherwise similar as in Figure 1, but the module was assumed to be attached on an ideal heat sink with a thermal resistance of 4 K/W. Here the assumed dissipated power was 5.44 W. The interface layers of the simulated structure are illustrated in Figure 2.

Table 1: Materials Used in Thermal Simulations.

Layer	Material	Size (x, y, z) (mm)	k (W/mK)
LED chip	SiC InGaN	$0.9 \times 0.9 \times 0.23$ $0.79 \times 0.79 \times 0.02$	270 100
	Si AlGaInP	$1.0 \times 1.0 \times 0.17$ $1.0 \times 1.0 \times 0.02$	118 100
Top metal	Au	$0.06 \times 0.7 \times 0.001$	296
Bonding wire	Au	0.022×0.022	296
Die bond	solder adhesive	$0.76 \times 0.76 \times 0.02$	57 3
Metallization	Ag/Pt1%	$2.3 \times 2.3 \times 0.008$	322
Substrate	alumina	$7 \times 7 \times 0.63$	25
Thermal vias	Ag/Pt1%	$\varnothing\ 0.3 \times 0.63$	322

The interface layer between the LED chip and alumina substrate (1. interface layer in Figure 2) was either AuSn solder or electrically conductive adhesive. The second interface between alumina substrate and heat sink was electrically isolating because the LEDs had to be isolated from each other and the heat sink. The isolation could be realized either with electrically non-conductive adhesive (k = 3.6 W/mK) or glass layer (k = 1.05 W/mK). If the glass layer is used, adhesive is needed to attach the substrate on the heat sink.

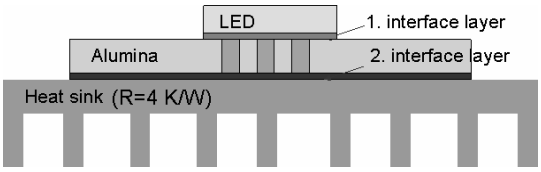


Figure 2: Interface Layers of Simulated Structure.

The simulation results are shown in Table 2. If the material on the chip-alumina interface is AuSn solder the thermal resistance, R_T, from the active junction to the bottom of the LED module is 2.8 K/W less than it would be if the interface material was conductive adhesive. The thermal resistance further increases 1.6 K/W if the electrical isolation is made with glass instead of non-conductive adhesive.

Table 2: Thermal Simulation Results with Different Interface Materials.

Interface layer 1		Interface layer 2		R_T (K/W)
Material	z (µm)	Material	z (µm)	
AuSn	20	Non-cond. adhesive	50	3.5
AuSn	20	Glass + adhesive	54	5.1
Conductive adhesive	20	Non-cond. adhesive	50	6.3
Conductive adhesive	20	Glass + adhesive	54	7.9

Thermal simulations were also used to study the effect of thermal vias and heat distribution layers. The test structure used in the simulations is illustrated in Figure 1. AuSn solder was used on the LED-alumina interface and non-conductive adhesive on the alumina-heat sink interface. The bottom of the structure was fixed on temperature 25 ºC assuming that the structure sits on an ideal heat sink. The assumed dissipated power was 5.44 W. Figure 3 shows the variations made in this simulation series and Table 3 lists the main results.

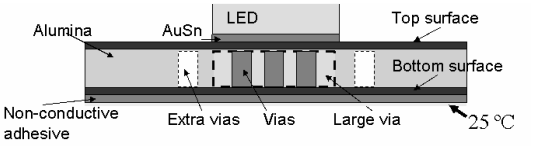


Figure 3: Simulated Structure with Variations of Thermal Vias and Heat Distribution Layers.

The simulations showed that thermal vias were the most effective heat management method for this module. Thermal vias with different locations and sizes were simulated. The simulations demonstrated that the vias were useful right under the heat source. Some extra vias were added around the LED chips, but their effect was minimal. Also the effect of one large via (Ø = 0.763 mm) in comparison with 5 smaller ones (Ø = 0.3 mm) was simulated. The thermal resistance decreased ~ 2% with the large via.

Another heat management option was the addition of heat distribution layers made with silver paste (k = 200 W/mK) on alumina substrate. For these layers two different thicknesses (22 µm and 55 µm) and three different sizes (large: 7×7 mm^2, mid-size: 3.5×3.5 mm^2, and small: 2.1×2.1mm^2) were simulated. The layer can locate either on the top surface, on the bottom surface or on both surfaces. The simulations showed that if there were thermal vias the effect of the heat distribution layer was quite small. However, if the vias were not an option, the heat distribution layer enhanced the thermal management of the structure significantly.

The heat distribution layer was useful only on the top surface. The benefit of the bottom layer was close to zero, or even negative if the layer was too thin. The thermal resistance of the module with heat distribution layer on both surfaces of the substrate was the lowest, but very close to the result of one layer on the top surface. Thus, there is no use of wasting the silver paste on both sides of the alumina. Another conclusion based on the simulations is that it is beneficial to use as thick a layer as possible. The size of the layer is not as significant and increasing the size of the heat distribution layer reduces the thermal resistance only up to a certain limit. Therefore, Table 3 lists the results only for the thicker mid-size (3.5×3.5 mm^2) heat distribution layer on top surface of the alumina substrate.

Table 3: Simulation Results with Different Heat Management Methods.

Vias (mm)	Heat distribution layer	R_T (K/W)	Change (%)
-	-	5.95	0
-	55 µm, mid-size, top surface	4.51	- 24
5 × Ø = 0.3	-	3.25	- 45
5 × Ø = 0.3	55 µm, mid-size, top surface	2.95	- 50
1 × Ø = 0.76	55 µm, mid-size, top surface	2.83	- 52

Final simulations were made with structure consistent with the actual prototype LED module. Now the alumina substrate size was 25.4×14.7 mm^2 and three different thicknesses, 0.63 mm, 1 mm, and 1.27 mm were tested. Heat distribution layer made with silver paste (k = 200 W/mK) was applied on top surface of the substrate. The layer thickness was 200 µm and total area under the LEDs 78 mm^2. There were four LED chips on the substrate, namely one blue, two green and one red. The power consumption used in the simulations was 4.96 W. The interface between LEDs and heat distribution layer was electrically-conductive adhesive (thickness of 20 µm), because the chips could not be soldered on the silver. The substrate-heat sink interface was non-conductive adhesive (thickness of 50 µm). The bottom of this adhesive layer was fixed to a temperature of 25 ºC assuming that the structure sits on an ideal heat sink.

The simulated thermal resistance of the structure with 0.63 mm thick substrate was 6.3 K/W. The resistances with 1 mm and 1.27 mm thick substrates were 6.7 K/W and 6.8 K/W, respectively. The surface temperatures of structure with 1-mm thick alumina substrate are illustrated in Figure 4. Figure shows that heat conducts poorly along the substrate even with the thick heat distribution layer. The red LED is cooler than the other ones due to its smaller forward voltage and heat dissipation.

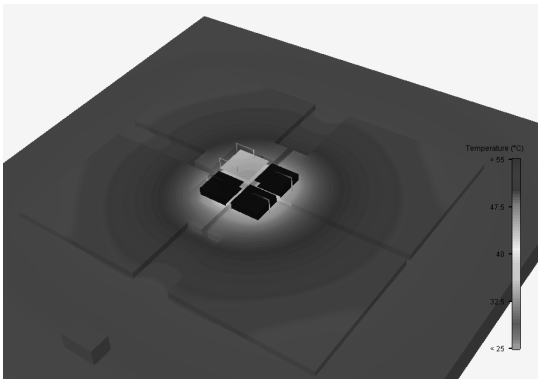


Figure 4: Simulated Surface Temperatures of Prototype Module with 1-mm Thick Substrate.

Thermal Via Experiments

Silver based thermal plug pastes are fairly high viscosity pastes that are used to fill lasered through holes on alumina substrates by stencil printing. Due to small amount of solvent, the deposited paste does not sag too much upon drying. Most importantly, the firing shrinkage of plug paste is very small, enabling crack-free thermal vias. Two commercially available plug pastes were evaluated to make thermal vias for high power LED chips.

Alumina substrates ($4'' \times 4''$) with lasered through hole structures were used in the tests. The diameter of holes varied between 0.25 mm and 0.9 mm. Substrate thickness was either 0.5 mm or 0.63 mm. A 50-µm thick punched stainless steel stencil was used. The printer table was equipped with a porous metal nest to supply a uniform through-hole vacuum. A sheet of paper was used between the nest and the substrate. The stencil apertures corresponded to the lasered substrate holes. The actual filling of the holes was made in double print mode with fairly slow squeeze speed and the stencil in contact with the substrate. The drying of the paste was made at 80 °C with the backing paper on a metal tray. After drying, the backing was removed and the substrate was sintered in a belt furnace using the standard 850 °C thick film profile. Figures 5 and 6 show examples of the filled and dried through-hole structures.

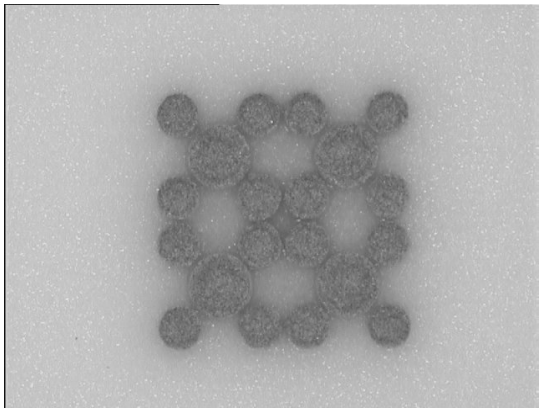


Figure 5: Thermal Via Structure for 2×2 LED Array on 0.5-mm Thick Alumina Substrate. Via diameters are 0.4 mm and 0.25 mm.

The biggest challenge with the processing of thermal plug pastes was how to fill the hole completely with a flat surface, to enable LED chip assembly. Naturally, the metallization is very flat on the bottom side of the substrate, because the paste stops to the backing paper. However, the paste adheres to the backing and when the backing is removed after drying, small cavities can be seen on the via plugs. On the top side or stencil side of the substrate, small holes up to a diameter of 0.4 mm can be filled totally in one print cycle. Larger holes, up to a diameter of 0.9 mm probably require two print-dry cycles to obtain a smooth via surface.

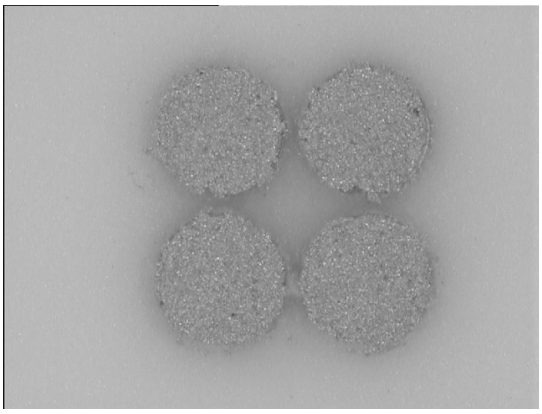


Figure 6: Thermal Via Structure for 2×2 LED Array on 0.63 mm Thick Alumina Substrate. Via Diameter is 0.9 mm.

The shrinkage of via plug paste is very small during sintering and there was no sign of via plug separation from the wall of the lasered hole, as can be seen in Figure 7.

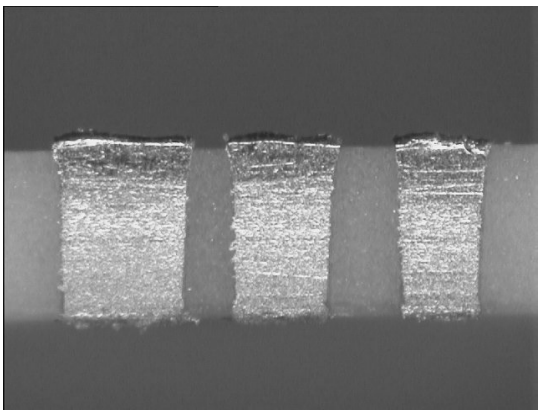


Figure 7: Sintered and Diced Via Plugs with Diameter of 0.4 mm, 0.3 mm and 0.25 mm. Substrate thickness is 0.5 mm.

Module Realization

We realized three module series that use a 0.63 mm, 1 mm or 1.27 mm thick alumina substrate. Due to production technology reasons we did not use thermal vias. A 200-µm thick Ag paste layer with an area of 4×4 mm^2 was printed to the substrate under each LED chip. The chips were die-bonded using electrically-conductive adhesive and wire-bonded with 25-µm Au wire. A thermistor was placed on the substrate for temperature monitoring. All chips and bonding wires were protected with UV-curable adhesive. One prototype module shows in Figure 8.

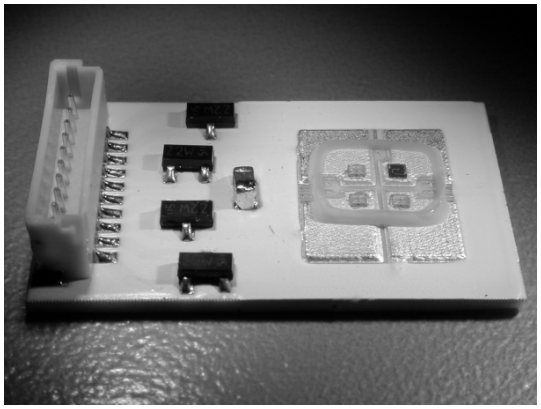


Figure 8: Prototype LED Module.

Module Measurements

The operational characteristics of the LED modules were measured using the setup shown in Figure 9. The module under test was placed on top of the thermoelectric cooler that was set to a temperature of 25 °C. The drive current of each LED was set to 350 mA. The optical power emitted from the LEDs was monitored using an optical fiber that was coupled to an optical power meter (Ando AQ-1135E with AQ-1972 detector). The forward voltage of the chips was also measured.

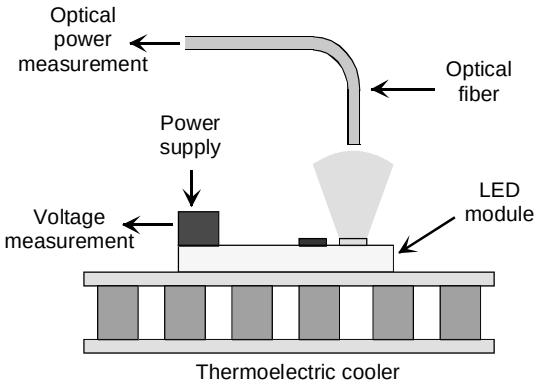


Figure 9: Measurement Setup for LED Modules.

The optical power of a blue LED as a function of time shows in Figure 10. In a warm-up time of one hour the power decreased 11% from its initial value. At the same time the forward voltage LED decreased 17 mV, Figure 11. According to manufacturer's data this corresponds to a temperature increase of 5.7 °C. This is equivalent to a thermal resistance of 4.8 K/W.

The module series will be subjected to reliability stress testing. This will include high temperature operating life (+85 °C, 1000 h), wet high temperature operating life (+70 °C/85%RH, 1000 h) and non-operating temperature cycle (–40 … +85 °C, 400 cycles) tests.

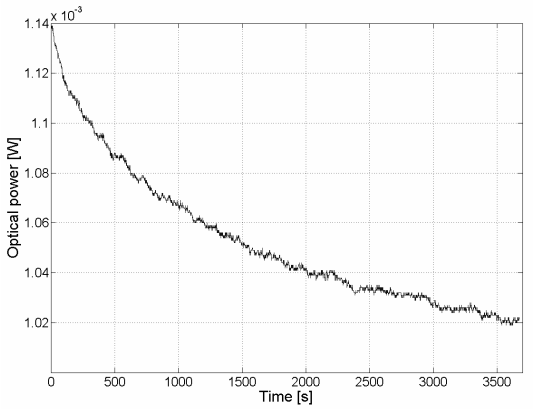


Figure 10: Optical Power of Blue LED on 1 mm Thick Alumina Substrate.

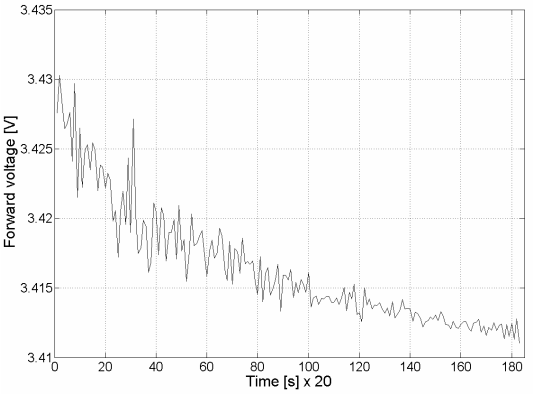


Figure 11: Forward Voltage of Blue LED on 1 mm Thick Alumina Substrate.

Conclusions

We realized three series of high-power RGB LED modules using bare chips. The modules used a 0.63 mm, 1 mm or 1.27 mm thick alumina substrate. A 200-µm thick Ag paste layer with an area of 4×4 mm^2 was printed to the substrate under each LED chip. The chips were die-bonded using electrically-conductive adhesive and wire-bonded with 25-µm Au wire. All chips and bonding wires were protected with UV-curable adhesive.

The simulated thermal resistance of the module with 0.63 mm thick substrate was 6.3 K/W. The resistances with 1 mm and 1.27 mm thick substrates were 6.7 K/W and 6.8 K/W, respectively. According to simulations, one large thermal via and heat distribution layer on top surface of the 0.63-mm thick substrate decreases the thermal resistance down to 2.8 K/W.

Two commercially available plug pastes were evaluated to make thermal vias for high power LED chips. The diameter of holes varied between 0.25 mm and 0.9 mm, and substrate thickness was either 0.5 mm or 0.63 mm. The biggest challenge with the processing of thermal plug pastes was how

to fill the hole completely with a flat surface, to enable LED chip assembly.

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