

A 3-D packaging concept for cost effective packaging of MEMS and ASIC on wafer level

Tobias Baumgartner*, Michael Töpfer*, Matthias Klein*, Bernhard Schmid**, Dieter Knödler**, Heikki Kuisma***, Sami Nurmi***, Hannu Kattelus+, James Dekker+ and Ralph Schachler++

*Fraunhofer IZM, Gustav-Meyer-Allee 25, 13355 Berlin, Germany Phone: +49-30-46403-602, Fax: +49-30-46403-123 and e-mail:tobias.baumgartner@izm.fraunhofer.de;

**Continental Teves AG & Co. oHG, Guerickestraße 7, 60488 Frankfurt/Main, Germany,

***VTI Technologies Oy, Myllynkivenkuja 6, Vantaa 01621, Finland,

+VTT Tietotie 3, Espoo 02044, Finland,

++AemTec GmbH Carl-Scheele-Str. 16, 12489 Berlin, Germany

Abstract

Heterogeneous integration bridges the gap between nanoelectronics and its derived applications. Currently MEMS and their signal conditioning ASICs are produced and packaged at different industry sectors (different fabs). To reduce costs and enhance yield and performance at the same time this quite expensive way of packaging has to be modified. This paper presents a different packaging concept. It uses standard redistribution layer technology (RDL) to package thinned chips on a full wafer substrate e.g. thinned ASIC chips on a MEMS wafer. For this approach no Through Silicon Vias (TSV) are needed. Standard chips can be used without redesign. Only Known Good Dies (KGDs) are packaged with the cost benefit of wafer level technology.

At the starting point for this type of packaging both ASIC and MEMS chips are still parts of full wafers. The wafer with the larger sized chips (e.g. MEMS chips) is used as a substrate for the further process steps. The wafer with the smaller sized chips (e.g. ASIC chips) is thinned down on wafer level to a thickness of 10µm to 40µm and diced. These thinned chips are glued onto the base wafer with a polymer layer (BCB from Dow Chemical). The polymer has been deposited and structured before gluing the next chip on top. After placement of the thinned chips the wafer is again coated with BCB to embed the chips. This polymer layer is photostructured to open contact pads on the base chips as well as on the embedded chips. The next step is the built-up of metal routing. Here a semi-additive process is used, which means electroplating on a sputter seed layer of TiW/Cu. This metal layer is followed by another polymer layer for passivation and acting as a solder mask. Then Under Bump Metallization (UBM) is applied again by electroplating. Finally Balling is done either by Ball Placement or by Solder Paste Printing. Now the wafer is diced and the full ASIC-MEMS package can be flip chiped onto a Printed Circuit Board (PCB). The technology will be demonstrated by the project RESTLES (Reliable System Level Integration of Stacked Chips on MEMS).

RESTLES will integrate technologies like silicon MEMS, ASIC, wafer thinning, chip stacking and flip chip to one packaged chip stack at die scale. The influence of the heterogeneous stack on performance and control mechanisms to eliminate parasitic effects will be investigated.

Key words: thin chip, embedding, wafer level, MEMS packaging,

Introduction

In IC production “Moore’s Law” is a well-known proclamation that predicts the miniaturization from one generation of ICs to the next one. For MEMS a similar “Moore’s MEMS law” does not exist, but there is still a tendency to shrink device

size for cost reduction and the access to new applications. . Due to the heterogeneous technologies and requirements like standard CMOS chips and silicon micromachined sensors the packaging thereof is often a limiting factor. To overcome this problem the integration on silicon level was considered very intensively, but hasn’t

become the mainstream. Mainly yield degradation, silicon area consumption and performance treats keeps the chips individual.

Therefore, making MEMS devices smaller is not only a matter of the silicon technology itself. The sizes of the chips (signal conditioning ASIC and MEMS element), the connection technology between ASIC and MEMS as well as the packaging are important for the size of the whole device.

The technology of Thin Chip Integration (TCI) [1] that was developed at Fraunhofer IZM enables to integrate MEMS and ASIC at chip scale by stacking and connect them with each other by the use of standard redistribution layer (RDL) technology on wafer level. There are further benefits given by the use of TCI such as well-defined and short routing appropriate for high frequency applications as well as cost reduction. The process flow of TCI is explained in the next chapter.

The process flow of TCI

TCI is used to stack at least two chips and connect them with each other without TSV. Both types of chips are fully processed with all frontend processes. The process flow of TCI is schematically shown in figure1. The chips of the base wafer stay at wafer level until the end of the TCI process. In order to stack the thin chips on the base wafer they have to be smaller than the base chip. Before stacking the chips are thinned down on wafer level to a final thickness of 10-40µm. and are singulated during thinning before further processing

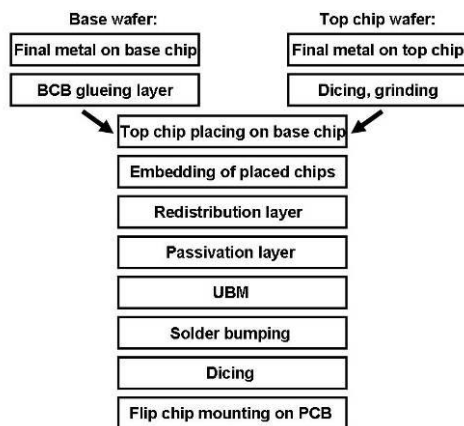


Figure 1: Process flow for TCI technology

The TCI process starts with the spin coating of a Photo-BCB layer (Benzocyclobutene - Cyclotene 4000 series from Dow Chemical Company) on the base wafer and photostructuring. This layer has two purposes: First it functions as the passivation of the final metal of the base wafer chips and secondly it works as the “glue” for the thinned top chips. After probing of top chip- and base wafer known good top dies are placed face up on top of known good base dies by a flip chip bonder. The next step is the embedding of the stack with another layer of Photo-BCB. This layer is opened at the pads

of the base chip as well as at the pads of the embedded thinned chip. In the next step a copper rerouting is built up to connect the pads in the desired routing and to form the I/O contact pads of the final device. The RDL is passivated with a 3rd layer of Photo-BCB and the I/O contact pads are opened by photolithography. Then a Ni/Au-UBM is deposited, patterned and solder balls are placed or screen printed on top of the UBM. After reflow of the solder the wafer is diced. Now the device is ready for flip chip mounting on a PCB or other substrate.

Technology demonstrator

The technology was evaluated by a demonstrator that was built up as part of the European project RESTLES (Reliable System Level Integration of Stacked Chips on MEMS). Here a MEMS wafer is used as the base wafer. Within this project the TCI technology is named SCOM (Stacked Chip on MEMS). The process flow for the RESTLES project is shown in figure2.

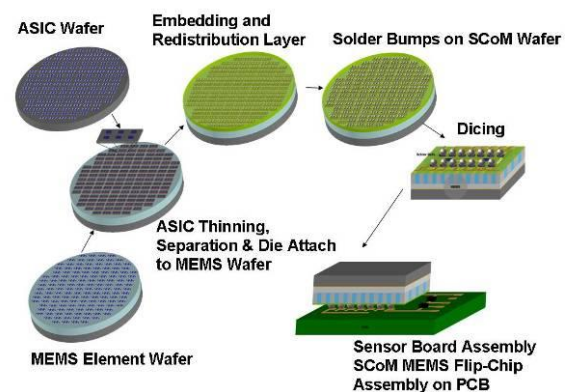


Figure 2: Process for RESTLES project

For the prototype device the base wafers contain inertial sensors and are made by project partner VTI. VTI’s 3D MEMS technology consist of a triple wafer stack with a cap wafer which has high doped through wafer Si contacts embedded in glass [2]. The contacts have Al pads on top and are separated by glass.

For the technology demonstrator wafers without sensor function were used as base wafers. They do have the same thickness and mechanical geometry as the final functional MEMS wafers and the same surface metallization. Non-functional dummy ASIC chips with Al structures were used as top chips. Those were thinned down to 30µm thickness. Figure3 shows a part of a base chip seen in an optical microscope.

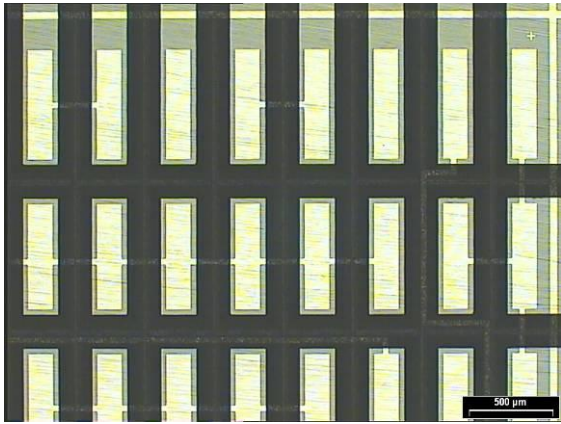


Figure 3: Base chip seen in an optical microscope before TCI process

A structured BCB layer is used to glue the top chip onto the base chip (Figure4).

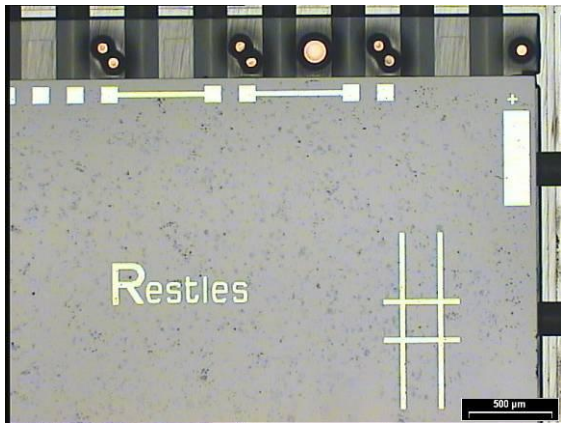


Figure 4: Thinned top chip after mounting on the base chip (optical microscope)

The top chip is embedded in another BCB layer. Subsequently the RDL layer is deposited. The RDL process is an additive process that uses a TiW/Cu seed layer, photoresist coating and structuring and electroplating in opened areas. Finally the photoresist is stripped and the seed layer etched. Figure5 shows the chip after RDL.

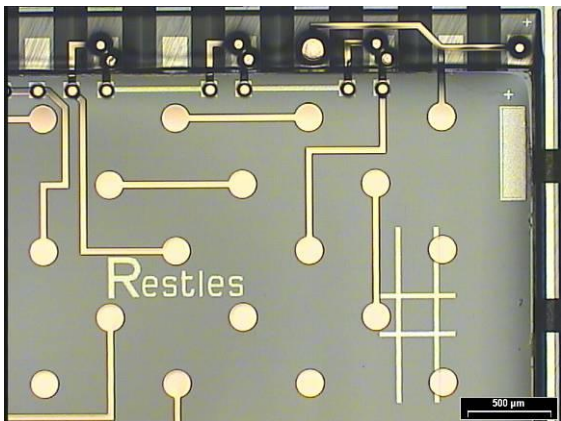


Figure 5: Thinned top chip on base chip after embedding and RDL seen in an optical microscope

Now the final BCB-passivation is coated and the I/O-pads are opened. The final step is the deposition of the Ni/Au-UBM, again by electroplating. (Figure6).

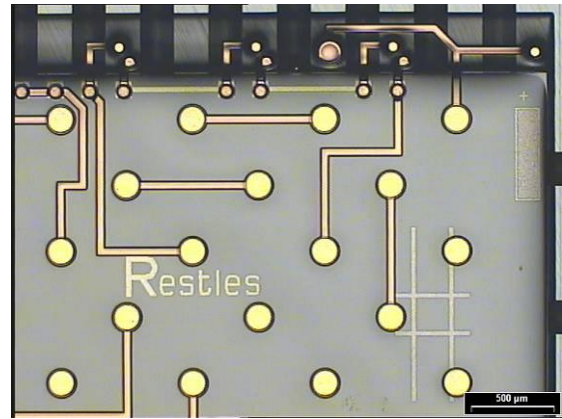


Figure 6: Thinned top chip on base chip after final passivation and Ni/Au-UBM (optical microscope)

At the project partner AEMtec Pb-free solder bumps were deposited by screen printing and fixed by a reflowed process. Figure7 shows the processed wafer after reflow of the solder bumps. A detailed picture is shown in figure8.

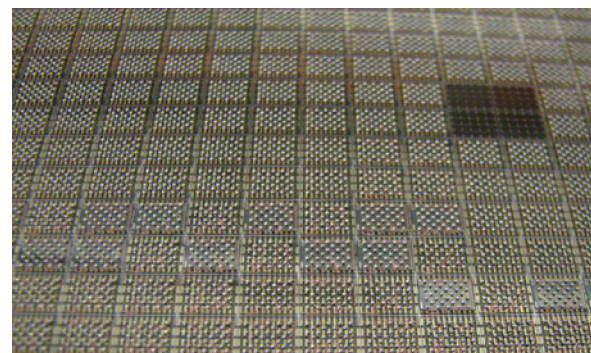


Figure 7: RESTLES wafer with embedded thinned chips after full TCI process before dicing

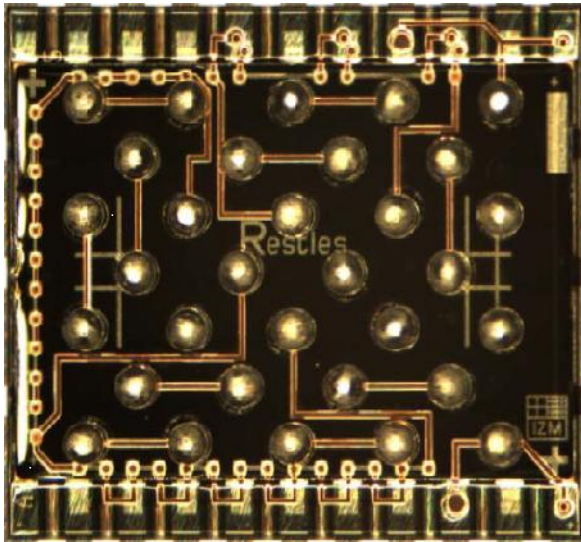


Figure 8: RESTLES SCoM-chip with embedded thinned chip after full TCI process

Then the SCoM-wafers were diced at VTI. After that the singulated devices were flip-chip mounted on PCB at AEMtec. (Figure 9 shows the mounted chip on PCB with underfill).

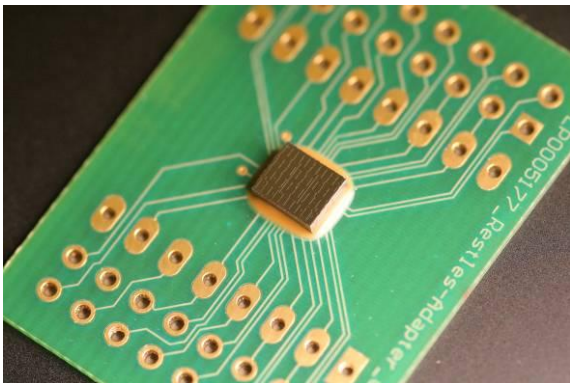


Figure 9: RESTLES SCoM-device after full TCI process mounted on PCB

A cross section of the PCB-mounted chip is shown in Figure 10.

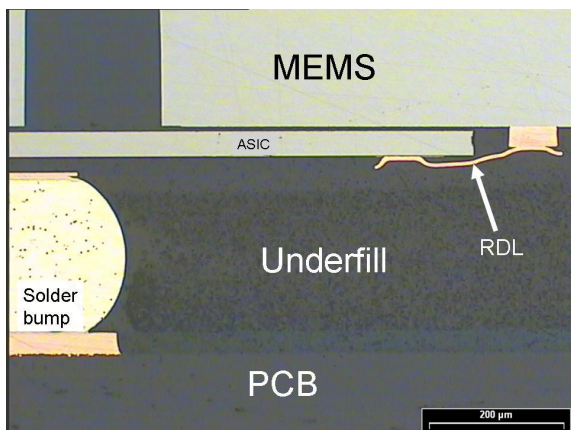


Figure 10: Cross section of a RESTLES SCoM-device stack mounted on PCB after full TCI process

Resistance Measurement Results

First daisy chain (DC) resistance measurements reveal very low parasitic resistance. The currently analysed DC's are shown in Figure 11 (DC 1 blue, DC 2 red, DC 3 green and DC 4 yellow).

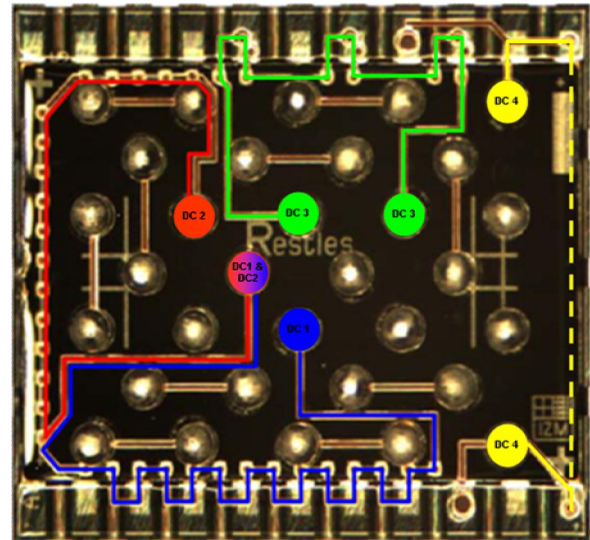


Figure 11: RESTLES SCoM-chip with daisy chain indication: DC 1 blue, DC 2 red, DC 3 green and DC 4 yellow (the dotted line is a metal runner on the MEMS layer)

DC 1 and DC 2 have only vias down to the top chip, but DC 1 has the RDL going over the top chip edge. The mean resistances of DC 1 is 2,12 Ohms and of DC 2 is 2,01 Ohms. The standard deviation of the measured 14 parts were 0,06 Ohms. Two of DC-2 have shown no connectivity. DC 3 has vias going down to MEMS and top chip pads. They have 1,95 Ohms (sigma 0,08 Ohms and 9 of 14 failing parts). DC 4 has only vias going down to MEMS pads. They have 2,00 Ohms (sigma 0,16 Ohms and 9 of 14 failing parts). The root cause of the failures is found in the embedding material when the top chip edge is too close to the dicing line of the SCoM device. Currently improvement of the embedding process is in progress to avoid these failures. In parallel these SCoM test devices are going into life time tests for reliability investigations.

Summary

A SCoM technology demonstrator that uses the same materials and surfaces as the final device was successfully built up. Via chain structures were successfully measured and show resistance of few Ohms. Currently the reliability of the demonstrators is under test. After passing these tests and further

improvements the next step is to build up functional devices. This is going to take place until end of 2009.

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References

- [1] M. Töpfer, K. Scherpinski, H.-P. Spörle, C. Landesberger, O. Ehrmann, H. Reichl, "Thin Chip Integration (TCI-Modules) – A Novel Technique for Manufacturing Three Dimensional IC-Packages", Proceedings IMAPS 2000, Boston, USA, September 2000
- [2] Heikki Kuisma, "Wafer level packaging of MEMS", Keynote at SMART SYSTEMS INTEGRATION conference, Barcelona, Spain, 9 –10 April 2008