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Micro-electro-mechanical radio-frequency switch fixed electrode by wet etching of AlSi-based multilayer

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Abstract

We studied the possibility and implications of using a magnetron-sputtered aluminum-silicon (Al-1%Si) film in developing the fixed electrode for a micro-electro-mechanical radio-frequency switch structure. We describe the electrode qualitative specifications which originate from the performance of an application and from processing, including process-flow integration. Most of our set of limitations and needs to fulfill is general, such that, the solutions and considerations we present for meeting them are of general applicability. The outline of the task was to produce an electrode that retains a smooth surface over subsequent process flow. High conductivity at dc as well as low losses up to GHz-range frequencies was required. The process integration suggested also considering step-coverage issues of later film-deposition steps and electrical contacting to other conductor layers.

We studied Mo and Mo/AlSi cap layers for controlling the surface morphology, pattern-edge slope and, the electrical contacts. Implications of the Freckle etching associated with AlSi wet etching are reflected to film characteristics and process-integration choices. We report quantitative data of the etch rates, pattern-edge slopes, pattern edge-line quality and, the surface topography in terms of hillock growth and pit formation. Electrical contacting to below and above layers is also quantified. Furthermore, we present etching behavior not commonly found in literature.

Keywords: RF-MEMS, aluminum-silicon, molybdenum, capping, Freckle, taper, hillock, pit

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Introduction

1.1. Alloys and capping of aluminum electrodes

Films of aluminum and its alloys are widely studied and applied in electronics and in micro-electro-mechanical systems (MEMS). Aluminum features high dc conductivity and low losses at GHz frequencies. Especially the development of liquid-crystal displays (LCD) and thin-film transistor (TFT) displays has promoted research on alloyed Al films with capping layers for surface quality and pattern-edge taper [1, 2, 3]. Both the composition and the capping are tools for suppressing hillock and pit formation under stress and thermal loading. The cap layers combined with wet patterning also provide means of generating a shallow pattern-edge taper for better step coverage of later deposited films. Capping synergy with improvement of contacts and surface-smoothness has drawn the attention from earlier studies based on plasma-etch tapering [4, 5, 6].
The behavior of aluminum-based thin films under stress and under heat loading has induced several experimental studies [7 – 10] and theoretical modeling [11 – 14] of grain-boundary evolution which results in hillocks and pits. In this text, “hillock” and “pit” refer to a film-grain deformation or dislocation along grain boundaries as illustrated later in chapter 3.2. Reports on experiments that yielded also through-film voids may refer to our pits as “grain-collapse” [9]. The definition hillock has also been assigned to deformations of different origin in small-grain Al films [15].
AlSi film is a common option where reliable contacting onto silicon surface is called for. The small proportion of alloyed Si in the film saturates Si solubility in Al so preventing metal penetration into, and consumption of, the Si substrate. AlSi surface morphology [8, 10] and electrical properties [16, 17], including electromigration [18], have been compared with related alloys and with pure Al, as reviewed in [19]. Studies on capped [17] or other multilayers [20] of AlSi are rare. Reports on Al-alloy films with Mo cap layer for controlling the surface morphology or with any capping for etch taper in wet etching have not concentrated in AlSi. Freckle etching, necessary for amorphous Si remnants removal, induces a complication which may hinder interest in AlSi wet etching.

1.2. RF-MEMS switch application requirements

The targeted application is the fixed electrode in a radio-frequency (RF) MEMS switch. The application has since been demonstrated and will be reported elsewhere. The switch features an upper released electrode separated by an air gap from the lower fixed electrode (Fig. 1). After a capacitive actuation closes the gap, the dielectric layer coating the fixed electrode keeps the contact capacitive, i.e., insulated in dc sense. Below the fixed electrode, an additional thin-film resistor (TFR) will be patterned for dc biasing.

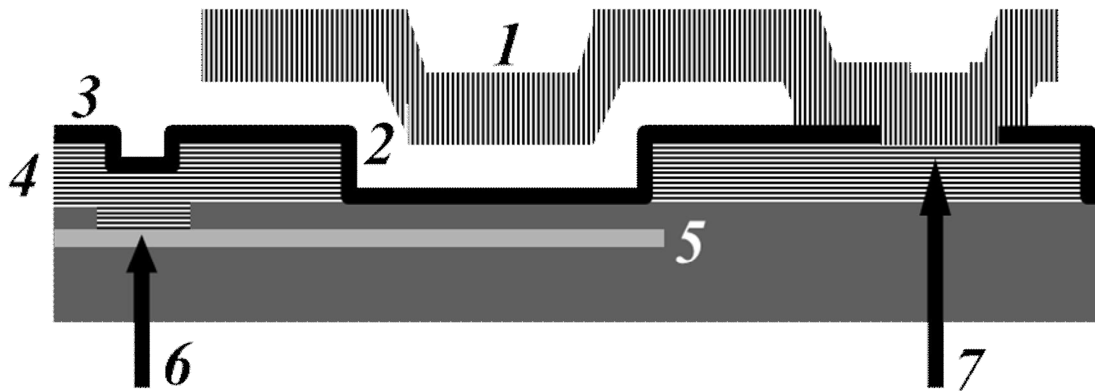

Fig. 1. Schematic illustration of the main features of the RF-MEMS switch. (1) Released actuable upper electrode, (2) Air gap, (3) Dielectric layer of the capacitive switch, (4) Fixed electrode developed in this study, (5) TFR between insulator layers. Note the electrical contacts: (6) between fixed electrode and TFR, (7) between released-electrode anchoring and fixed electrode.

The process must be compatible with the complementary metal–oxide–semiconductor (CMOS) process in two senses. First, the fabrication process of the RF circuitry must allow for monolithic integration onto a CMOS wafer. On the other hand, a requirement to exclude materials that contaminate CMOS-processing equipment is of practical importance where single facility is shared between MEMS and CMOS fabrication. Together these boundary conditions limit the maximum process-step temperatures near 400 ^{o}C and rule out common metals like Au, Cu, Pt and their alloys including AlCu and AlCuSi. Among metals that feature low losses at GHz regime and few micro-Ohm-cm resistivity at dc, we are left with Al and the alloy AlSi.

While selecting AlSi for our electrode material, we must address the Al-based films tendency to deform when exposed to temperature loads. Hillocks may ultimately support the down-pulled switch apart from dielectric-layer surface thus reducing the down-state capacitance. Our study aimed at keeping the electrode surface as smooth as possible. Pits and hillocks were here treated as equal defects to be avoided. Other applications and process flows may suffer differently from the two. If the sacrificial layer for the RF-MEMS switch air gap (Fig. 1 (2)) were more planarizing, the process would better tolerate occasional pits but would be sensitive for hillocks. We used non-planarizing chemical-vapor-deposited (CVD) SiO_2 since polymer sacrificial layers would have been too unstable for being left as final component mechanical members.
The electrode pattern-edge profile must not be a vertical wall as left after typical plasma-etching processes. The released-electrode mechanical durability at fixed-electrode edge step does not allow for bad step coverage. For sacrificial layers, we used plasma-enhanced-CVD (PECVD) SiO_2 with poor step-coverage profile. Better behaving low-pressure-CVD SiO_2 was excluded due temperature limitation during process steps after the AlSi electrode. Accordingly, we targeted at generating a shallow slope for the pattern edge.

The electrode edge line must be as straight as possible and free from unidealities like mouse bites. Wet etching adds uncertainty in the final line width, thus suggesting extra tolerance for the minimum line width in design rules. However, smooth edge line remains essential for well-defined width of long narrow conductors.
One more issue is the electrical contacting. Aluminum does not reduce native oxides on conductor surfaces. In addition, it generates a durable native oxide on its own surface. We needed ohmic contacts where indicated (6) and (7) in Fig. 1. However, high-quality contacts of a single-ohm or below dc resistance were not required. This was because the circuits operate at high frequencies and the TFR itself features some 1 kOhm sheet resistance anyway.

2. Experiment

2.1. Test Material and Sample Types

Test wafers were prepared and patterned with a bare TiW/AlSi electrode (Fig. 2a) and with two options of capped TiW/AlSi. Cap layer was 50-nm Mo (Fig. 2b) or 50-nm Mo + 50-nm AlSi (Fig. 2c). The initial motivation to incorporate the double-layer cap was in TiW-layer plasma etching as explained in section 3.1.3. The Mo/AlSi-capped electrodes were also prepared without the underlying TiW layer (Fig. 2d). Some wafers featured an oxide-insulated MoSiN TFR beneath the electrode (Fig. 2d,e). The TFR was for studying the effect of the TiW layer on the electrical contacting downwards (see section 3.3.). Most wafers (Fig. 2a-e) were further processed so that another oxide-insulated AlSi was patterned on top. The 1500-nm layer was for studying the cap-layers effect on the contact resistances upwards as well as for simulating the full process flow of the MEMS switch in Fig.2. A set of simpler single-layer wafers (Fig. 2f-h) were prepared for further checking the Mo, AlSi, and Si-substrate etching behavior and for gaining the etch-rate data presented in section 3.1.1.

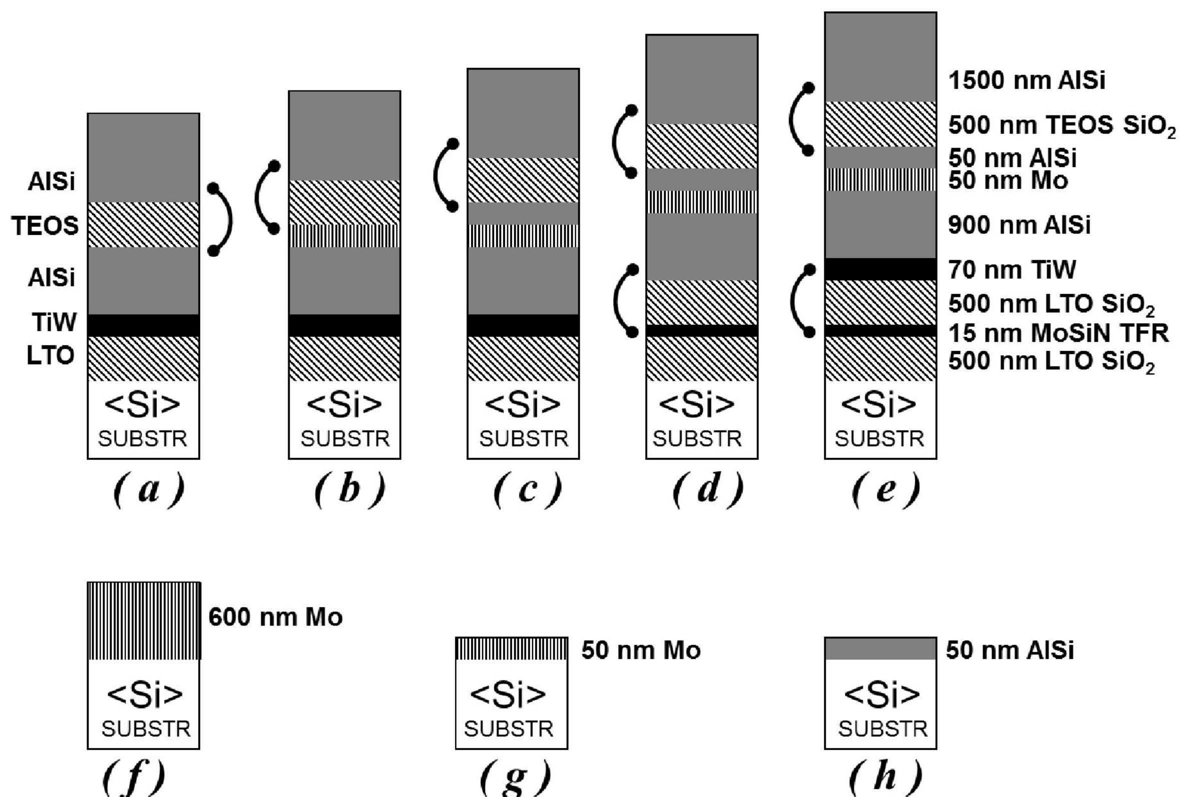

Fig. 2. Illustration of the experiment test material. The via structures through SiO_2 insulators are not illustrated in layer images but indicated by the connector arcs.

2.2. Sample Preparation

Each lithography was done with SPR700 photo resist (PR) (Rohm and Haas Electronic Materials) except for the electrode wet etching, where AZ 5214E (MicroChemicals GmBH) was used. Baking temperatures were 110 °C and 120 °C for SPR700 and AZ 5214E, respectively. Priming-oven temperature was 150 °C for both.
The TFR layer was dry etched in Cl_2/CF_4 plasma and the vias for electrode contacts wet etched in buffered hydro-fluoric acid (BHF). The TiW layer was always sputtered in a single session together with subsequent electrode metal layers: AlSi/Mo/AlSi. The dry patterning of TiW in SF_6/BCl_3 plasma always took place only after the more experimental wet-etching of the other electrode layers. In the TiW etching, we planned to either exploit the photo-resist pattern of wet steps or to do without PR but, as explained in section 3.1.3., ended up with an extra PR-lithography step. The PECVD tetraethyl-orthosilicate (TEOS) oxide was dry etched for vias in two steps: fluorocarbon and SF_6 plasmas. Finally, the top AlSi was plasma patterned in a standard Cl_2 chemistry.
The wet etching of the electrode multi layer was more a part of the experiment than mere sample preparation. Accordingly, discussion on etching steps continues in chapter 3. Generally, a standard phosphoric-acid wet etchant PWS 80-16-4(65) by Honeywell was applied in aluminum and molybdenum etching. Freckle etchant by Fujitsu, containing phosphoric, acetic, fluoroboric, and nitric acids, was used for removing the amorphous Si precipitates left from AlSi.
Finally, PR of each lithography step was stripped by a two-step process which combines 75-minutes O_2-plasma stripping and 15-minutes Posistrip (by DuPont) wet remover. The Posistrip wet step takes place at T = 80 °C whereas the wafer temperature in O_2 plasma is 140 °C. After the electrode etching and after sacrificial-layer etching, PR-strip was varied by omitting the O_2-plasma in either one of the two steps as indicated “with/without O2 plasma : W/WO” in Table 1.

WAFER / STEP	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
TiW/AlSi/Mo/AlSi sputtering	A	A	A	A	AM	AM	AM	AM	AM	AM	AM	AMA	AMA	AMA	AMA	AMA	AMA	AMA
PWS 30C etch	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
Freckle (prior PR strip)	O	O	-	-	O	O	O	-	-	-	-	O	O	O	-	-	-	-
PR strip **W/WO** O2-plasma	W	W	W	WO	W	W	W	W	W	WO	WO	W	W	W	W	W	WO	WO
Freckle (after PR strip)	-	-	O	O	-	-	-	O	O	O	O	-	-	-	O	O	O	O
TiW plasma etching	O	O	O	O	O	O	O	O		O		O	O	O	O		O	
PECVD TEOS and patterning	O	O	O	O	O	O		O		O		O	O		O		O	
PR strip **W/WO** O2-plasma	W	WO	W	W	W	WO		W		W		W	WO		W		W	
Top AlSi sputtering and patterning	O	O	O	O	O	O		O		O		O	O		O		O	
TEOS HF-vapor removal	O	O	O	O	O	O		O		O		O	O		O		O	

Table 1. Processing differences of 18 sample wafers of types a), b) and c) of Fig.2. Dashed lines indicate samples and process phases of hillock and pit counting. Contact-resistances measurement is indicated by the double line. Blank columns indicate samples removed from processing for destructive SEM cross-section studies. Symbols “AM / AMA” refer to the two capping structures and “A” to bare AlSi. “O” indicates the step was done whereas “-” means not. “W / WO” stand for With / WithOut O_2 plasma in PR stripping.

2.3. Analysis Methods and Equipment

Layer thicknesses and the overall qualitative appearance of the samples at different phases of processing were studied through scanning electron microscope (SEM) imaging (LEO Supra 35 field-emission SEM, model year 2003). Beam acceleration voltage was 10 keV in figures 3b and 3c, 4 keV in figures 4 and 8, and 5 keV in other presented SEM images. Our SEM installation resolution is limited at 10 nm which dominates the inaccuracy in thickness determination for layers below 500 nm. The 1 µm and 1.5 µm AlSi layers were thick enough for a 2 % relative uncertainty to limit the accuracy.

An optical white-light profilometer WYKO SP3000 (Veeco Instruments Inc.) in vertical-scanning mode was applied for counting and categorizing hillocks and pits of electrode surfaces. After scanning 4 areas of 2700 μm^2 of each sample, isolated recesses and rises reaching depths and heights that exceeded the category limit were counted. Minimum visible lateral feature size was limited by a sampling step of 82 nm. The results are given normalized for 1000 μm^2 areal density. An automatic zero-level determination of the data was based on data mean. The possibility of very deep or high features shifting the mean from an intuitive zero-level was manually checked for any suspicious data.

Electrical dc contact resistances between layers were recorded by a four-probe current-voltage measurement. The daisy-chain test structure featured 20 vias of 1000-μm^2 area each in series.

3. Results

3.1. Patterning

3.1.1. AlSi and cap layers wet etching

The wet patterning of bare AlSi electrode (samples 1-4) proceeded through the PWS and Freckle etching without surprises. A typical spherical etch front is seen in Fig. 3a. Noteworthy are the "mouse bites" decorating the pattern edge as seen in Figs. 3b and 3c.

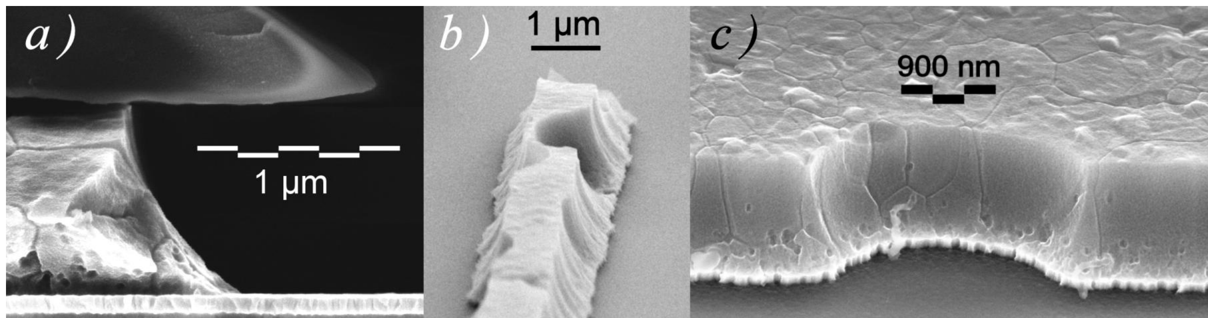

Fig. 3. SEM images of wet-etching results of bare TiW/AlSi electrode. a) Cross-section after PWS and Freckle etchings with PR still on top and non-patterned TiW at bottom ; b) and c) PWS-etching mouse bites shown after PR stripping and TiW-layer plasma etching.

Non-trivial results were recorded in wet etching of the Mo and Mo/AlSi capped multi layers. Molybdenum is etched faster than AlSi so that, instead of the spherical etch front, a slope is achieved. A potentially very useful 15-degree slope of a Mo/AlSi-capped multilayer was etched in PWS at T = 40 ^{o}C and is shown in Fig. 4 prior to the Freckle-etch removal of amorphous-Si residues.

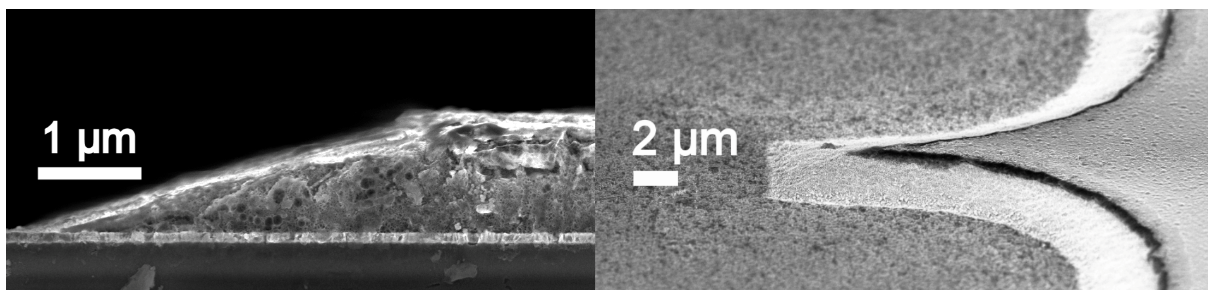

Fig. 4. A 15-degree slope resulted from PWS etching of Mo/AlSi-capped multilayer at T = 40 ^{o}C. Pictures show the sample prior to Freckle etching thus a grass mat of amorphous Si residues is still there.

We found the control of the slope difficult. For Mo in PWS etching at T = 30 ^{o}C and 40 ^{o}C, the test with samples of type f) of Fig. 2 yielded lateral etch rates of 600-900 nm/min and 1100-1400

nm/min, respectively. Vertical rates are 40 % faster due a columnar-grown structure of the Mo film. The PWS-etch datasheet and our own experience indicate AlSi rates 120 nm/min and 350 nm/min at T = 30 °C and 40 °C, respectively. Calculation suggests expecting slopes 8°-11° and 14°-18° at T = 30 °C and 40 °C. Most results, including that of Fig. 4, correspond to the expectations but, especially at T = 40 °C, wafer-to-wafer variation occasionally caused results 10° – 25°. Apparently the arrangement of Mo/AlSi capping with the fastest etching at second thin layer from PR is prone to lose adhesion to PR at etch front due the top thin AlSi collapsing after Mo-layer under cutting. As a result, the top surface etch rate and, accordingly, the resulting slope suffer increased variation. The unfortunate direction of the slope T-dependence challenges the control of overall under cut. The line-width control would benefit from steeper slope but, on the other hand, the high overall rate at T = 40 °C is problematic.

A positive result to note, common for both capping types, is the smooth appearance of the pattern edge line. The mouse bites seen in Figs. 3b and c for a bare-AlSi layer wet-etch result are absent.

3.1.2. Freckle etching

Results of the Freckle etching after PWS step could not be explained by a single etch rate of AlSi. Thin layers of AlSi or Mo are completely removed in Freckle etch. All capped samples that had PR stripped prior to Freckle etching (Table 1. samples 8-11, 15-18), independent of PR-strip method, lost their capping layers as shown in Fig. 5 for sample 18. Also the thin part of capped-AlSi pattern-edge slope was cut away up to some 350-nm thickness. However, exposure to Freckle etch does not thin down the 900-nm thick AlSi within a 30 nm repeatability in our observations. The steeper slope of non-capped AlSi is only cut in case the PWS-step under cut was minimized and the slope shallow part thus left longer than the example seen in Fig.3. An etch rate above 100 nm/min for thin layers but below 10 nm/min for thick AlSi is not in line with existing data [21] as discussed in chapter 4. The samples with PR stripped only after Freckle etching kept their capping layers, as shown in Fig. 6, but still lost the thin end of the slope.

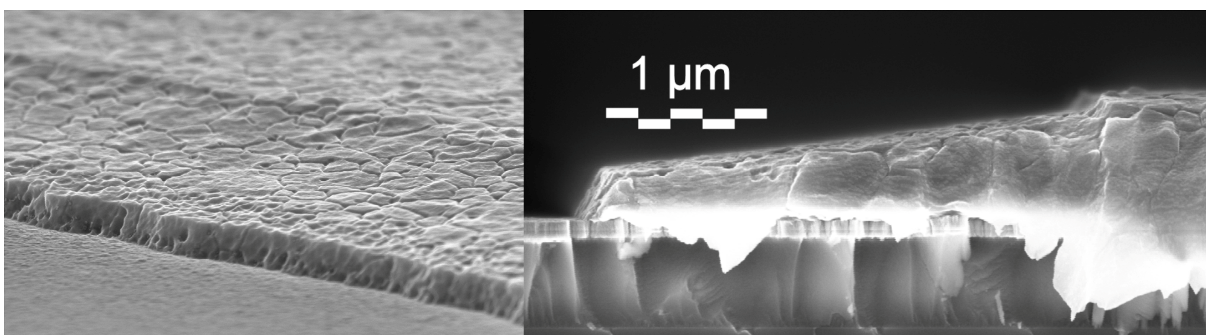

Fig. 5. Sample 18 Freckle etched after PR stripping. Capping layers (Mo/AlSi) are gone and the 3-µm slope is cut at 300-nm thickness. PWS etch at T = 30 °C resulted 7-degree slope.

Further studies with samples of types f, g, and h of Fig. 2 revealed that thin Mo or AlSi is etched in the Freckle also when sputtered on a Si-substrate surface. The single-crystalline Si substrate itself was etched in the Freckle at a rate of 60 nm/min with near 50 % inaccuracy in the result.
We further observed that Mo is etched in the Freckle independent of the thickness. Even though Freckle-etch time was never varied from standard 3 minutes, vertical rate was estimated 500 nm/min based on different etch-depths of Si-substrate under thin and thick Mo films. With thick Mo, the lateral rate (undercut) is some 50 % slower due to columnar structure of the film. The lateral rate goes fast further down with decreasing film thickness.

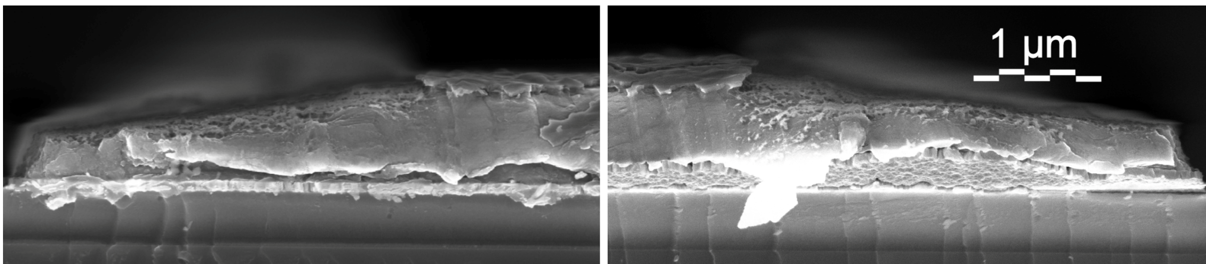

Fig. 6. Cross-section images of sample 7 Freckle etched when PR still shielded the Mo capping layer. Mo is seen still there on top surface where the slope ends. PWS at T = 30 ^{o}C resulted 7- and 8-degree slopes of length 3.2 µm cut at 350-nm thickness.

3.1.3. TiW plasma etching

A discourse of trials and errors of process-flow integration left us with single option of an etching sequence with the desired result. The plasma-etching of the 70-nm TiW-layer at bottom of the multilayer electrode appeared too insecure with the initial PR masking used for the electrode wet etching. The PR pattern having experienced a sequence of four wet steps (PWS, rinse, Freckle, rinse), small features occasionally end up dislocated on the wafer. The anisotropic plasma etching may then leave short-circuiting connections between conductors meant isolated. As a result, PR must be stripped after Freckle etch.
The TiW etching cannot, however, be done without PR still shielding the pattern. The SF_6/BCl_3 plasma reacts at the cap-layers pattern edge yielding precipitates up to several micrometers dimensions. We indeed expected trouble in using Mo-only cap on AlSi as the etch mask but believed Mo/AlSi cap would perform better. Now, the location of precipitates is special in that Mo and AlSi may locally both be exposed to plasma chemistry. In the case of Mo-only cap, this is clear but, with Mo/AlSi capping, the electrode surface main area is shielded against Mo exposure to the plasma chemistry. However, at the pattern edge, the order of the cap-layers borders is not well defined. Between the slope and the pattern inner area, Mo/AlSi-capped samples show a transition layer where faster-etching Mo has at least partially solved in PWS and in Freckle but, thin AlSi on top is not fully removed (Fig. 7). Still, faster wet etching of Mo does not always ensure all Mo

being well shielded by the thin top AlSi. Occasionally, thin AlSi may have collapsed or fractured during the wet steps thus allowing plasma to permeate and reach the Mo layer.
A detailed examination of the phenomenon was out of the scope of our study. The problem was circumvented by repeated PR lithography of the same electrode pattern. Alignment, such that the latter lithography covers all cap-layer edges, is straight forward since PWS wet etching has shrunk the pattern several micrometers smaller compared with the photo mask.

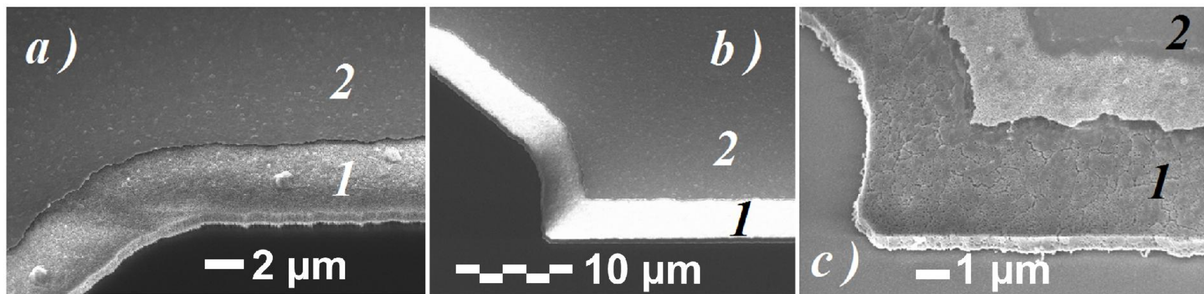

Fig. 7. a) and b) Top views of Mo-capped sample 7 and c) of Mo/AlSi-capped sample 14 after Freckle etched when PR still shielded the capping layers. Slope is indicated 1 and multi-layer top surface 2. Slope of sample 7 shows hillocks in a1) while surface is smooth. Sample 14 in c) well reveals a transition zone from slope 1 to top surface 2. Pictures also reveal the smooth pattern edge line free from mouse bites.

3.2. Hillocks and Pits

Hillocks and pits, portrayed in Fig. 8, were counted after the PR strip of the electrode patterning and after the Freckle etching. In addition, samples 1, 5, and 12 (types (a), (b) and (c) of Fig. 2) were re-studied after the sample-preparation process flow was completed. All open TEOS-oxide, not coated with 1.5-µm AlSi, was removed in anhydrous HF-vapor.

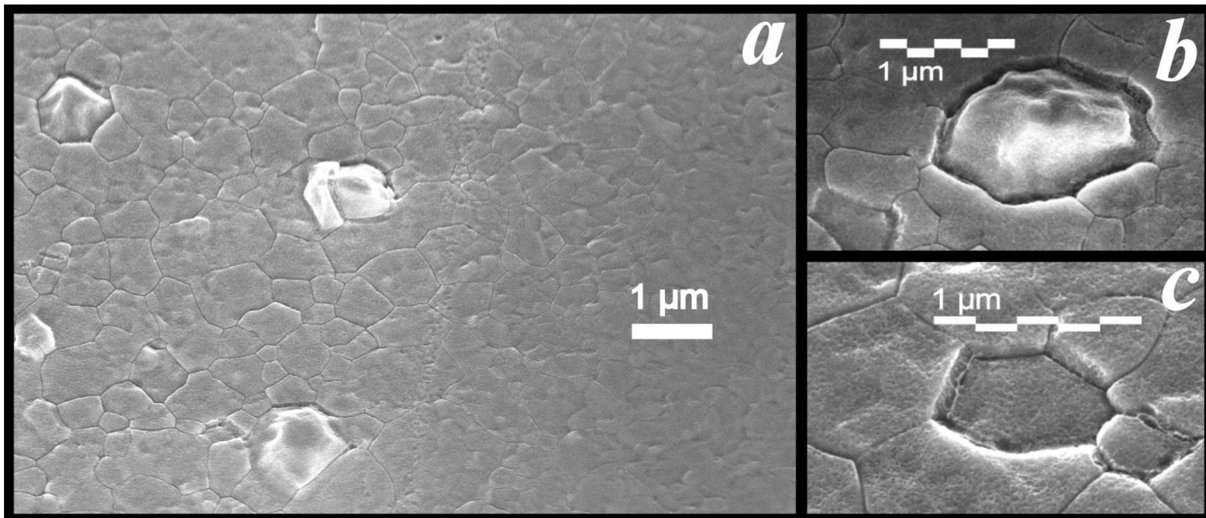

Fig. 8. SEM images of hillocks and pits on AlSi surface. a) Left from a transition zone, Freckle etching removed thin capping Mo/AlSi from top of 1-µm AlSi prior to O_2 plasma treatment. Right from the zone, Freckle-etch removed the cap layers only after O_2 plasma. Remarkable difference is clear. LHS features severe hillocking and distinctive grain boundaries whereas RHS remains smooth. b) A portrait of a typical hillock. c) A typical pit recess.

The result of the first counting, in terms of hillocks only, needs no graphs to state. Bare AlSi with O_2-plasma PR stripping generates near 10 hillocks per 1000 μm^2 of heights up to 500 nm whereas, both Mo and Mo/AlSi capping prevent all hillocking. Sample 4 (bare AlSi with only Posistrip PR strip) shows only 50 nm hillocks with density less than 2/1000 μm^2. The observations indicate the O_2-plasma PR stripping is the process responsible for most hillock growth. Note how the several-µm slope of the capped structures essentially represents a non-capped bare AlSi surface. The slope may thus grow hillocks as shown in Fig. 7a even if the top surface remains nice and smooth. Looking at pits reveals more interesting dependences (Fig. 9). Bare AlSi again shows worst pit formation in O_2 plasma but now sample 3 exceeds samples 1 and 2 far beyond. The difference is the Freckle etching after the O_2-plasma PR stripping. Since sample 4 with the PR stripped in Posistrip shows very little pits, Freckle alone on an exposed AlSi surface is harmless but seems very influential after the O_2 plasma.

The electrodes with Mo (samples 5-11) and Mo/AlSi (samples 12-18) capping restate the observation. Pits are formed in the O_2 plasma since samples 10,11,17,18 with the Posistrip PR stripping show least pits. Again, the Freckle etching has significantly increased pits when applied after the O_2 plasma (samples 8,9,15,16) but has no effect when preceded by the Posistrip PR stripping. The effect of the Freckle removing the cap layers is common for both the low and the high extremes in pit formation, i.e., for all Mo-cap samples 8-11 and Mo/AlSi-cap samples 15-18.

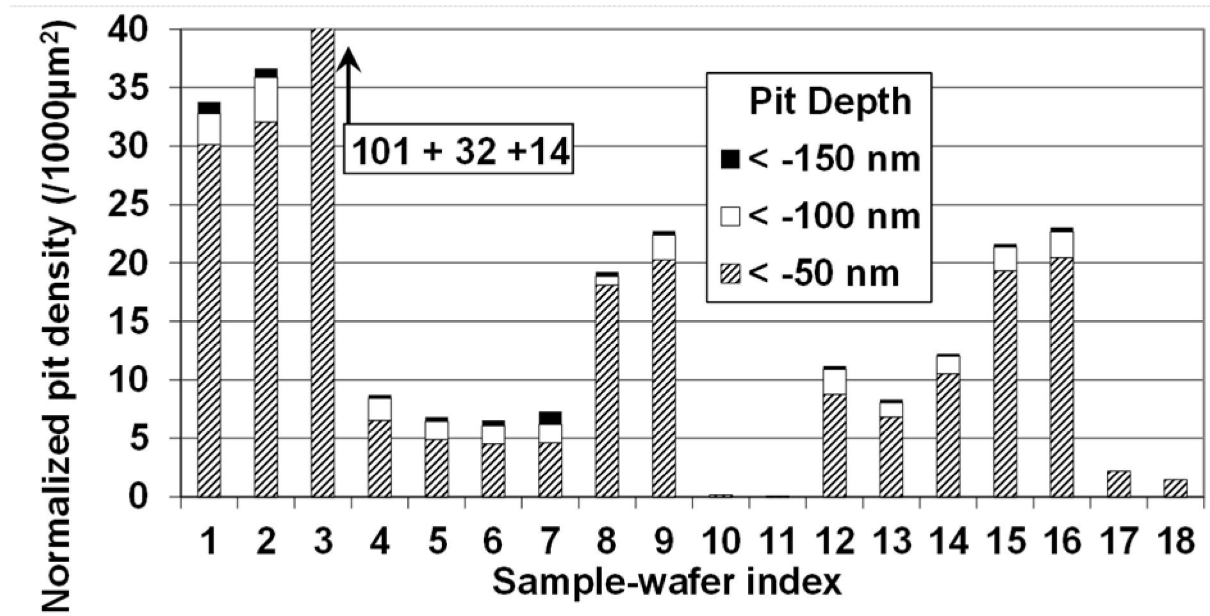

Fig. 9. Pit densities as number per 1000 μm^2 for each sample. Three categories of pit depths are piled incrementally in each bar.

A small difference between cap compositions is observed. Few shallow pits were found with Mo/AlSi cap even without plasma stripping of the PR (samples 17, 18) whereas, almost none with Mo cap (10, 11). Also samples for which the Freckle exposure did not remove the cap layers show clearly more shallow pits with Mo/AlSi capping (samples 12-14) compared with Mo-only cap (samples 5-7).

Final counting of hillocks and pits of sample wafers 1, 5, and 12 was done after HF-vapor removal of the TEOS oxide where not covered by the top 1500-nm AlSi. The non-capped bare AlSi consistently generates more and higher/deeper hillocks/pits than the capped versions. An interesting observation in Fig. 10 is that, during later processing steps, sample 5 with Mo-cap electrode has grown much more hillocks than Mo/AlSi capped sample 12. However, the few of sample 12 are taller. Pit formation does not make that significant difference between the capping types even though the deepest pits were only found for the Mo-cap version.

Generally, increased hillocking in later processing is explained by the TEOS-deposition temperature of 350 ^oC and by the two more hot plasma strips of the PR: those of the lithography PR for the TEOS and for the top AlSi.

An indication of the uncertainty level is the apparent cutting of sample 12 pit density by half during processing. The observation is not likely to represent a real result but is merely attributed to different locations of wafer.

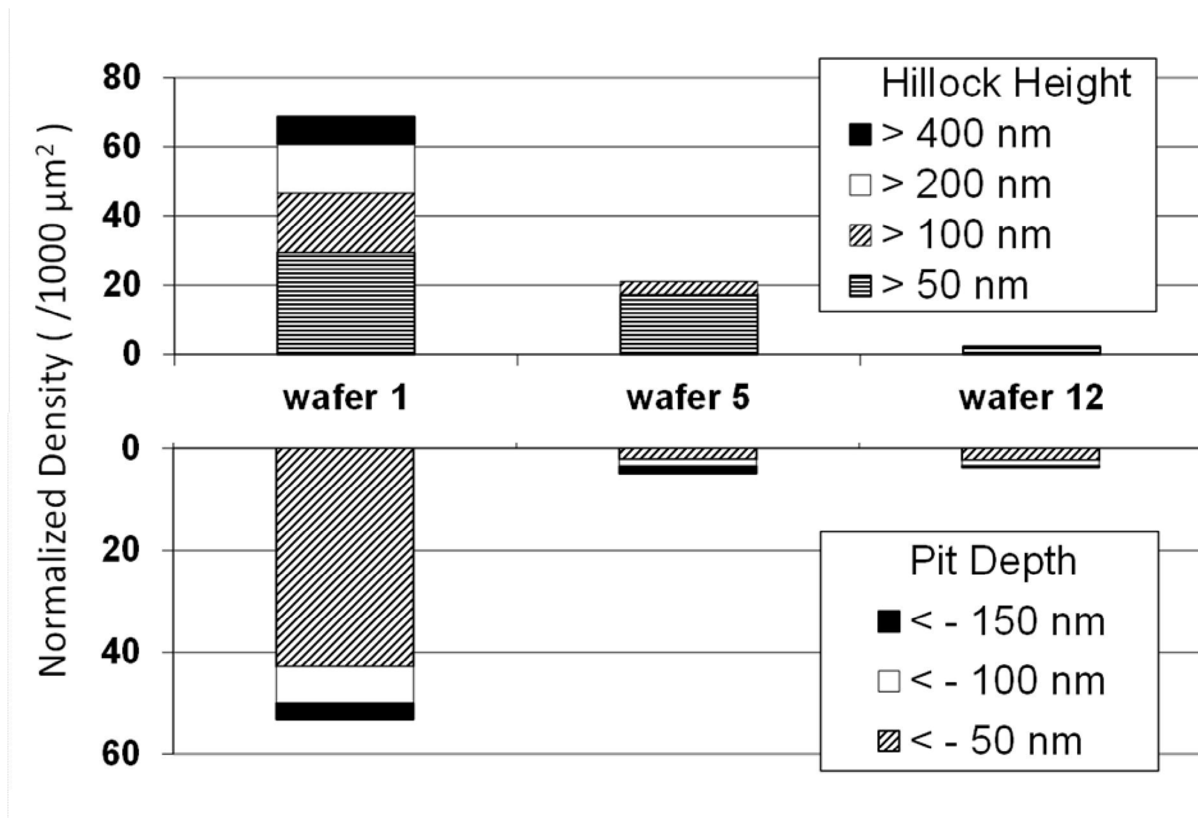

Fig. 10. Categorized hillock and pit densities after complete process flow which included top AlSi sputtering and patterning and TEOS-oxide removal.

3.3. Contact Resistances

Daisy-chain resistances between the multi-layer electrode and the thick top AlSi are split in two (Fig. 11). Both the samples initially sputtered bare AlSi and those left without cap layers after the Freckle exposure yield high contact resistance. All samples with the cap layers, whether Mo or Mo/AlSi, exhibit good-quality contact to the top AlSi layer. Samples 2, 6, and 13 did not observably benefit from skipping the O_2-plasma in PR stripping after TEOS-oxide vias etching.

The contact resistance between the TFR-pattern and the fixed electrode (Fig.1 (6)) needs an oxide-reducing adhesion layer. Direct sputtering of the fixed-electrode AlSi onto the TFR, exposed at the vias (Fig. 2d), resulted a non-Ohmic contact which insulates at dc. The TiW-layer and the extra effort for patterning it, as explained above in section 3.1.1., was thus proven necessary.

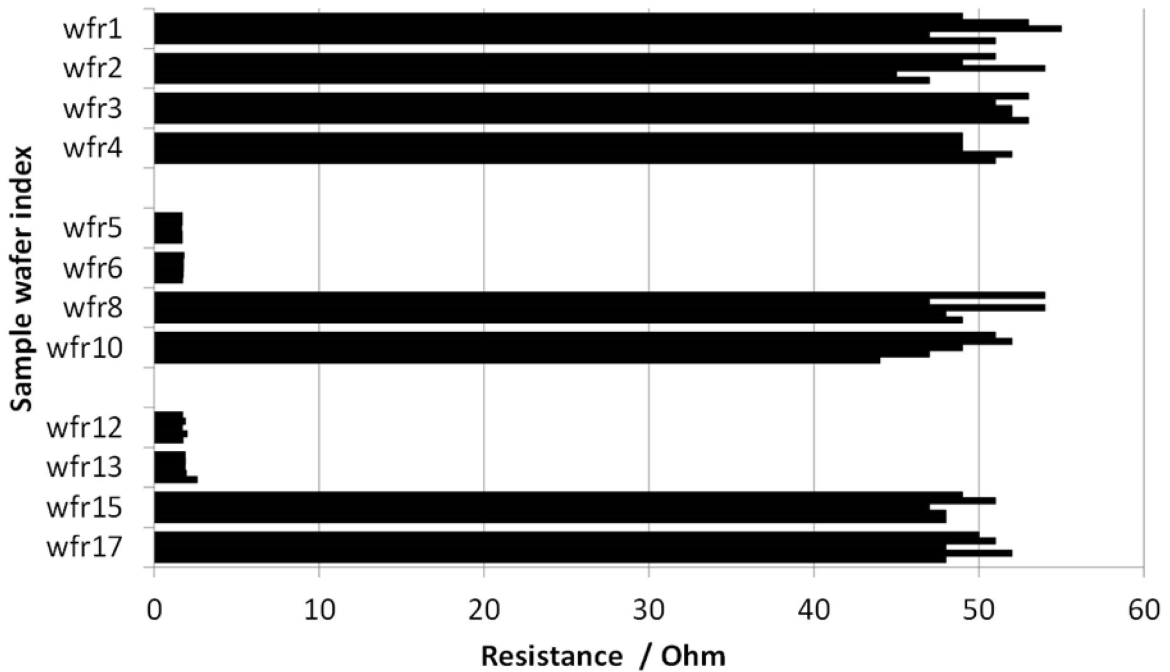

Fig. 11. Resistances over a daisy-chain of contacts between fixed electrode and released-electrode anchors (see also Fig.1. (7)). Bar-bundles show five measurement locations over wafer. Grouping follows the initially sputtered electrode type: Top bare AlSi, middle AlSi/Mo, bottom AlSi/Mo/AlSi. Samples of logically missing numbers were consumed in SEM studies prior to these measurements.

4. Discussion

We revealed certain processing issues induced by the Freckle etching which is needed to accompany the wet etching of AlSi. Thin AlSi layers and all Mo layers exposed were removed at a rate exceeding 100 nm/min whereas thick AlSi is etched less than 10 nm/min or not at all. We believe the key difference between the thinner and the thicker layers is in the grain size and in size ratio to film thickness. The conflict with previously published data that introduces a general AlSi etch rate in the Freckle etch may originate from differences in AlSi sputtering processes and thus from the film grain structure. Assuming both conflicting data are correct in respective sample-preparation facilities, our results suggest caution when planning process flows that involve AlSi exposure to the Freckle etchant.
The Freckle etching was seen to deepen the pits when applied after a hot O_2 plasma. The associated apparent increase in pit number density can be attributed to the same phenomenon with an original pit shallow enough to be ignored but counted after deepened. We anticipate the effect manifests Si accumulation at AlSi grain boundaries such that the Freckle etch, indeed intended for amorphous-Si removal, attacks the Si. A visually distinctive “opening” of the grain boundaries after exposure to hot O_2 plasma and to Freckle etch was seen in Fig. 8. The test did not resolve whether the effect of the Freckle etch after the O_2 plasma was due combination of the treatments or, whether the Freckle

simply grows the pits deeper after they were born by any origin. Considering the pit formation and the grain collapse of Al or AlSi film is generally attributed to thermal stress, any initiation of pits is not likely to take place in the room-temperature Freckle etch. The effect of the Freckle etchant would thus be to merely continue the pit formation by further weakening the forces that act against thermally-born stresses at grain boundaries at the pit periphery.

Another question left open was the property through which the Mo/AlSi capping performed differently to the Mo-only cap. The difference may originate from material composition but also simply from thickness. Essentially the result may only indicate 50+50=100 nm cap is stronger to 50 nm.

The accuracy of our quantitative data is limited by several sources of variation. The pattern-edge slopes vary due uncertainty in the condition of the cap layers and in their interface to PR during PWS wet etching. The top AlSi of the Mo/AlSi cap may collapse and, generally, thin cap layers do not make a repeatable liquid-flow channel. Finally, inaccuracy of the hillock and pit densities is reflected in the observation of one sample apparently gone down in pit number along further processing, which most probably did not really happen.

5. Conclusions

An applicable AlSi electrode in terms of contact resistances, surface quality, and pattern-edge slope was achieved. The data provides arguments for choosing between the cap-layer types and wet-etch temperatures, according to the application preferences. The presented phenomena suggest a process flow including the Freckle etch with PR left on, followed by PR strip, and repeated lithography for the TiW plasma etching. RF circuitry incorporating the MEMS switch and the electrode here presented has since been realized and will be reported later.

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