Title	Gravure printed low voltage polymer transistors and inverters
Author(s)	Hassinen, Tomi; Sandberg, Henrik
Citation	Thin Solid Films. Elsevier, Vol. 548 (2013), Pages 585 - 589
Date	2013
URL	http://dx.doi.org/10.1016/j.tsf.2013.09.070
Rights	This is a post-print version of the published article and it may be downloaded for personal use only.

Gravure printed low voltage polymer transistors and inverters

Tomi Hassinen*, Henrik G.O. Sandberg

VTT Technical Research Centre of Finland, Tietotie 3, Espoo, FI-02044 Finland
*Tomi.Hassinen@vtt.fi

Abstract

We present a gravure printed low voltage transistor using commercial polymer materials. Patterned thin layers (down to 200 nm) were formed by single printing steps on *polyethylene terephthalate* substrates which had pre-patterned metal electrodes. Materials were air stable and there was no need for substrate or metal electrode pre-treatment. Good electrical performance with minimal hysteresis was achieved. Low voltage operation is demonstrated with inverter circuits, which operate down to 5 volts.

1 Introduction

The low cost printed electronics needs high throughput printing processes. Gravure printing is one of the most interesting methods as it simple, fast and cost effective [1]. It has been used in combination with other processing methods to partially or fully print electronic components [1–12]. For printed polymer thin film transistors, the gate dielectric thickness has been usually 0.5-2 µm thick in order to get a good yield without short circuits. The thickness raises the operation voltage to tens of volts, and that is too high for real applications. Use of high-k dielectrics could lower the operation voltage, but they must be used in combination with another low-k dielectric, adding one processing step [5].

Here we present gravure printed low voltage polymer transistors on flexible substrate. The materials were a low-k dielectric and an air stable semiconductor from *Merck*. By using pre-patterned metal electrodes on *polyethylene terephthalate* (PET) substrate, we could make transistors with varying dimensions. The dielectric layer was scaled down to 200 nm. Transistors and inverter circuits made of the interconnected transistors were characterized. The results are intended to show the potentiality of the gravure printing also for the thin layers of the electronics components, and that with more recent materials the performance would be close to what is needed for real applications in low cost large area electronics.

2 Experimental details

Semiconductor *Lisicon SP0300* and a matching dielectric *Lisicon D320* were acquired from *Merck*. Materials came as ready-to-use printing inks. Semiconductor had 1% and dielectric 10% solid content in *mesitylene* and *n-decane* respectively. *Poly(methyl methacrylate) PMMA* was also tried as a gate dielectric. Two inks with concentrations 4

and 8% were prepared by dissolving *PMMA* (996 000 Mw *Sigma-Aldrich*) in a 1:1 mixture of *butyl acetate* and *ethyl lactate*. We used *Melinex ST504 PET* substrates. They had lithographically patterned high definition 40 nm thick gold source and drain electrodes.

Air and processing stability of the materials was studied by making *spin coated reference* samples in different conditions. Spin coating (semiconductor 1000 rpm 20 s, dielectric 1000 rpm 30 s) was done in air or in nitrogen glove box. Drying of the films was done in nitrogen, air or vacuum oven at 100°C for 20 minutes. There is no significant difference in the performances between the transistors made with different methods. Later the *printed* transistors showed similar stability and performance.

PET substrates with pre-patterned gold electrodes were cleaned and used without adhesion related pre-treatment. Printing was done with *Schläfli Labratester* gravure printer in normal laboratory environment. Machine dependent printing settings were: speed 6 m/min and pressure dial at 4.2. Gravure printing test plate had 8 different line densities. Transfer volumes of the gravure plate cells were measured with *Nanofocus µSurf* optical profilometer. Printed sample was dried in oven at 100°C for 20 minutes. Both semiconductor and dielectric were printed with the same plate and dried the same way. Printed film thicknesses were measured with Dektak 150 profilometer. Several sets of film thickness combinations were printed. The transistor structures were completed by top gate deposition (40 nm gold) through a shadow mask in the thermal vacuum evaporator. Transistors from the best set were connected together in diode connected load configuration (enhancement mode driver and load transistors) [13], forming inverter circuits (Fig. 1).

3 RESULTS AND DISCUSSION

3.1 Transistors using Lisicon D320 dielectric

The printed semiconductor was 10-80 nm and dielectric 200-560 nm thick. Thickness was proportional to the transfer volume of the cells (Fig. 2). Ink transfer ratio from gravure cells to the substrate was over 50%, which is remarkably high [14]. The printed semiconductor film quality was poor, as there were thickness variations and some wetting differences on the substrate and the gold film. Still the semiconductor formed a continuous layer on top of the interdigitated source and drain electrodes. The dielectric film had better quality. There were only minor thickness variations. Edge quality is limited by the gravure cell size (Fig. 3). Dimensions of the test transistors were: channel length 5-20 µm, channel width 8-80 mm.

Electrical measurements show that even though the semiconductor film seemed to have poor quality, the transistors work very well. The performance of the printed transistor is similar or better than the spin coated reference transistor with roughly the same

dimensions (Fig. 4). That must indicate that the semiconductor film did form properly on the channel area (between interdigitated electrodes), and the uneven areas outside the active area did not cause noticeable degradation in performance. Transistor output and transfer curves show good saturation (Fig. 5-6). The gate leakage current is at a low level even for the thinnest dielectrics. Table 1 shows the characteristics of the transistors in the best set. The best combination was with the thick semiconductor (70-80 nm) and thin dielectric (220-250 nm). The semiconductor thickness affects the *Off current* and *mobility*, and often the optimal value is between 50 and 100 nm [15], [16]. Decreasing of the dielectric thickness enhances the transistor performance by decreasing *operation voltage*, *subthreshold slope* and *threshold voltage* (see Table 1 and Fig. 7) [17–19]. Electrical current-voltage and capacitance-voltage measurements in Fig. 4-6 and 8 show overlapping forward and reverse sweeps. This low *hysteresis* and the *threshold voltage* at the thinnest dielectric thicknesses indicate a good interface is formed between the active layers. *Permittivity* of the dielectric is 2.2, which is one reason for the low hysteresis [5]. *Interface trap density* was calculated according to the method used by [20], [21].

$$N_{Trap}^{Max} \approx \left[\frac{qS \cdot \log(e)}{kT} - 1 \right] \frac{C_{ins}}{q} \qquad (1)$$

In the equation (1) the dielectric capacitance C_{ins} was 9 nF/cm^2, q was the *electronic charge*, k the *Boltzmann's constant* and T *temperature*. Subthreshold swing S values were 1.25 and 2.25 V/dec for forward and reverse sweeps (Fig. 6), and the calculated *interface trap densities* were $1 \cdot 10^{12}$ cm^{-2} and $2 \cdot 10^{12}$ cm^{-2} respectively. Another methods where the difference between *turn on* and *threshold voltage* [22] or *hysteresis* ΔVth [21] was used to estimate the trap density were also tried. As the turn on and threshold voltages reached low values, the resulting calculations were inaccurate or gave unrealistic values. Equation 1 gives a more reliable estimate of the interface traps in this case. The result is good for such a printed air stable polymer transistor [20–22].

Contact resistance was calculated using *transmission line method* [23]. Total source to drain resistance was calculated from the transistor output data at -1 V_{DS} and -10, -15, and -20 V_{GS}. The extrapolated *normalised* single *contact resistance* is in the range of 100 kΩ·cm at -20 V_{GS} (Fig. 9). The value agrees with the ones typically achieved with staggered organic transistor [7], [23], [24].

The sample set with the best values in Table 1 was used in the inverter tests. Varying Load and Drive transistor size (W/L) combinations were tried with ratios 1:3 – 1:50. Larger size ratio between load and drive transistor resulted in larger amplification, but slower operation speed due to larger relative RC time constant [25]. Voltage amplification clearly above unity was achieved with size ratios over 1:10 (Fig. 10). The *Off* to *On* transition of the drive transistor is fast, but the *On* to *Off* transition takes time as the charge in the channel must go through the large impedance of the load (Fig. 11). Rough estimation using the channel capacitance and diode connected transistor current at

the working voltage yields the time constant of ~0.2 seconds, which is about the same as shown in the Fig. 11. Working inverter shows the potentiality of the use of printed polymer transistors in more complex logic circuits even at low voltages.

3.2 Transistors using PMMA dielectric

Transistors were also made with similar process but replacing the *D320* dielectric with *PMMA*. The printed dielectric layers were very thin, dropping the yield of the pinhole free processing to less than 40% for 190-180 nm thick and to 0% for thinner layers. Again the *threshold voltage* was very low, between -0.5 and 1.5 volts for all the transistors measured. *Subthreshold slope* was 1.0-1.8 V/dec and 3.1-3.5 V/dec for forward and reverse sweeps respectively. But the *mobility* was 0.0005 $cm^2/(Vs)$, when with *Lisicon D320* dielectric it was 0.04 $cm^2/(Vs)$. As the other values do not indicate problems, the reason for the mobility degradation could indeed be the *energetic disorder* and *enhanced charge carrier localization* suggested by [5]. The more *polar PMMA* with a permittivity between 3.3 and 3.9 has larger polarization effect reaching through the interface to the active semiconductor layer. The active layer of this semiconductor is sensitive to the polarization effect, but it obviously does not indicate that *PMMA* would not work with other semiconductors [26].

4 Conclusions

The results show that with modern materials an air stable and hysteresis free gravure printed transistors and inverters can operate at low voltages. The studied material combination is otherwise excellent, but the semiconductor is inherently limited by its mobility. More recent polymer semiconductors with mobility between 0.1 and 1 may prove to be as well printed in thin layers, thus making low cost large area electronics possible with a performance close to amorphous silicon and small molecules.

References

[1] P. Kopola, M. Tuomikoski, R. Suhonen, A. Maaninen, Thin Solid Films 517 (2009) 5757.

[2] J.-M. Verilhac, M. Benwadih, A.-L. Seiler, S. Jacob, C. Bory, J. Bablet, M. Heitzman, J. Tallal, L. Barbut, P. Frère, G. Sicard, R. Gwoziecki, I. Chartier, R. Coppard, C. Serbutoviez, Organic Electronics 11 (2010) 456.

[3] M. Hambsch, K. Reuter, M. Stanel, G. Schmidt, H. Kempa, U. Fügmann, U. Hahn, A.C.C. Hübler, Materials Science and Engineering B 170 (2010) 93.

[4] H. Yan, Z. Chen, Y. Zheng, C. Newman, J.R. Quinn, F. Dötz, M. Kastler, A. Facchetti, Nature 457 (2009) 679.

[5] M.M. Voigt, A. Guite, D.-Y. Chung, R.U. a. Khan, A.J. Campbell, D.D.C. Bradley, F. Meng, J.H.G. Steinke, S. Tierney, I. McCulloch, H. Penxten, L. Lutsen, O. Douheret, J. Manca, U. Brokmann, K. Sönnichsen, D. Hülsenberg, W. Bock, C. Barron, N. Blanckaert, S. Springer, J. Grupp, A. Mosley, Advanced Functional Materials 20 (2010) 239.

[6] P. Kopola, T. Aernouts, S. Guillerez, H. Jin, M. Tuomikoski, A. Maaninen, J. Hast, Solar Energy Materials and Solar Cells 94 (2010) 1673.

[7] J. Veres, S.D. Ogier, S.W. Leeming, D.C. Cupertino, S. Mohialdin Khaffaf, Advanced Functional Materials 13 (2003) 199.

[6] A. de la Fuente Vornbrock, D. Sung, H. Kang, R. Kitsomboonloha, V. Subramanian, Organic Electronics 11 (2010) 2037.

[9] H. Kang, R. Kitsomboonloha, J. Jang, V. Subramanian, Advanced Materials 24 (2012) 3065.

[10] H. Kempa, M. Hambsch, K. Reuter, M. Stanel, G. C. Schmidt, B. Meier, A.C. Hübler, IEEE Trans. Electron Devices 58 (2011) 2765.

[11] G. C. Schmidt, M. Bellmann, B. Meier, M. Hambsch, K. Reuter, H. Kempa, A.C. Hübler, Organic Electronics 11 (2010) 1683.

[12] C. Kim, Z. Wang, H.-J. Choi, Y.-G. Ha, A. Facchetti, T. J. Marks, Journal of the American Chemical Society 130 (2008) 6867.

[13] H.-Y. Tseng, V. Subramanian, Organic Electronics 12 (2011) 249.

[14] X. Yin, S. Kumar, Chemical Engineering Science 61 (2006) 1146.

[15] S. Hoshino, T. Kamata, K. Yase, Journal of Applied Physics 92 (2002) 6028.

[16] H. Jia, S. Gowrisanker, G.K. Pant, R.M. Wallace, B.E. Gnade, Journal of Vacuum Science Technology A Vacuum Surfaces and Films 24 (2006) 1228.

[17] N. Gupta, Physica Scripta 76 (2007) 628.

[18] G. Paasch, S. Scheinert, Materials SciencePoland 22 (2004) 423.

[19] J. Veres, S. Ogier, G. Lloyd, D. De Leeuw, Chemistry of Materials 16 (2004) 4543.

[20] L.T.L. Teng, W.A Anderson, IEEE Electron Device Letters 24 (2003) 399.

[21] M. McDowell, I.G. Hill, J.E. McDermott, S.L. Bernasek, J. Schwartz, Applied Physics Letters 88 (2006) 073505.

[22] K.P. Pernstich, S. Haas, D. Oberhoff, C. Goldmann, D.J. Gundlach, B. Batlogg, A. N. Rashid, G. Schitter, Journal of Applied Physics 96 (2004) 6431.

[23] P. V Necliudov, M.S. Shur, D.J. Gundlach, T.N. Jackson, 2001 International Semiconductor Device Research Symposium Symposium Proceedings 47 (2001) 259.

[24] D. Boudinet, M. Benwadih, S. Altazin, R. Gwoziecki, J.M. Verilhac, R. Coppard, G. Le Blevennec, I. Chartier, G. Horowitz, Organic Electronics 11 (2010) 291.

[25] G.H. Gelinck, T.C.T. Geuns, D.M. de Leeuw, Applied Physics Letters 77 (2000) 1487.

[26] R. Ponce Ortiz, A. Facchetti, T.J. Marks, Chemical Reviews 110 (2010) 205.

Figures and a table

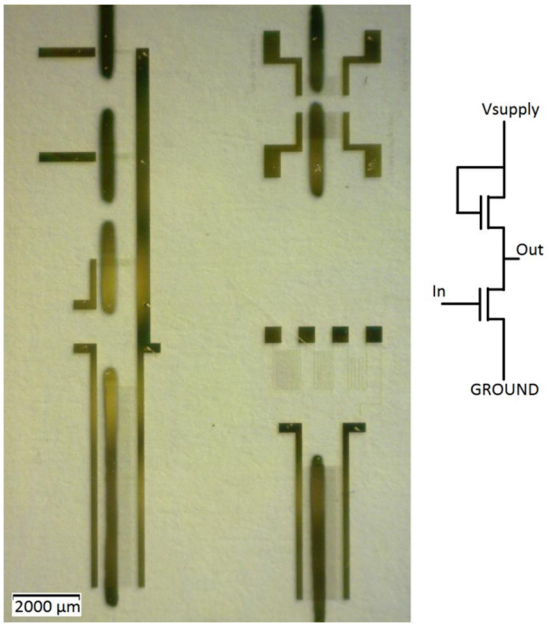

Fig. 1. Photograph of transistors and inverter circuits and the inverter schematics.

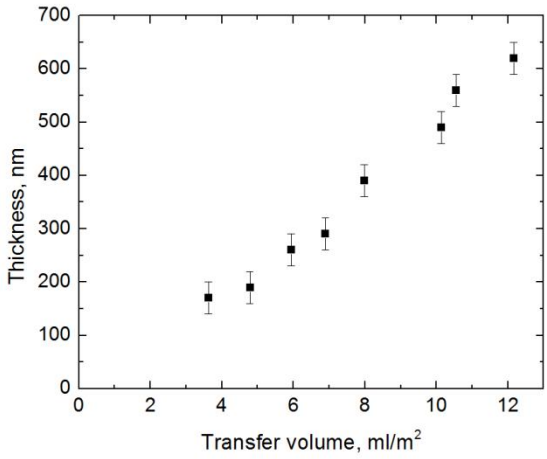

Fig. 2. Gravure printed *Lisicon D320* dielectric film thickness for 8 different gravure plate transfer volumes.

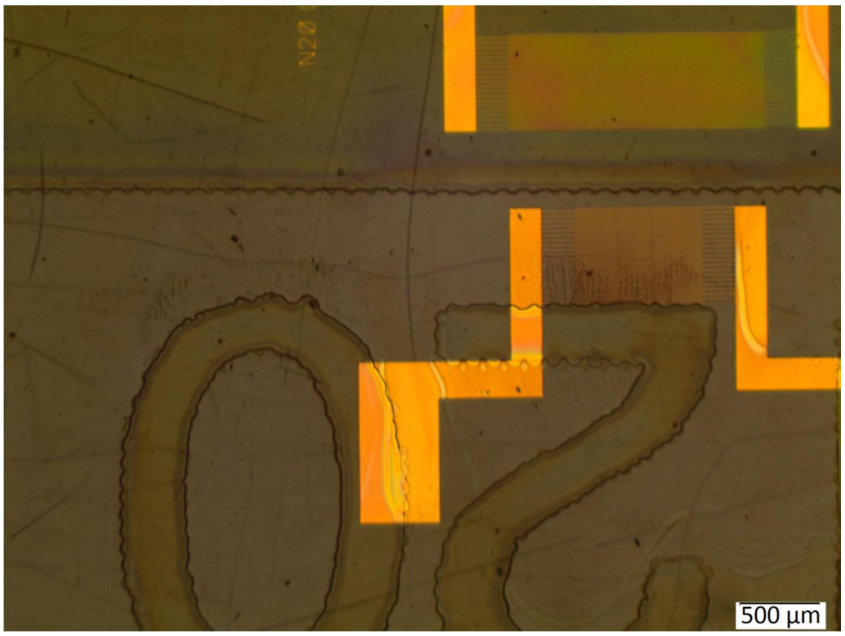

Fig. 3. Detail of a patterned feature printed with dielectric ink. Edge quality is following the gravure cell sizes. Printing line density was 120 lines/cm.

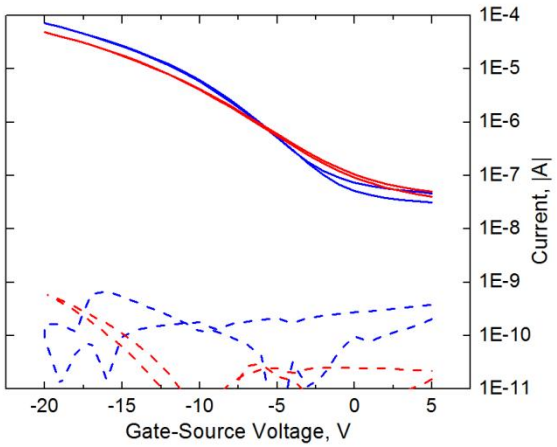

Fig. 4. A comparison of the transfer characteristics of spin coated (red) and printed (blue) transistors. Absolute drain current is shown with a solid line and the gate leakage current with a dashed line. Transistor channel length was 15 µm and width 6870 µm. The drain-source voltage was -20 V.

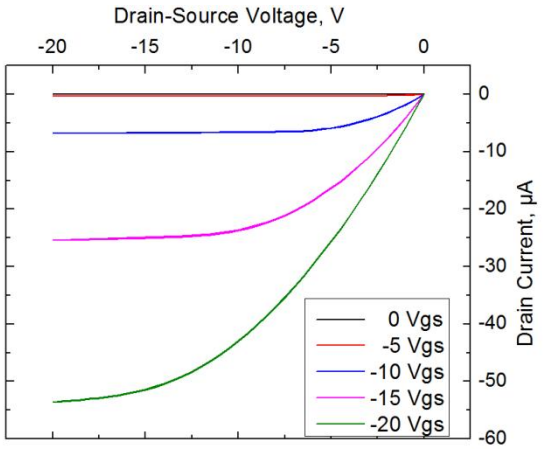

Fig. 5. Printed transistor *output* characteristics. Transistor channel length was 15 µm and width 6870 µm.

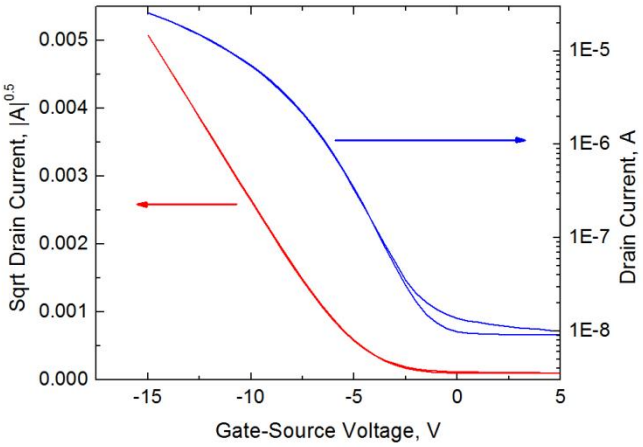

Fig. 6. Printed transistor *transfer* (I_D vs.V_{GS}) characteristics at -15 V_{DS}. Transistor channel length was 15 µm and width 6870 µm.

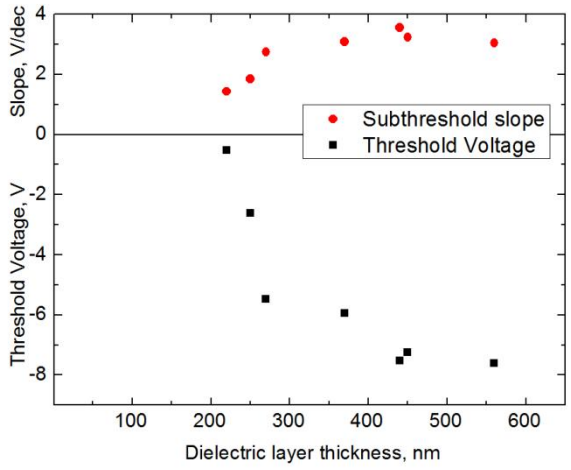

Fig. 7. Printed transistor *subthreshold slope* (red) and *threshold voltage* (black) plotted versus the printed dielectric thickness.

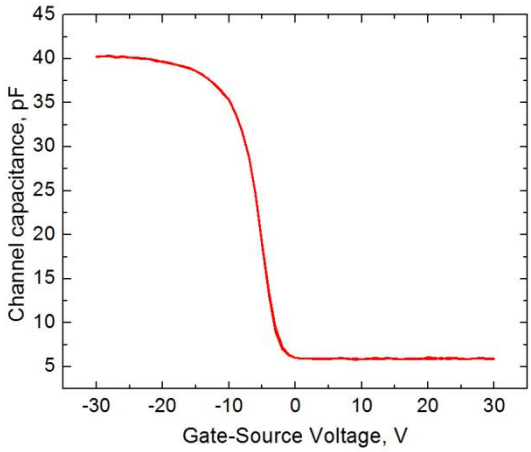

Fig. 8. Overlapping forward and reverse sweeps of *capacitance-voltage* measurement at -20 V_{DS} show no indication of hysteresis or *threshold voltage shift*.

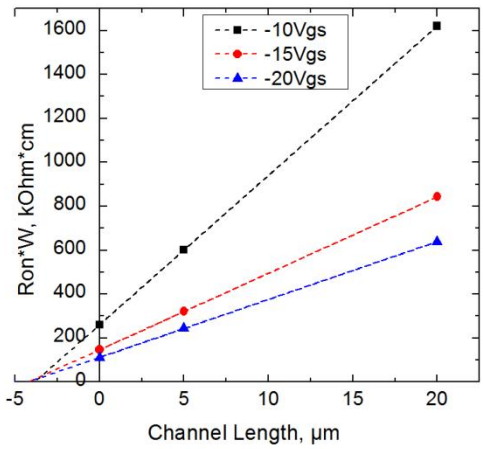

Fig. 9. The plot shows an example of *channel* and *contact resistances* of a transistor at gate-source voltages V_{GS}= -10 V, V_{GS}= -15 V and V_{GS}= -20 V. Drain-source voltage was -1 V.

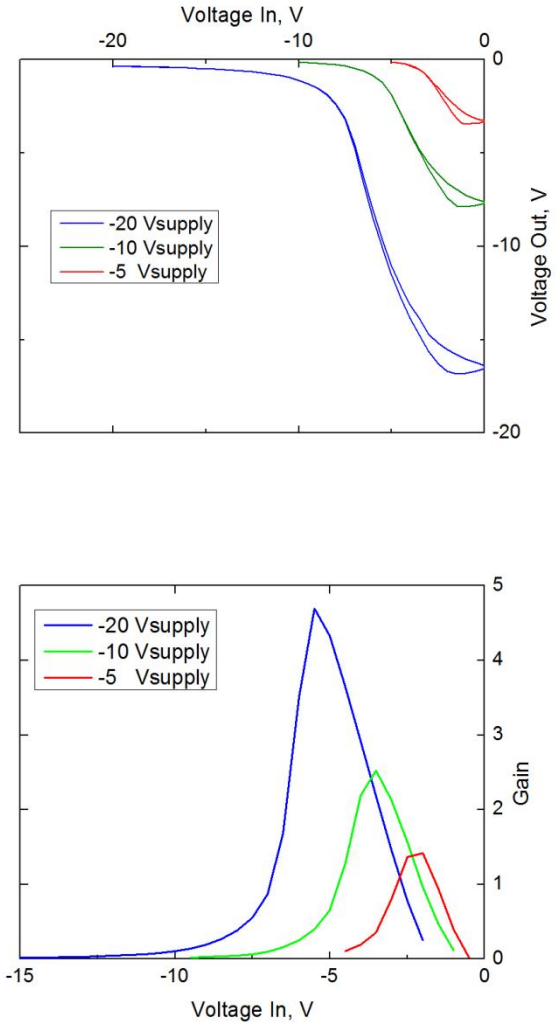

Fig. 10. The inverter worked at low voltages, shown by a) the *output swing* and b) corresponding *voltage gain* values at V_{SUPPLY}= -20 V, V_{SUPPLY}= -10 V and V_{SUPPLY}= -5 V.

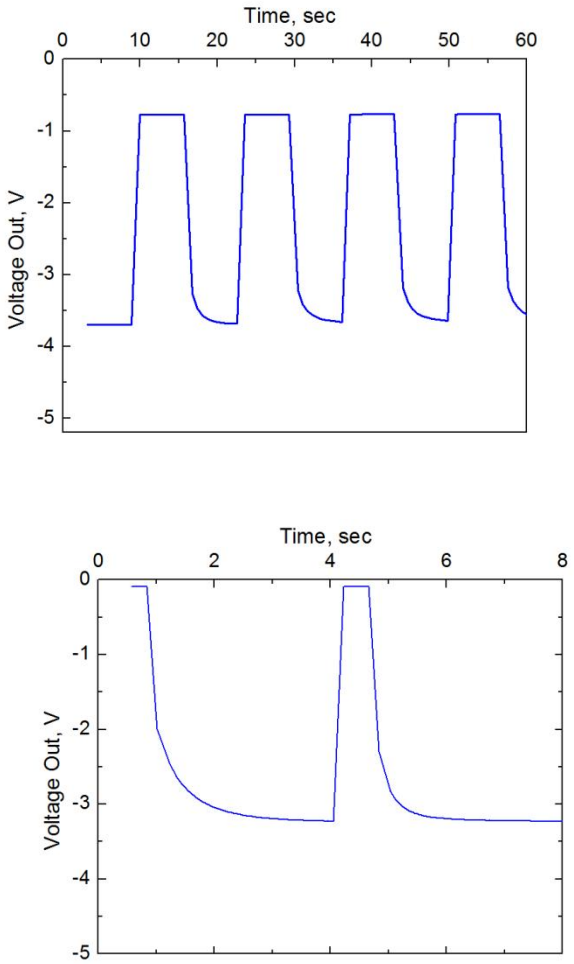

Fig. 11. Inverter dynamic characteristics are presented by the response to a 0 to -5 V *square wave* input signal. In a) the inverter had a *load:drive* size ratio of 1:10 and in b) 1:30. The long *On* to *Off* transition (closing) of the drive transistor is shown clearly. In b) the step time scale is different in order to show the full tail of the transition.

Dielectric thickness, nm	560	440	450	370	270	250	220
Mobility, $cm^2/(Vs)$	0.01	0.02	0.02	0.03	0.02	0.04	0.03
Threshold voltage, V	-7.6	-7.5	-7.2	-5.9	-5.5	-2.6	-0.5
On/Off ratio	4 000	1 400	2 200	6 800	4 000	7 500	6 500
Subthreshold slope, V/dec	3	3.6	3.2	3.1	2.7	1.8	1.4

Table 1. The transistor characteristics of a printed sample series with different dielectric thicknesses.