Title	Roll-to-roll compatible organic thin film transistor manufacturing technique by printing, lamination, and laser ablation
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Citation	Thin Solid Films. Elsevier. Vol. 571 Part 1 (2014), pages 212 - 217
Date	2014
URL	http://dx.doi.org/10.1016/j.tsf.2014.10.086
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Roll-to-roll compatible Organic Thin Film Transistor manufacturing technique by printing, lamination, and laser ablation

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Abstract

We present roll-to-roll printing compatible techniques for manufacturing organic thin film transistors using two separately processed foils that are laminated together. Introduction of heat assisted lamination opens up possibilities for material and processing combinations. Lamination of two separately processed substrates together will allow usage of pre-patterned electrodes on both substrates and materials with non-compatible solvents. Also the surface microstructure is formed differently when laminating dry films together compared to film formation from liquid phase. Demonstrator transistors, inverters and ring oscillators were produced using lamination techniques. Finally, a roll-to-roll compatible lamination concept is proposed where also the *source* and *drain* electrodes are patterned by laser ablation. The demonstrator transistors have shown very good lifetime in air, which is contributed partly to the good material combination and partly to the enhanced interface formation in heat assisted lamination process.

1. INTRODUCTION

In a roll-to-roll printing process the organic electronic devices are made typically with additive processes, i.e. the layers are printed on top of each other. Printing techniques are similar for all polymer devices (e.g. transistors, light emitting diodes [1], solar cells [2], sensors [3], and they all have the same principle limitations, although the most critical limiting restriction may be different. The transistor is a basic electronic component that can be used to very sensitively probe the different limitations of the manufacturing process, such as thin film layer thickness, morphology and roughness, feature size and registering accuracy. The basic device concept is described by Sze [4] and reviewed from a conjugated polymer and oligomer perspective by Horowitz [5-7]. Polymer transistor processing follows the same design rules as other printed devices. All layers of an organic thin film transistor (OTFT) can be printed [8], adding one patterned layer on top of another. However, the limited resolution of the printing processes limits the performance of such devices. In order to achieve better performance, the electrode dimensions and layer thicknesses must be small, and the *gate* to *source/drain* electrode overlap must be minimized. One approach is to use a pre-processed and pre-patterned [9] substrate with metal (or e.g. conductive transparent *indium tin oxide* (ITO) electrodes. A plastic substrate can have etched metal features with high definition providing excellent base onto which to build the device. After deposition of the active printed layers the top electrode must be deposited. In *top gate* configuration the need for resolution is not so strict therefore the *gate* electrode can be printed. However, the capacitance resulting from the gate-source/drain electrode overlap is a major component in limiting the switching speed of the transistor.

Furthermore, some of the active layers may not be compatible with the following printing step, or a high definition and high conductance top electrode is needed. For this case we introduce a lamination technique.

Lamination of a protective barrier foil is typically used as the last finishing step of the device fabrication [10], [11]. It has been shown to enhance lifetime of organic transistors [12]. But also the active layers can be laminated [13]. Lamination has been used in a *pentacene* OTFT when the interface was studied with *quartz* or *silicon* substrates [14] or with polydimethylsiloxane stamps [15], [16]. Another author uses lamination to make the electrode contacts for transistors [17], [18]. Semiconducting single crystals [19] or sheets [20] have been laminated on silicon wafers. Here we present the lamination of two plastic sheets with pre-patterned electrodes, with one containing the polymer semiconductor and another containing the polymer dielectric. By introducing heat and pressure, the sheets make the contact between the polymer layers. This technic allows the usage of materials with non-compatible solvents (no need for orthogonal solvent) [20]. It allows the use of pre-patterned (metal) electrodes on both sides. The active layers are automatically shielded by the two substrates. Also the surface microstructure is formed differently when laminating dry films together compared to film formation from solvent [14]. Lamination induced mobility increase in OTFTs, attributed to surface smoothening and relaxation of crystalline *pentacene* films has been reported by *Tunnell et al.* [14]. The molecular orientation and packing has improved the mobility when the film is annealed [21] or deposited by *solution-shearing* [22-24]. In the work by *Oh* [22], the pressure assisted thermal cleavage was done as post-treatment for the film, resulting in smoother surface roughness, void space removal, better crystallinity and thus increased mobility. All these reports indicate that the molecular packing can be enhanced in some cases by introducing shearing forces, pressure and/or temperature. This enhancement is studied in our work by comparing laminated devices with ones made with normal deposition methods. Scheme of the lamination process together with materials and printing methods are presented in Fig. 1 and 2. Possible applications could be e.g. electronic labels and signs with a display element and backplane lamination step (could simplify the process), smart cards and some sensor applications with sensitive layers.

2. Experimental

2.1 Materials

Silicon (Si) substrates with thermally grown *silicon oxide* (SiO_2) (thickness 300 nm) and patterned gold electrodes were used as rigid substrates, and *poly(ethylene terephtalate)* (PET) *Melinex ST504 DuPont Teijin Films* plastic sheets with or without ITO layer were used as flexible substrates. Patterned gold electrodes were either thermally evaporated through a shadow mask or patterned lithographically on the substrates. ITO layer coated on PET substrate was used only for *gate* electrodes and was not patterned.

Dielectric materials used in the lamination tests were *poly(methyl methacrylate)* (PMMA) (120,000 Mw), *poly(methyl silsesquioxane)* (PMSSQ), *poly(4-vinylphenol)* (PVPh) (25,000

Mw) and *poly(melamine-co-formaldehyde)* (PMF), a cross-linker for PVPh. Dielectrics and solvents *n-butanol, toluene* and *ethyl diglycol acetate* (EDGA) were purchased from Sigma Aldrich.

An undisclosed manufacturer provided *a modern amorphous polymer semiconductor*. Different version was used in the initial and the final tests (as an advanced version became available), but for consistency all the results were compared with reference devices made with the same material version. The comparison of the effects of different processing was thus possible.

2.2 Lamination

Lamination tests were performed with a range of different substrates, materials and configurations (see the materials section) in order to find combinations that result in working devices and a robust laminated structure. In a lamination process two substrates with varying processed layers were attached together on a hot plate by applying pressure (10-40 kN/m^2) and heat (140-160°C) for 15-20 minutes. Reference samples without the lamination step were made by spin coating organic layers on Si/SiO_2 substrate, or by printing the dielectric and semiconductor on ITO-coated PET substrate and evaporating top *source* and *drain* electrodes. All tests were done manually with small sheets. The roll-to-roll process was not tested due to lack of compatible machinery with high registration requirement.

First lamination tests were done utilizing *n-type Si* substrate with lithographically patterned gold *source* and *drain* electrodes, which were laminated on PET substrates featuring an un-patterned ITO conductor as a *gate* electrode, and gravure printed insulator and semiconductor layers (Fig. 1). Electrical properties of the laminated double *gate* structure were characterized with *gate* connected either to the bottom ITO electrode or to the top electrode (conductive *n-doped* silicon wafer) (Fig. 1). Results were compared respectively to reference devices, which did not utilize the lamination step.

The next step was to replace the rigid silicon wafer with a flexible PET substrate with lithographically patterned *source* and *drain* electrodes (Fig. 2a). Final version of the laminated structure was made by exchanging the ITO coating with a patterned gold electrode which exhibited the additional advantage of being less fragile in the lamination process (Fig. 2b).

After studying the lamination techniques with single transistors, demonstrator inverters and ring oscillators were constructed using two flexible PET substrates. On the first substrate the gate electrode, dielectric layers, and the semiconducting layer were deposited. The second substrate with source-drain electrodes was laminated on top of the semiconductor. The threshold voltage of the transistor was different for PVP:PMF cross linked dielectric and PMMA/PMSSQ dielectric double layer. This is exploited [25,26] in the inverter design, and a working 3-stage ring oscillator is demonstrated. The load and drive transistors in the inverter stages had 1:20 *channel width* ratio. The *channel length* was 15 µm for both

transistors.

In addition to the electrode layer lamination, also the lamination of the semiconductor and dielectric layer interface was studied. The electrodes and the semiconductor were deposited on one substrate and the gate electrode and dielectric on another. Lamination of the dry layers eliminates the requirement of orthogonal solvents for the two printed layers. Demonstration transistors were constructed with combination of laser patterned *source-drain* electrodes.

2.3 Laser Ablation

High definition laser patterning by ablation [13], [27-29] of thin gold films was studied by using three different lasers on four substrates PET, PEN *(poly(ethylene naphthalate))*, PI *polyimide* and glass. Picosecond pulse lasers from *Lumera* (ultraviolet (UV) 355 nm and infrared (IR) 1064 nm wavelengths), and a femtosecond pulse laser from *Quantronix* (800 nm wavelength) were used in this study. Transmittance spectrum (Fig. 3) of the substrates was measured with an *Avaspec 2048 spectrophotometer*. The laser ablation of a thin metal film does not work properly on substrates that absorb the laser wavelength, as this will cause melting of the substrate surface. PET and glass were transparent at all used wavelengths while PEN was not transparent at the available UV wavelength. Polyimide absorbed strongly all used wavelengths of the laser light. Substrates were chosen for the laser processing accordingly.

Typical drawbacks of a laser ablation process are pattern edge roughness (both in-plane linearity and protruding metal spikes), substrate deformation and residue of the patterned material [27]. In order to minimize them different processing conditions and parameters were tried. Laser power, pulse repetition rate, and scanning speed were varied, and an optimal parameter range was found. Processing in vacuum was also explored, but with only marginal enhancement of the quality. The effect of a protective resist that could be removed after the ablation process was studied. However, there was no change in ablation edge quality, but the resist layer was useful for removing the small amount of ablation residue that is spread around the processed patterns.

Laser ablation of the gold film was achieved with reasonable quality with all three lasers, as long as the substrate was chosen properly. The marginally best edge quality (on flexible substrate) was achieved with the UV picosecond pulse laser on a PET substrate, and was therefore chosen for the demonstration of the electrode processing.

2.4 Roll-to-roll Compatible Transistor Process Details

After lamination tests with lithographically patterned or shadow mask evaporated electrodes, the following roll-to-roll compatible lamination process was developed (Fig. 2b). Initial gold structures (40 nm) were evaporated on PET substrates through a shadow mask, forming the *gate* electrode on one substrate and the basis for the *source* and *drain* electrodes on the other. This metal deposition without high precision structures could be

done for example by the technique showed by Lo et. al.[30]. In that article, also the overall lamination concept is shown, where in the end the two separately processed substrates are laminated together. In this work the channel separating the *source* and *drain* was formed by laser ablation. The UV laser beam was scanned at 200 mm/s with pulse frequency of 50 kHz and pulse power of 15 mW. With the chosen optics, the laser beam was focused to a spot with about 15 µm diameter. The final ablation patterned transistor channel length (L) was 16 µm. The formed interdigitated finger electrodes defined a very wide (W) transistor channel of 145 mm (Fig. 4). Laser ablation, as well as all the remaining processing steps of the transistor preparation including the conjugated polymer printing, was done under normal laboratory conditions.

The quality of the laser ablated channel was acceptable for transistor use (Fig. 4-6). Channel edge defects associated with ablation methods were kept at minimum. The edges were protruding upwards at some places, preventing the use of very thin dielectric layers. The maximum peaks were less than 200 nm high.

The semiconductor material was dissolved in toluene and filtered through 1 µm syringe filter. 1.6% solution was spin cast on the *source-drain substrate* at 2000 rpm for 1 minute. PMMA dielectric was dissolved in 2:1 mixture of toluene and EDGA. The solution with a concentration of 16.6% was spin coated on the *gate substrate* at 8000 rpm for 1 minute. Both films were dried gradually to 100°C. Semiconductor thickness was ca. 100 nm and dielectric thickness was 2.5 µm in this test. Thinner layers could be possible also.

Lamination took place on a hotplate at 160 °C. The *source-drain* substrate and the *gate* substrate were placed on top of each other, with the electrodes aligned properly (Fig. 2b). When pressure and heat were applied, the dielectric and semiconductor films were laminated together. A 10 kg weight was used on top of the sample, giving rise to an estimated pressure of 40 kN/m^2. After 15 minutes of heating under the pressure the sample was cooled and some glue was deposited on the edges of the two substrates, fixing them together. Faster lamination process was not tested, but should be possible.

2.5 Measurements

The quality of the laser ablation was studied with an optical microscope, a *Dektak 150 Stylus Profilometer*, a *NT-MDT Scanning Probe Microscope (AFM) in contact mode* and *a Leo 1430 Scanning Electron Microscope (SEM)* with 5 kV accelerating voltage. Storage (in dark) and measurement of the sample were done under normal room conditions without additional shielding. Transistor characteristics were measured with a *Keithley 4200-SCS Semiconductor Characterization System*. The sample was measured from time to time during a period of 3 years.

3. Results and Discussion

Current levels and mobilities of the laminated double *gate* OTFTs (see Fig. 1) were observed to be ca. 40-50 times higher than observed with reference samples having same

electrode geometry. This applies regardless of which *gate* electrode was used while the other *gate* electrode was floating.

The same performance enhancement was observed with the laminated electrodes on flexible substrate (Fig. 2a) when compared with electrodes made by thermal evaporation through a shadow mask (data not presented here). It is clear that the lamination process itself has an effect on the electrical properties most probably arisen from morphological changes in the semiconductor layer close to the semiconductor-dielectric interface. Higher mobility levels can be resultant from the enhanced π-π*- stacking and arisen conjugation level induced by heat and pressure in the lamination process [31].

The transistors made with PVP:PMF dielectric had a slightly negative (-10 V) threshold voltage, and they were used as *drive* transistors in the inverters. The *diode connected load* [32],[33] transistors were made with PMMA and PMSSQ double layer, which had a positive threshold voltage (+20 V). Tuning of the threshold voltage [34],[35] was achieved by depositing a thin PMSSQ layer on top of the PMMA layer. The threshold voltage was strongly dependent to the time of exposure to air. Also the lifetime of the transistors was low. Inverters made with the threshold tuned transistors worked with a maximum gain of 9.5 at 40 V supply voltage (Fig.7). A three stage ring oscillator was constructed using the inverters. The oscillation peak-to-peak amplitude was 6 V and frequency was 31 Hz at 45 V supply voltage.

The scanning laser patterning process for the electrodes, the solution processing of the semiconductor and dielectric layers, and the device assembly by lamination of flexible substrates are all roll-to-roll compatible methods and allow for fast and low cost device fabrication. Finally we demonstrate a fully roll-to-roll compatible laminated transistor. The results show good transistor behavior with enhanced mobility and lifetime in air. Figures 8-10 show the characteristics of a laminated transistor after 3 years storing in air in a dark laboratory cupboard. The plots for both transfer and output characteristics have overlapping forward and reverse sweeps, showing very little hysteresis which is indicative of a good interface between the dielectric and the semiconductor. The mobility and threshold voltage reached a quite stable long term value after an initial settling time, and there is little degradation after 3 years (Fig. 8-10). During the stable measuring period (34 months) the mobility was 0.082 ±0.005 cm^2/Vs, threshold voltage -3 ±0.3 V, On/Off ratio 700 ±300 and subthreshold slope S 4.5 ±0.4 V/dec. The variance in the values is due to changes in measuring environment and conditions [36]. The measurements made during the winter months in dry conditions show decrease in mobility but increase in On/Off ratio (Fig. 10) which is contributed to a sensitivity to humidity common in conjugated polymers. The change in two months was as much as 7 % in mobility and 80 % in On/Off ratio when the relative humidity (RH) changed from rainy season (38 % RH) to a dry winter season (13 % RH). The devices were measured only occasionally with a few months intervals. Thus, stress data for the OTFT is missing and would have required a different experimental setup.The lifetime enhancement was evident in this case when compared to the transistors in the inverter demonstrator, or spin coated references. The degradation of the

semiconductor caused by the environment must be dependent on the way the semiconducting active layer is organized and formed in the dielectric interface. So it is dependent both on the material combination and the processing method. This is why shearing forces in printing or lamination can have a positive effect on overall performance as well as the lifetime of the whole device.

The bond between the polymer layers was not very strong, so the sheets were easily delaminated if a differential force was applied to the substrates. That is understandable, when considering the thin layers and the form of the attachment. The polymers are not melted together (which would make the bond stronger but intermixed), but the bond forms between two separate flat thin layers of polymers of different type. In order to minimize the mechanical stress on the sample and the risk of delamination, extra glue on the edges was used to keep the laminated structure intact. In a real roll-to-roll lamination process the glue material should be deposited between the sheets in the open areas, but keeping in mind that the thickness should be similar to other layers in order not to disturb the active area contact. However, this is a practical matter only to do with the actual manufacturing process of a real circuit and should be solved differently for different products and systems. Thinner laminated substrates are preferable, as the mechanical stress due to bending forces is comparably smaller.

The choice of the active transistor materials is very important. Polymer semiconductors might not withstand the temperature needed for lamination, and the proper attachment is achieved only with compatible materials. Especially in a configuration where the lamination interface is the active transistor interface, the performance is highly sensitive to any morphological changes that are induced by the lamination process.

4. Conclusions

The main advantage of the lamination technique is the possibility to use two pre-patterned substrates or the use of two materials which have incompatible solvents. The shearing forces in the lamination process can have a positive effect on the organizing of the active layer in thin film transistor, enhancing performance and lifetime. Laser ablation was tested as possible processing method for high definition patterning. The techniques reported here add to the many mass production possibilities already available in the field and may provide a crucial advantage for device performance and manufacturing efficiency for certain material combinations and transistor based application.

References

[1] P. Kopola, M. Tuomikoski, R. Suhonen, A. Maaninen, Gravure printed organic light emitting diodes for lighting applications, Thin Solid Films 517 (2009) 5757-5762.

[2] P. Kopola, T. Aernouts, S. Guillerez, H. Jin, M. Tuomikoski, A. Maaninen, J. Hast, High efficient plastic solar cells fabricated with a high-throughput gravure printing method, Sol. Energy Mater. Sol. Cells 94 (2010) 1673-1680.

[3] J. Kukkola, E. Jansson, A. Popov, J. Lappalainen, J. Mäklin, N. Halonen, G. Tóth, A. Shchukarev, J.-P. Mikkola, H. Jantunen, K. Kordas, Hast, T. Hassinen, A. Sunnari, K. Jokinen, H. Haverinen, R. Sliz, G. Jabbour, T. Fabritius, R. Myllylä, A. Vasiliev, N. Zaretskiy, Novel printed nanostructured gas sensor, Procedia Eng. 25 (2011) 896-899.

[4] S.M. Sze, K.K. Ng, Physics of Semiconductor Devices, Wiley-interscience, Hoboken, 2006.

[5] G. Horowitz, Organic semiconductors for new electronic devices, Adv. Mater. 2 (1990) 287-292.

[6] G. Horowitz, Organic thin film transistors: From theory to real devices, Adv. Mater. 10 (1998) 365-377.

[7] G. Horowitz, Organic thin film transistors: From theory to real devices, J. Mater. Res. 19 (2004) 1946-1962.

[8] M. Hambsch, K. Reuter, M. Stanel, G. Schmidt, H. Kempa, U. Fügmann, U. Hahn, A. Hübler, Uniformity of fully gravure printed organic field-effect transistors, Mater. Sci. Eng., B 170 (2010) 93-98.

[9] B. Michel, A. Bernard, A. Bietsch, E. Delamarche, M. Geissler, D. Juncker, H. Kind, J.-P. Renault, H. Rothuizen, H. Schmid, P. Schmidt-Winkel, R. Stutz, H. Wolf, Printing meets lithography: soft approaches to high-resolution patterning , IBM J. Res. Dev. 45 (2001) 697-719.

[10] S. Steudel, K. Myny, S. Schols, P. Vicca, S. Smout, A. Tripathi, B. van der Putten, J.-L. van der Steen, M. van Neer, F. Schütze, O. Hild, E. van Veenendaal, P. van Lieshout, M. van Mil, J. Genoe, G. Gelinck, P. Heremans, Design and realization of a flexible QQVGA AMOLED display with organic TFTs, Org. Electron. 13 (2012) 1729-1735.

[11] F.C. Krebs, T. Tromholt, M. Jørgensen, Upscaling of polymer solar cell fabrication using full roll-to-roll processing, Nanoscale 2 (2010) 873-886.

[12] J.H. Lee, G.H. Kim, S.H. Kim, S.C. Lim, Y.S. Yang, J.H. Youk, J. Jang, T. Zyung, Longevity enhancement of organic thin-film transistors by using a facile laminating passivation method, Synth. Met. 143 (2004) 21-23.

[13] E. Menard, M.A. Meitl, Y. Sun, J.-U. Park, D.J.-L. Shir, Y.-S. Nam, S. Jeon, J.A. Rogers, Micro-and nanopatterning techniques for organic electronic and

optoelectronic systems, Chem. Rev. 107 (2007) 1117-1160.

[14] A. Tunnell, D. Hines, E. Gomar-Nadal, E. Williams, Printing-induced improvements of organic thin-film transistors, Org. Electron. 9 (2008) 507-514.

[15] M. Ling, Z. Bao, D. Li, Transistor performance of top rough surface of pentacene measured by laminated double insulated-gate supported on a poly (dimethylsiloxanes) base structure, Appl. Phys. Lett. 88 (2006) 033502-033502.

[16] M.L. Chabinyc, A. Salleo, Y. Wu, P. Liu, B.S. Ong, M. Heeney, I. McCulloch, Lamination method for the study of interfaces in polymeric thin film transistors, J. Am. Chem. Soc. 126 (2004) 13928-13929.

[17] Y.-L. Loo, T. Someya, K.W. Baldwin, Z. Bao, P. Ho, A. Dodabalapur, H.E. Katz, J.A. Rogers, Soft, conformable electrical contacts for organic semiconductors: High-resolution plastic circuits by lamination, Proc. Nat. Acad. Sci. 99 (2002) 10252-10256.

[18] J. Zaumseil, K.W. Baldwin, J.A. Rogers, Contact resistance in organic transistors that use source and drain electrodes formed by soft contact lamination, J. Appl. Phys. 93 (2003) 6117-6124.

[19] S. Haas, Y. Takahashi, K. Takimiya, T. Hasegawa, High-performance dinaphtho-thieno-thiophene single crystal field-effect transistors, Appl. Phys. Lett. 95 (2009) 022111.

[20] F. Li, A. Nathan, Y. Wu, B.S. Ong, Organic Thin Film Transistor Integration, Wiley-VCH, Weinheim, 2011.

[21] X. Zhang, L.J. Richter, D.M. DeLongchamp, R.J. Kline, M.R. Hammond, I. McCulloch, M. Heeney, R.S. Ashraf, J.N. Smith, T.D. Anthopoulos, B. Schroeder, Y. Geerts, D. Fischer, M. Toney, Molecular packing of high-mobility diketo pyrrolo-pyrrole polymer semiconductors with branched alkyl side chains, J. Am. Chem. Soc. 133 (2011) 15073-15084.

[22] J.H. Oh, W.-Y. Lee, T. Noe, W.-C. Chen, M. Könemann, Z. Bao, Solution-shear-processed quaterrylene diimide thin-film transistors prepared by pressure-assisted thermal cleavage of swallow tails, J. Am..Chem. Soc. 133 (2011) 4204-4207.

[23] G. Giri, E. Verploegen, S.C. Mannsfeld, S. Atahan-Evrenk, S.Y. Lee, H.A. Becerril, A. Aspuru-Guzik, M.F. Toney, Z. Bao, Tuning charge transport in solution-sheared organic semiconductors using lattice strain, Nature 480 (2011) 504-508.

[24] W.-Y. Lee, J.H. Oh, S.-L. Suraru, W.-C. Chen, F. Würthner, Z. Bao, High-Mobility Air-Stable Solution-Shear-Processed n-Channel Organic Transistors Based on Core-Chlorinated Naphthalene Diimides, Adv. Func. Mater. 21 (2011) 4173-4181.

[25] L. Kergoat, L. Herlogsson, B. Piro, M.C. Pham, G. Horowitz, X. Crispin, M. Berggren, Tuning the threshold voltage in electrolyte-gated organic field-effect transistors, Proc. Nat. Acad. Sci. 109 (2012) 8394-8399.

[26] C. Huang, H.E. Katz, J.E. West, Solution-processed organic field-effect transistors and unipolar inverters using self-assembled interface dipoles on gate dielectrics, Langmuir 23 (2007) 13223-13231.

[27] C. Momma, B.N. Chichkov, S. Nolte, F. von Alvensleben, A. Tünnermann, H. Welling, B. Wellegehausen, Short-pulse laser ablation of solid targets, Opt. Commun. 129 (1996) 134-142.

[28] M.C. Gower, Industrial applications of laser micromachining, Opt. Express 7 (2000) 56-67.

[29] D. Kim, S. Jeong, J. Moon, S. Han, J. Chung, Organic thin film transistors with ink-jet printed metal nanoparticle electrodes of a reduced channel length by laser ablation, Appl.Phys. Lett. 91 (2007) 071114-071114.

[30] C.-Y. Lo, J. Hiitola-Keinänen, O.-H. Huttunen, J. Petäjä, J. Hast, A. Maaninen, H. Kopola, H. Fujita, H. Toshiyoshi, Novel roll-to-roll lift-off patterned active-matrix display on flexible polymer substrate, Microelectron. Eng. 86 (2009) 979-983.

[31] R.D. McCullough, R.D. Lowe, M. Jayaraman, D.L. Anderson, Design, synthesis, and control of conducting polymer architectures: structurally homogeneous poly (3-alkylthiophenes), J. Org. Chem. 58 (1993) 904-912.

[32] Y. Yun, C. Pearson, M. Petty, Circuits, Bootstrapped inverter using a pentacene thin-film transistor with a poly (methyl methacrylate) gate dielectric, IET Circuits Devices Syst. 3 (2009) 182-186.

[33] T. Hassinen, H.G. Sandberg, Gravure printed low voltage polymer transistors and inverters, Thin Solid Films 548 (2013) 585-589.

[34] A. Wang, I. Kymissis, V. Bulovic, A.I. Akinwande, Engineering density of semiconductor-dielectric interface states to modulate threshold voltage in OFETs, IEEE Trans. Electron Devices, 53 (2006) 9-13.

[35] C. Huang, J.E. West, H.E. Katz, Organic Field-Effect Transistors and Unipolar Logic Gates on Charged Electrets from Spin-On

Organosilsesquioxane Resins, Adv. Funct. Mater. 17 (2007) 142-153.

[36] H. Yan, Z. Chen, Y. Zheng, C. Newman, J.R. Quinn, F. Dötz, M. Kastler, A. Facchetti, A high-mobility electron-transporting polymer for printed transistors, Nature 457 (2009) 679-686.

FIGURES

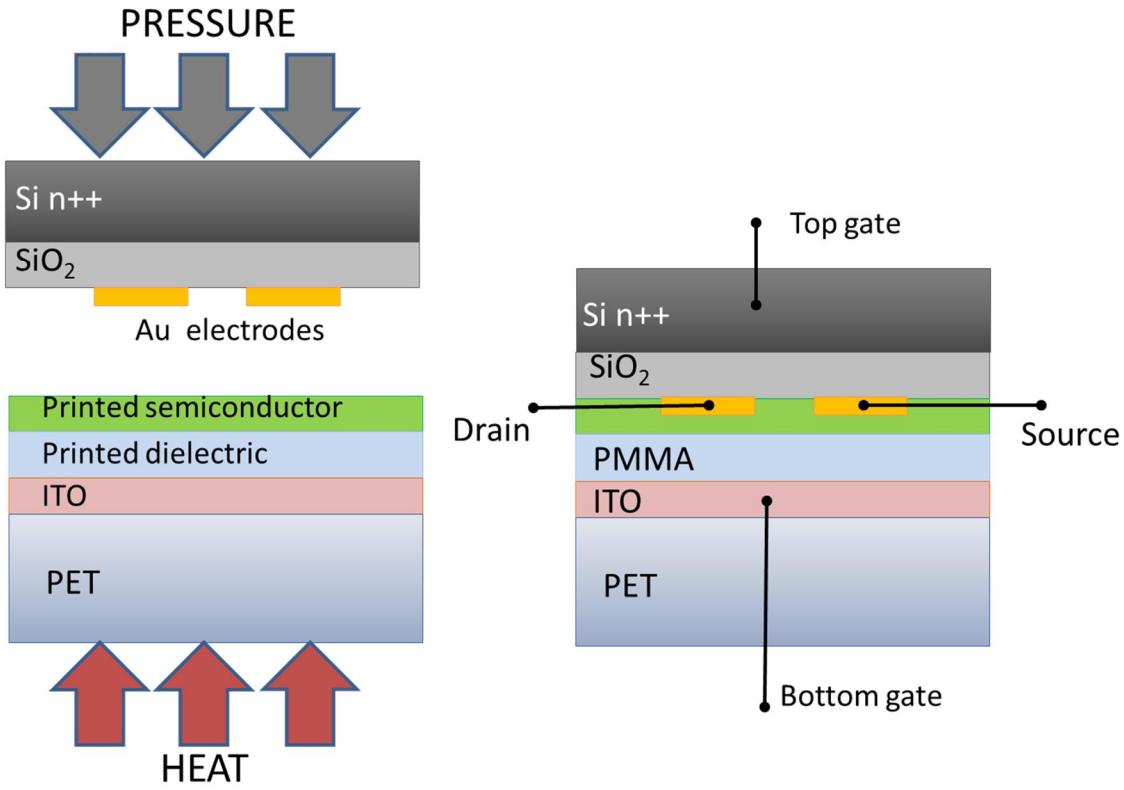

Fig. 1. Schematic picture of the double gate transistor layers and lamination process (left), and double gate transistor electrode configuration (right).

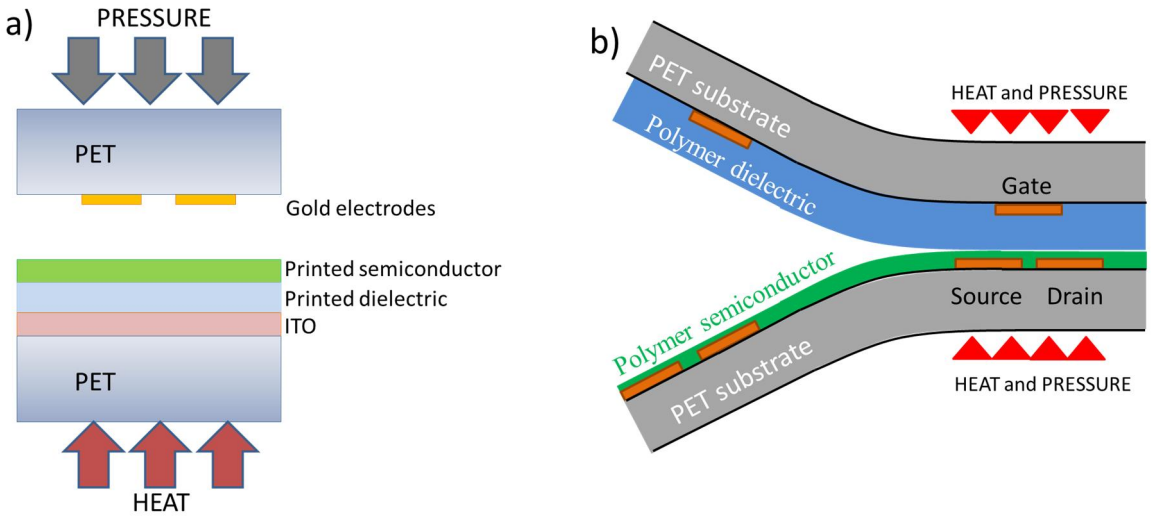

Fig. 2. Schematic pictures of the two different lamination processes. a) PET foil with well-defined source-drain electrodes is laminated on the ITO-PET substrate containing printed polymer layers. b) Two flexible PET foils both containing metal electrodes and a polymer layer are laminated together.

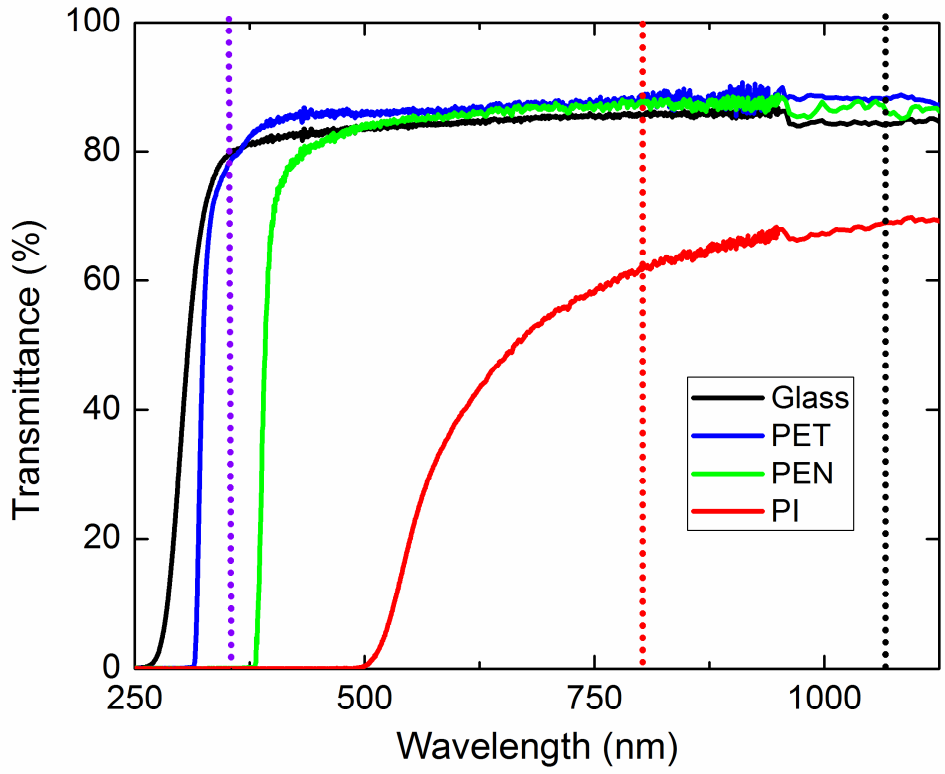

Fig. 3. Transmittance spectrum of the substrates used. The laser wavelengths 355 nm, 800 nm and 1064 nm are marked in the picture.

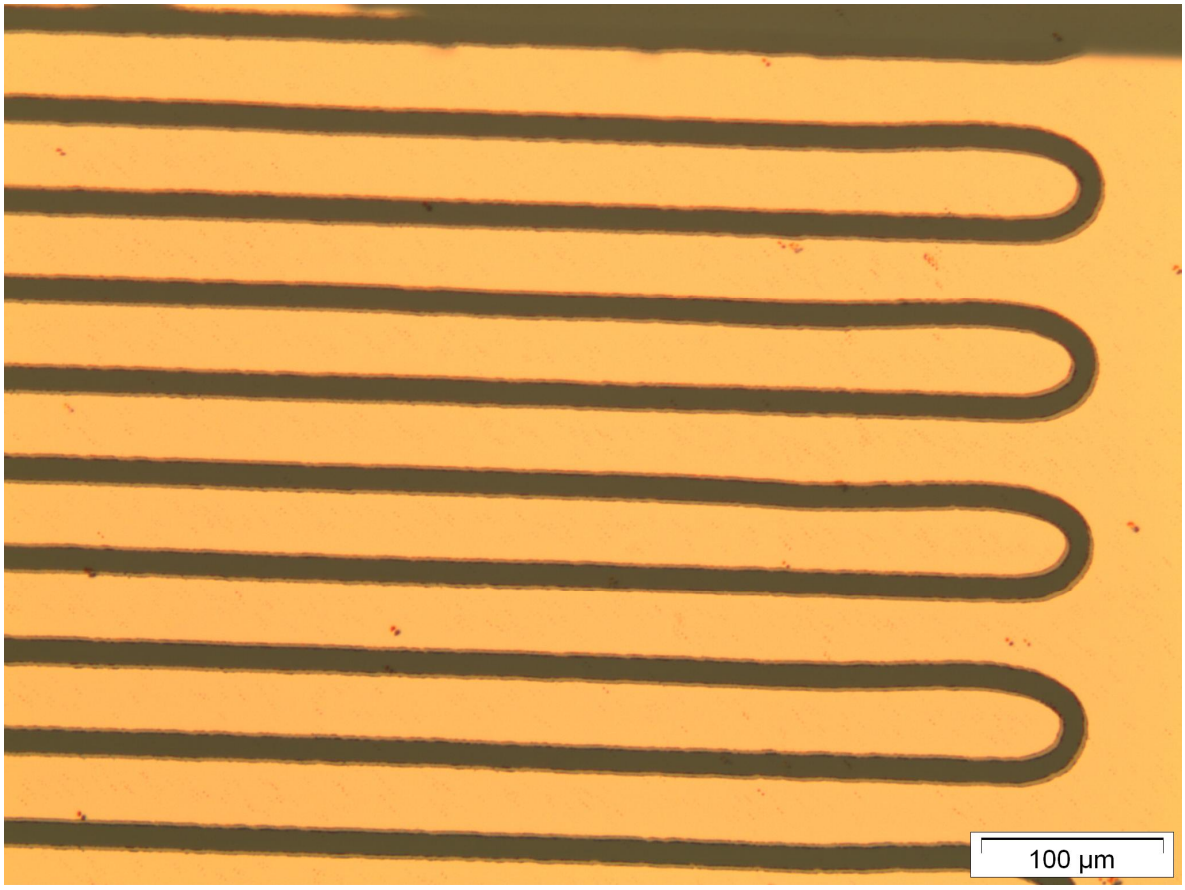

Fig. 4. Optical image of the transistor channel. The interdigitated electrodes were formed from a thin gold film by laser ablation.

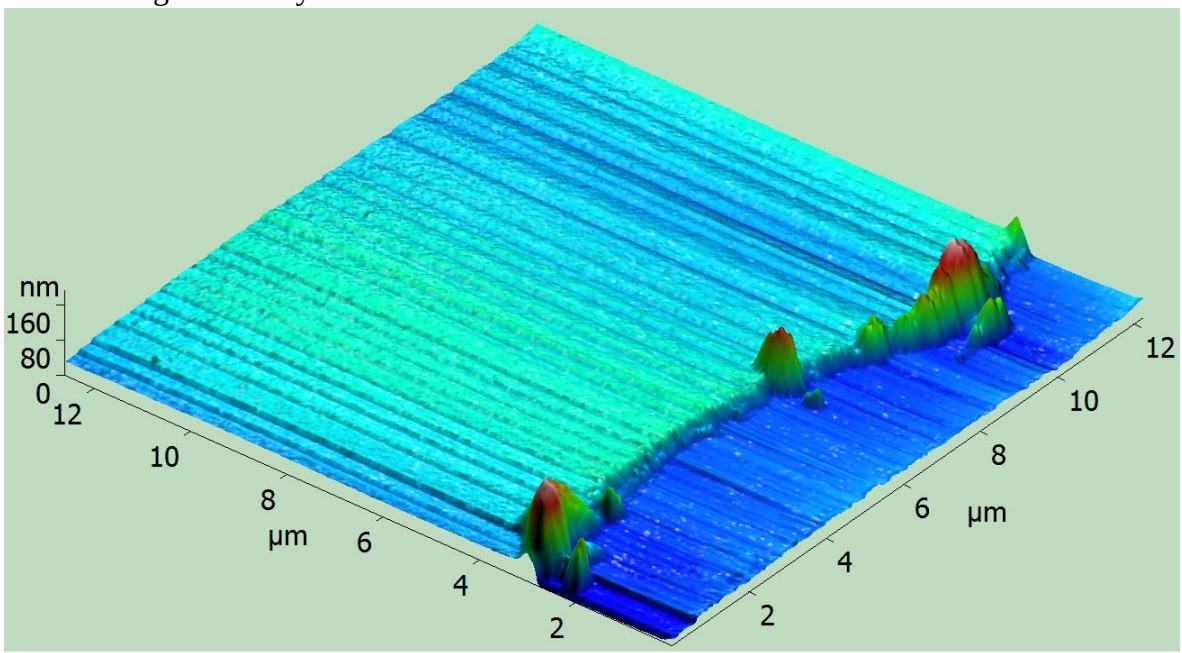

Fig. 5. AFM image shows how the laser ablation causes some small defects on the edge of the electrode. However, the typical peak height for protruding metal “spikes” was less than 200 nm.

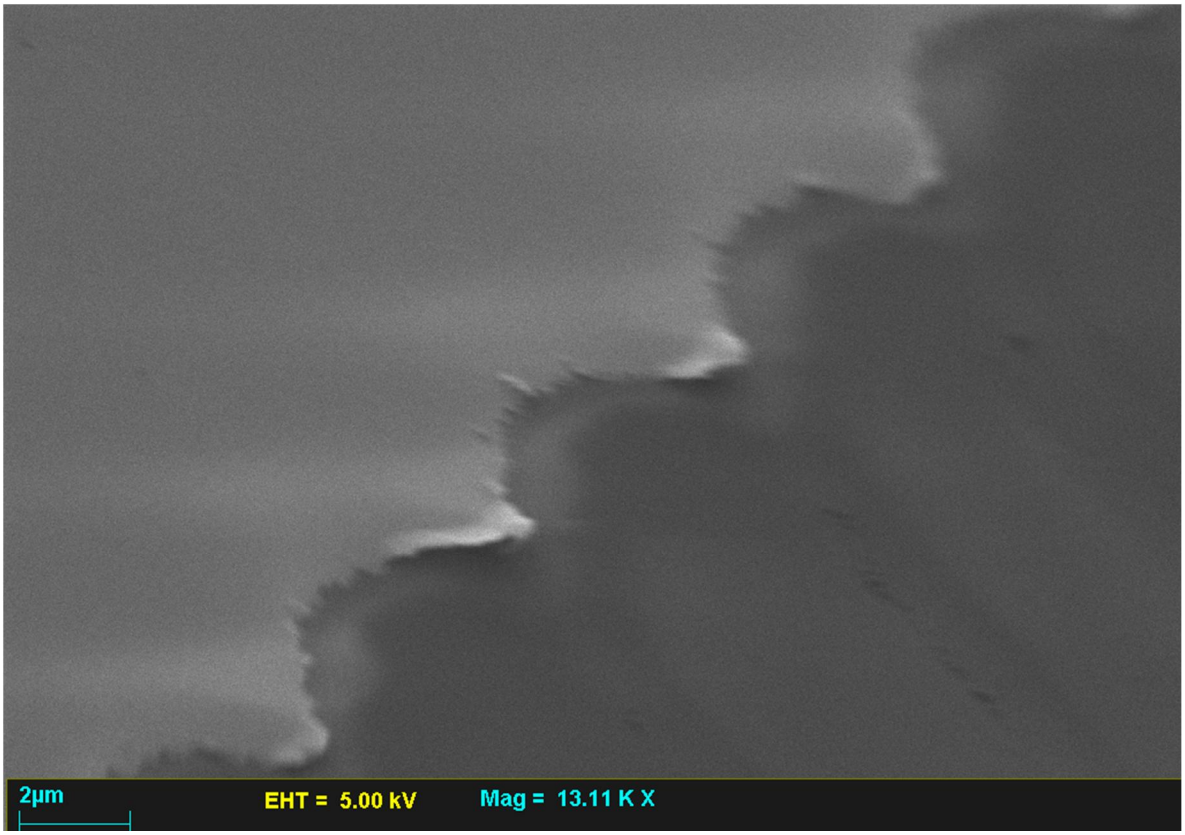

Fig. 6. Scanning Electron Microscope image of the laser ablated channel shows some of the typical edge defects. Without optimized parameters, the formed metal “saw tooth” patterns can delaminate from the substrate and bend upwards to form protruding “spikes”.

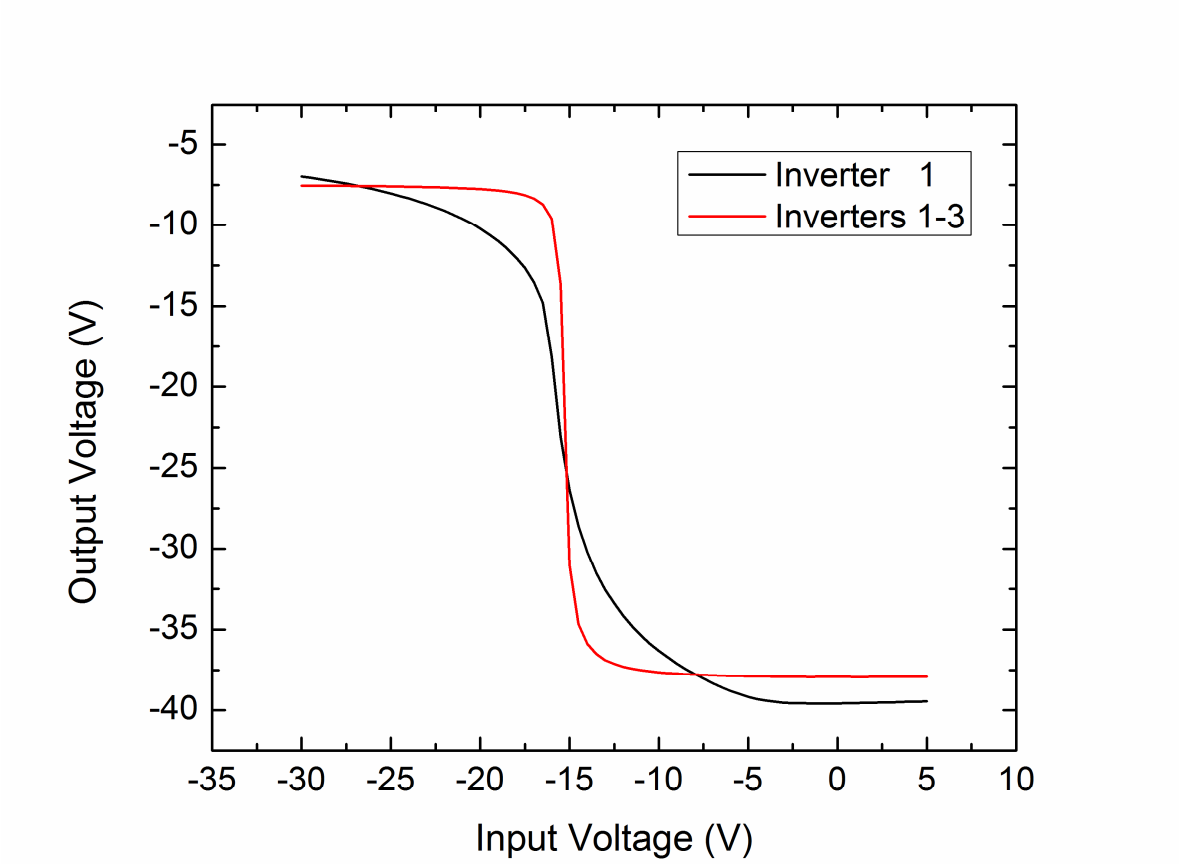

Fig. 7. Inverters made by lamination show symmetrical switching. One stage and 3 inverter stages connected together are shown.

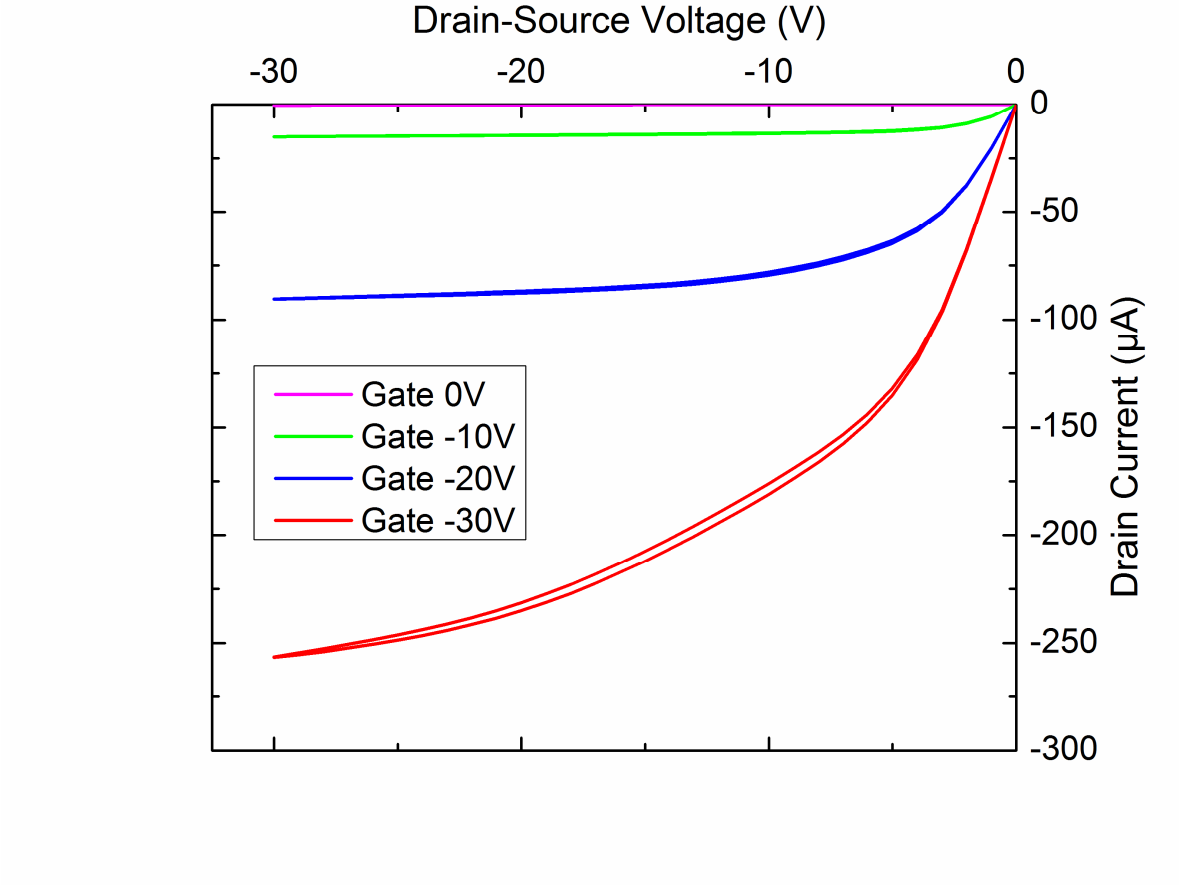

Fig. 8. An output curve of a laminated organic thin film transistor after 25 months in air.

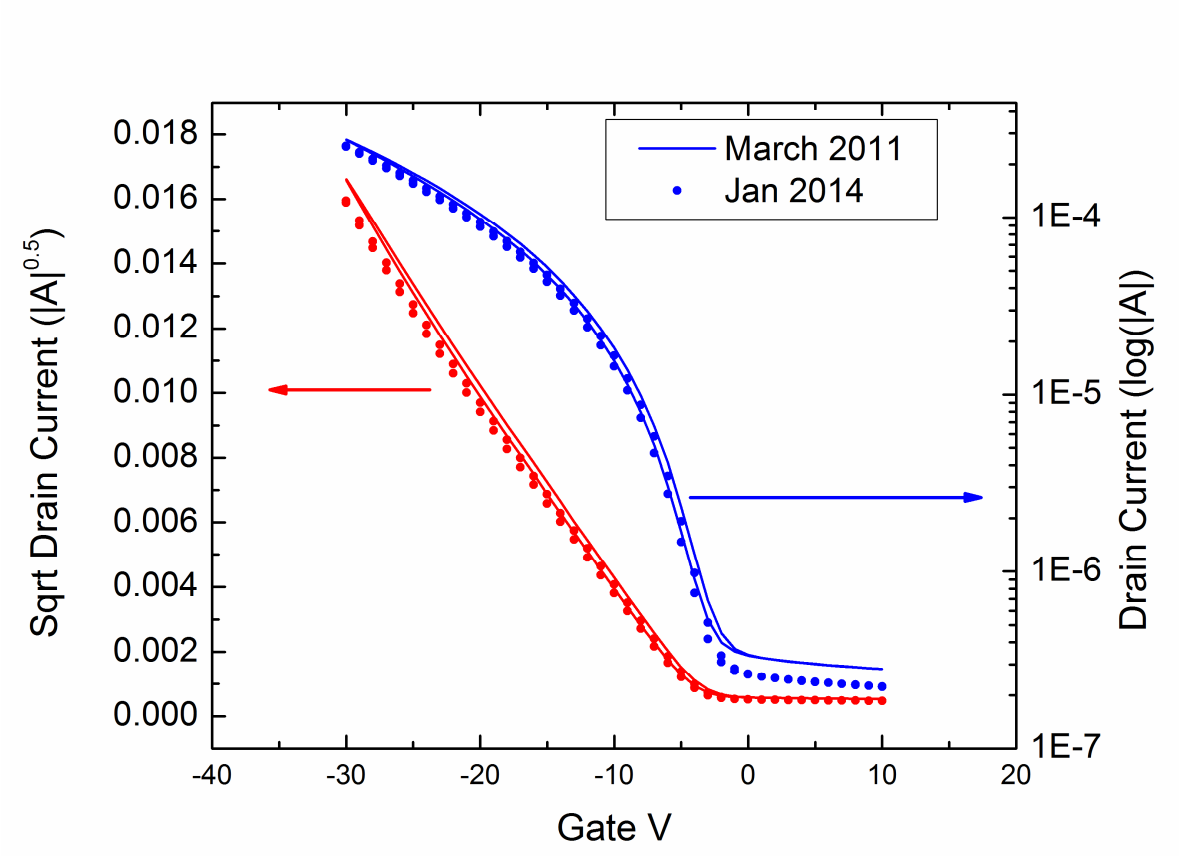

Fig. 9. Transistor transfer characteristics show little change after storing in air. Solid lines present the values measured after 3 months and symbols after 36 months.

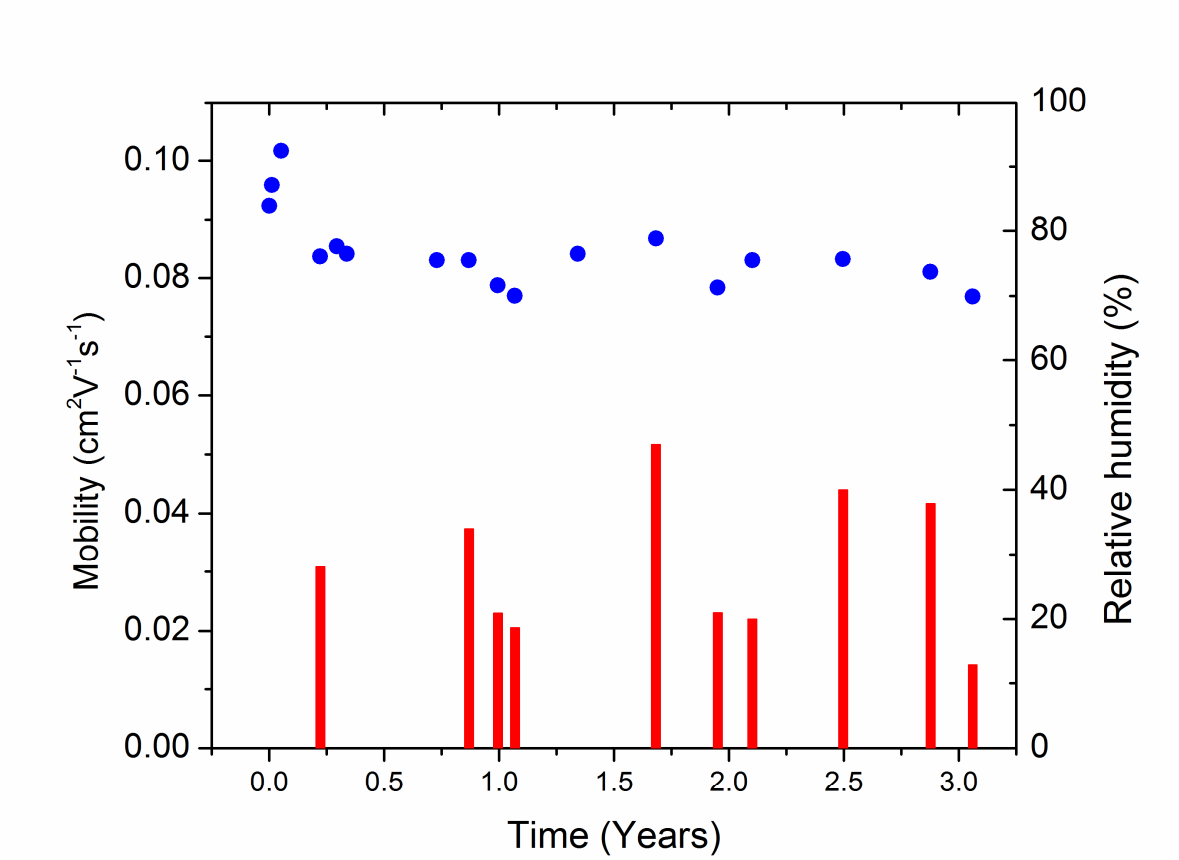

Fig. 10. Chart shows the transistor field effect mobility (dots) over a period of 36 months, and relative humidity values (bars). There is a dip in the values measured during the dry winter months.