# Extraction of Parasitic Resistances in GaAs MESFET's

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## *Abstract*

*In this paper analytical solutions for the parasitic resistances of MESFET are illustrated. Calculations are based on an extraction method presented by P. Debie, L. Martens and D. De Zutter. Due to analytical solutions no numerical iterations are needed. Resistor measurements show that the method is sensitive to the accuracy of the measured voltages. Repeatability can be increased by data processing the measured data.*

## 1. Introduction

Accurate and fast parameter extraction for modeling of MESFET's is important when designing and developing microwave circuits. The performance of both digital and analog/microwave FET's is degraded by parasitic resistances [1]. For example, transconductance, noise figure and power consumption are strongly affected by parasitic resistances.

There are several approaches proposed how to extract the parasitic resistances [2]-[4], most of them based on a combination of DC and small-signal parameters measured under certain special bias point. For wafer probing a fast and reproducible technique of determining the parasitic resistances is desired. For the extraction of these resistances an extraction method is presented in [5]. The method uses only three DC measurements from which three relations between the drain, source and gate resistances $R_D$, $R_S$ and $R_G$ are obtained. Equations are solved by a small iteration process to obtain accurate results for $R_D$, $R_S$ and $R_G$.

It is presented that the parasitic resistances can be calculated analytically from the three equations. Therefore, no iterations are required and the extraction method becomes faster and more reliable. When processing measured data further to reduce measurement noise more accurate results are received for parasitic resistances.

## 2. Analytically Solved Resistances

Fig. 1 shows a DC equivalent circuit model of a GaAs MESFET which is derived from the nonlinear Statz model available in SPICE3 [5]. The model is applied to cold-FET (Vds=0) situations. It includes the parasitic resistances $R_G$, $R_S$ and $R_D$, the diodes $D_{gd}$ and $D_{gs}$ representing

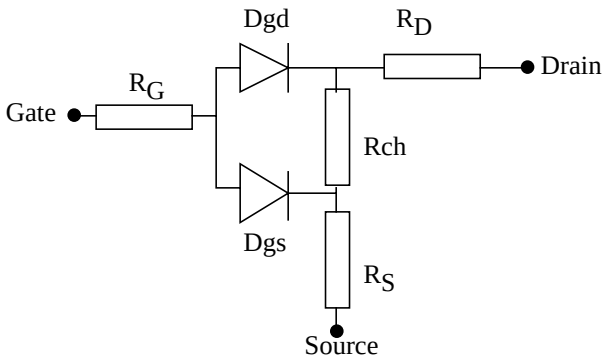


**Figure 1** *DC equivalent circuit of MESFET for cold-FET (Vds=0) applications.*

the gate-channel Schottky junction and the channel resistance $R_{ch}$. The diodes are assumed to be identical. Before the calculation of the parasitic resistances the junction saturation current IS and the ideality factor N of the Schottky diodes are determined according to [6]. The measurement system is presented in [5] and the received equations are:

$$R_d + \frac{2V_{d1}}{I_g} = R_s \qquad \text{(EQ 1)}$$

$$\frac{R_s}{2} + R_g = \frac{V_{g1} - nV_T \ln\left(1 + \frac{I_g}{2IS}\right)}{I_g} \qquad \text{(EQ 2)}$$

$$R_s + R_g = \frac{V_{g2} - nV_T \ln\left(\frac{2 + \frac{I_g}{IS}}{1 + e^{\frac{R_s I_g - V_{d2}}{nV_T}}}\right)}{I_g} \qquad \text{(EQ 3)}$$

The gate and drain voltages $V_{g1}$ and $V_{d1}$ are from the first measurement, $V_{g2}$ and $V_{d2}$ are from the second measurement and $I_g$ is the used current.

Eq. 2 and 3 are used to calculate the function $f(R_S)=0$ for Newton iteration purposes. When analysing $f(R_S)=0$ it is found out that there are two solutions for $R_S$. Fig. 2 shows the behaviour of $f(R_S)$ for a MESFET with the measured voltages $V_{g1}$, $V_{d1}$, $V_{g2}$ and $V_{d2}$ at $I_g$=47mA. Received values for $R_S$ are 3.45 Ω and 4.64Ω.

A disadvantage of Newton's method is that the iteration sequence may sometimes convergence to a solution different from the expected one [7]. Therefore, when using Newton iteration received values for $R_S$, $R_G$ and $R_D$ might vary rather much between different iteration times.

The aim of this work is to determine parasitic resistances without Newton iteration. This becomes possible because parasitic resistances can be calculated analytically from Eq. 1-3. In the analytical calculations two solutions for $R_S$ are obtained in Eq. 4.

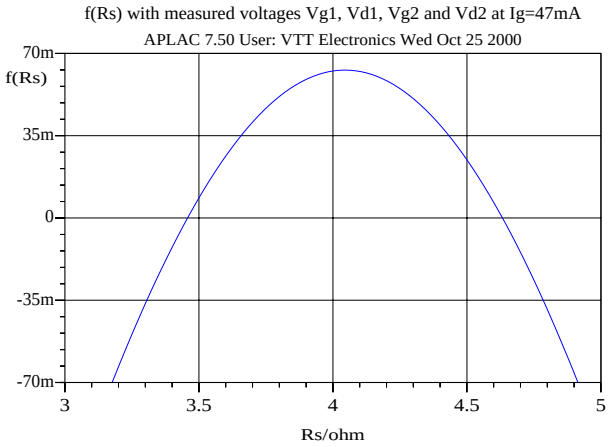


**Figure 2** *Function f(Rs) of a MESFET with measured voltages $V_{g1}$, $V_{d1}$, $V_{g2}$ and $V_{d2}$ at $I_g$=47mA.*

$$R_{S1/2} = 2\frac{nV_T}{I_g}\ln\left(0.5w_3 \pm 0.5\sqrt{w_3^2 - 4w_3}\right) + \frac{nV_T}{I_g}w_2 \qquad \text{(EQ 4)}$$

The parts $w_1$, $w_2$ and $w_3$ used in Eq. 4 are given as:

$$w_1 = \frac{V_{g1} - nV_T \ln\left(1 + \frac{I_g}{2IS}\right)}{I_g} \qquad \text{(EQ 5)}$$

$$w_2 = \frac{2Ig}{nV_T}\left(\frac{Vg2}{I_g} - \frac{nV_T}{I_g}\ln\left(2 + \frac{Ig}{IS}\right) - w_1\right) \qquad \text{(EQ 6)}$$

$$w_3 = \exp\left(\frac{V_{d2}}{nV_T} - w_2\right) \qquad \text{(EQ 7)}$$

Calculated solutions for $R_S$ have to fulfil the following conditions:

$$w_3 \geq 4 \qquad \text{(EQ 8)}$$

$$\frac{V_{d2}}{I_g} \geq R_{S1/2} \qquad \text{(EQ 9)}$$

One of the two solutions received for $R_S$ in Eq. 4 fulfils Eq. 8 and 9, which is shown to be:

$$R_S = 2\frac{nV_T}{I_g}\ln\left(0.5w_3 - 0.5\sqrt{w_3^2 - 4w_3}\right) + \frac{nV_T}{I_g}w_2 \qquad \text{(EQ 10)}$$

$R_G$ and $R_D$ are calculated from Eq. 1 and Eq. 2. There is only one solution for $R_S$, $R_G$ and $R_D$. This would not be necessarily the case if Newton iteration was used.

## 3. Measurement Results

The resistor measurement of a MESFET is performed by a DC parameter extractor implemented on top of APLAC circuit simulator and design tool [8]. The extractor controls the HP 4145A parameter analyser. The measurements are done with one on-chip MESFET transistor. In the following example W/L of the component is 1700µm/1µm. HP 11612A bias networks are used at the gate and drain nodes. The series resistance of bias networks $R_{bias}$ is 0.5Ω.

$R_S$ is sensitive to the accuracy of measured voltages, which can be seen in Eq. 4. Fig. 3 illustrates analytically calculated $R_S$ as a function of $I_g$ with and without function fittings to measured voltages $V_{g1}$, $V_{d1}$, $V_{g2}$ and $V_{d2}$. The first-order function is fitted to $V_{d1}$, $V_{d2}$ and to the measured function $w_2$ in Eq. 6. The second-order function is fitted to $V_{g2}$. It is obvious that the reduction of measurement noise increases the repeatability when several measurement are

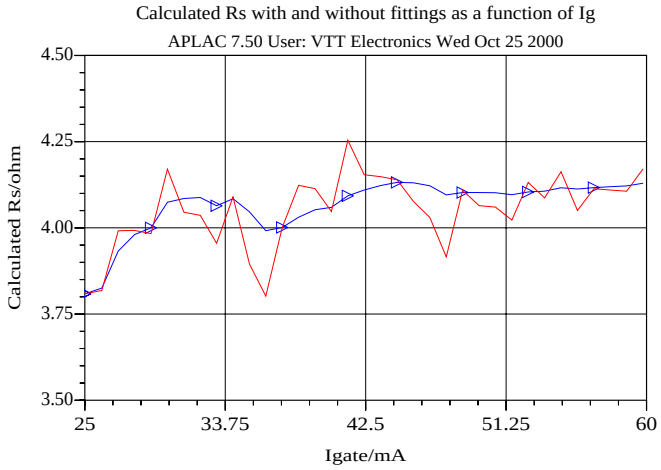


**Figure 3** *Analytically solved RS as a function of Ig with and without function fittings.*

performed. Statistics of 100 measurements seen in Tab. 1 confirms this. Analytical calculations are faster than Newton iterations. However, the data processing of the measured voltages for reducing the measurement noise does the analytical calculations slower.

**Table 1: Statistics of 100 Measurements**

| | Average | | | Standard Deviation | | |
|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 1 | 2 | 3 |
| $R_S$ | 4.105Ω | | 4.092Ω | 0.50% | | 0.19% |
| $R_D$ | 5.036Ω | | 5.027Ω | 0.50% | | 0.22% |
| $R_G$ | 3.126Ω | | 3.104Ω | 0.33% | | 0.11% |

1. Newton iteration
2. Analytical calculation
3. Analytical calculation with reduction of measurement noise

## 4. Conclusions

The parasitic resistances can be calculated analytically. Therefore, no iterations are needed. In this way possible problems with the iteration are avoided. For example, the iteration does not converge to the desired solution or the iteration does not find the solution at all. The analytical calculations are also faster than iterations.

The disadvantage of the method is the sensitivity to the measured voltages. The function fittings to the measured voltages are used to reduce the measurement noise. Thus the values of extracted parasitic resistances do not vary much when several measurements are performed. The advantage is also that the resolution of the measurement device does not have to be very high.

## 5. Acknowledgements

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## 6. References

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