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Abstract

This work reports on studies and the fabrication process development of micromechanical silicon-on-insulator (SOI) devices. SOI is a promising starting material for fabrication of single crystal silicon micromechanical devices and basis for monolithic integration of sensors and integrated circuits. The buried oxide layer of an SOI wafer offers an excellent etch stop layer for silicon etching and sacrificial layer for fabrication of capacitive sensors. Deep silicon etching is studied and the aspect ratio dependency of the etch rate and loading effects are described and modeled. The etch rate of the deep silicon etching process is modeled with a simple flow conductance model, which takes into account only the initial etch rate and reaction probability and flow resistance of the etched feature. The used model predicts qualitatively the aspect-ratio-dependent etch rate for varying trench widths and rectangular shapes. The design related loading can be modeled and the effects of the loading can be minimized with proper etch mask design.

The basic SOI micromechanics process is described and the drawbacks and limitations of the process are discussed. Improvements to the process are introduced as well as IR microscopy as a new method to inspect the sacrificial etch length of the SOI structure.

A new fabrication process for SOI micromechanics has been developed that alleviates metallization problems during the wet etching of the sacrificial layer. The process is based on forming closed cavities under the structure layer of SOI with the help of a semi-permeable polysilicon film.

Prototype SOI device fabrication results are presented. High Q single crystal silicon micro resonators have potential for replacing bulky quartz resonators in clock circuits. Monolithic integration of micromechanical devices and an integrated circuit has been demonstrated with the developed process using the embedded vacuum cavities.

Preface

This dissertation is a result of experimental work carried out during 1997–2004 at VTT´s Microelectronics research field. The work summarizes the results of numerous projects involving SOI device process development. MEMS is an emerging technology that promises to bring about exiting applications, ambient intelligence, sensor networks providing a wealth of useful information, new medical solutions, long life, happiness and prosperity to all mankind. This presentation is my two-cents worth on that topic.

Many people have helped and instructed me over the years and have made the writing of this text possible. I shall try to list them here – not in any particular order – and some may well have slipped through the gap. They are no less important. To those at VTT Microelectronics: A. Lehto, H. Kattelus, J. Heleskivi, I. Suni, P. Kuivalainen, S. Franssila, M. Blomberg, A. Torkkeli, P. Seppälä, J. Karttunen, P. Pekko, J. Dekker, J. Saarilahti, H. Ronkainen, S. Eränen, T. Vehmas, H. Ritala, K. Henttinen, T. Suni, A. Häärä, T. Häkkinen, K. Järvi, R. Lindman, T. Visti, T. Virolainen, M. Markkanen; to those at the VTT Microsensing research field: H. Seppä, A. Oja, T. Mattila, T. Sillanpää, V. Kaajakari; and to those among our industrial partners and customers: H. Kuisma, J. Ruohio, T. Ryhänen, V. Ermolov, J. Mäkinen, M. Tilli, K. Thequist – Thank You all!

I am grateful to Dr. Risto Mutikainen and Prof. Klas Hjort for their pre-examination of the thesis and their valuable comments. I am also thankful to the opponent, Dr. Robert Aigner, for agreeing to examine the thesis. Mrs. Adelaide Lönnberg did an excellent job checking the language of this thesis and making it readable.

Many thanks to my parents. Two other people deserve special appreciation, first my wife Niina for putting up with me for so many years and my dear son Simo-Pekka. And for weird completeness, I want to add a four-footed friend to my list: Piki, the small energetic Westie-lad, for being such a delightful creature.

Finally, I wish to thank everybody who feels entitled to or finds use for my gratitude.

Jyrki Kiihamäki, Helsinki, March 2005.

List of publications

This work is based on the following original publications, which are referred to in the text by their Roman numerals. In addition, some previously unpublished results and results presented in our other related publications [Refs. 56, 62, 79, 83, 96, 102, 113, 117, 118, 121] are included in the text to give the reader a broader perspective of the work.

Paper I   Kiihamäki, J. Deceleration of silicon etch rate at high aspect ratios. J. Vac. Sci. Technol. A, Vol. 18, No. 4, (2000), pp. 1385–1389.

Paper II   Karttunen, J., Kiihamäki, J., Franssila, S. Loading effects in deep silicon etching. Proc. SPIE, Vol. 4174, (2000), pp. 90–97.

Paper III   Kiihamäki, J. Measurement of oxide etch rate of SOI structure using near IR microscopy. Physica Scripta, Vol. T101, (2002), pp. 185–187.

Paper IV   Kaajakari, V., Mattila, T., Oja, A., Kiihamäki, J., Seppä, H. Square-extensional mode single-crystal silicon micromechanical resonator for low-phase-noise oscillator applications. IEEE Electron Device Letters, Vol. 25, No. 4, (2004), pp. 173–175.

Paper V   Kiihamäki, J., Dekker, J., Pekko, P., Kattelus, H., Sillanpää, T., Mattila, T. 'Plug-Up' – A new concept for fabricating SOI MEMS devices. Microsystem Technologies, Vol. 10, No. 5, (2004), pp. 346–350.

Paper VI   Kiihamäki, J., Ronkainen, H., Pekko, P., Kattelus, H., Theqvist, K. Modular integration of CMOS and SOI-MEMS Using 'Plug-Up' concept. Digest of Technical Papers The 12th International Conference on Solid-State Sensors, Actuators and Microsystems, Vol. 2. Institute of Electrical and Electronics Engineers, (2003), pp. 1647–1650.

The author is the sole writer of articles I and III, and the primary author of articles V and VI. The author also made major contributions in the experiments, analysis and writing of paper II; the final mask layouts and the device fabrication process of paper IV were designed and supervised by the author.

Contents

Appendices

      Papers I–VI

List of used acronyms and symbols

AES	Acoustic emission sensor
ARDE	Aspect ratio dependent etching
BAW	Bulk acoustic wave
BESOI	Bonded-etched silicon on insulator
BOX	Buried oxide layer
CMOS	Complementary metal-oxide semiconductor
CMP	Chemical mechanical polishing
DRIE	Deep reactive ion etching
DSB	Direct silicon bonding
ECR	Electron cyclotron resonance
EDP	Ethylene diamine pyrocatechol, anisotropic silicon wet etchant
EEPROM	Electrically erasable programmable read-only memory
HARMST	High aspect ratio micro structure technology
HF	Hydrofluoric acid
IC	Integrated circuit
ICP	Inductively coupled plasma
IR	Infrared
KOH	Potassium hydroxide, anisotropic silicon wet etchant
LF	Low frequency
LPCVD	Low pressure chemical vapor deposition
MEMS	Microelectromechanical system
MOSFET	Metal oxide semiconductor field effect transistor
MST	Microsystem technology
NMOS	N-channel metal-oxide semiconductor (transistor)
PMOS	P-channel metal-oxide semiconductor (transistor)
RF	Radio frequency
RIE	Reactive ion etching
SCS	Single crystal silicon
SEM	Scanning electron microscope
SFB	Silicon fusion bonding
SIMOX	Separation by implantation of oxygen
SIRM	Scanning infrared microscopy

SOI	Silicon on insulator
TCR	Temperature coefficient of resistance
TMAH	Tetramethylammonium hydroxide, anisotropic silicon wet etchant
TXRF	Total X-ray reflection fluorescence
VLSI	Very large scale integration
A_w	Etchable area on the wafer
C_w	Work capacitance
D	Drive gap width
E	Young´s modulus
ER	Etch rate
f_r	Resonance frequency
G	Etchant generation rate
HFE	Forward current gain (a transistor model parameter)
K	Molecular flow transmission probability
k_e, k_m	Electrical and mechanical spring constants
L	Beam length
P	Pressure
R	Radius
S	Reaction probability
T	Film thickness
U_{DC}	Bias voltage
$\hat{u}_{ac}$	Drive voltage
V	Reactor volume
VTH	Threshold voltage (a transistor model parameter)
β	Proportionality factor to etching species
δ	Deflection
ν	Poisson ratio
ρ	Density of material
τ	Mean lifetime of active species
ω, ω_0	Angular frequencies

1. Introduction

1.1 Background

Integrated circuits made on single crystal silicon have revolutionized our way of life. Silicon chips have penetrated into every conceivable place and will probably continue to do so in the future. Besides its favorable electronic properties, over the past two to three decades silicon has become increasingly attractive as a mechanical material. Silicon is an abundant and inexpensive material that has excellent mechanical properties [1, 2]. Silicon process technology is well suited for making miniaturized devices, and patterning technologies are well developed. Features below 100 nm in size are routinely fabricated in modern integrated circuit (IC) fabs. The most important factor in the success of silicon microfabrication is that processes are mostly batch processes, which facilitates huge scaling benefits. What could be a cheaper man-made highly sophisticated object than an integrated circuit? Hundreds of millions of transistors are placed on a chip that costs only tens of Euros or less.

The mature mass fabrication technology for making integrated circuits has inspired engineers and scientists to seek out new applications for silicon that utilize its excellent mechanical properties, eventually introducing new functionality into silicon integrated circuits. A technological revolution similar to the one in which transistors were replaced by vacuum tubes can happen again with silicon micromechanics replacing bulky mechanical sensors and actuators. Miniaturization of mechanical devices can bring about unforeseen products and applications.

New applications include all kinds of sensors and actuators. The new microsystems technology (MST) or micro-electromechanical systems (MEMS) tries to add senses to the silicon chip's already existing brain – its computing power. The highest volume of micromechanical applications today are accelerometers for the automotive industry, light processors for data projectors, and inkjet printer heads. Commercial breakthroughs in medical and health care applications and wireless communication applications are eagerly awaited by industry.

1.2 Scope and objectives of the thesis

The common objective of all the projects that contribute to this thesis has been the development of silicon-on-insulator (SOI) micromachining technology, and gaining an understanding of the possibilities and limitations of this relatively new branch of micromechanics. As the thickness of bonded and etched SOI (BESOI) structure layers requires different etch tools and etch processes compared to what is common in the semi-conductor industry, significant effort is dedicated to deep silicon etching of SOI structures. Emphasis has been given to studying phenomena related to device layout design. The physics and chemistry of the etching process and etch process development have intentionally been given a secondary position.

Development and integration of device fabrication steps into processes, as well as fabrication of sample devices and prototypes, have been the most important aspect of the current work. All the devices processed during this work were micro-electromechanical; no fluidic or optical devices were fabricated, though this versatile fabrication technology could be adapted to those purposes also. The device operation was in all cases based on electrostatic actuation and capacitive readout. A schematic example of micromechanical SOI device is shown in Figure 1.
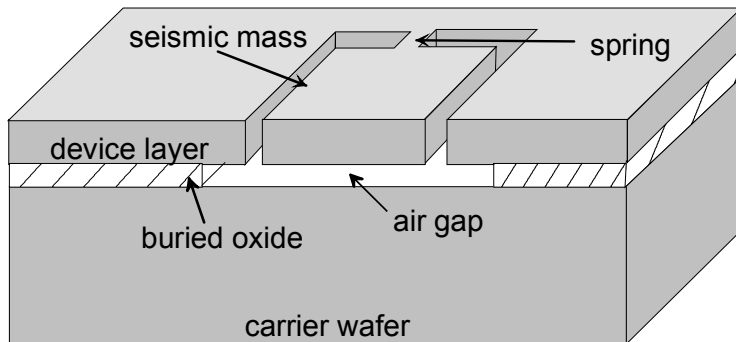

Figure 1. Example of a micromechanical SOI device.

Wafer bonding and pre-bond processing have been excluded from this work, which has concentrated on fabrication methods available in a conventional

integrated circuit fabrication environment. However, some analysis methods and MEMS-specific release and drying methods not used in IC fabrication are studied and applied when considered useful or necessary.

1.3 Facilities, equipment, and methods

This work was performed in the Microelectronics research field at VTT Information Technology. Full access to a clean room and integrated a circuit fabrication line were available throughout. The fabrication line consisted of complete equipment suitable for 0.6 micrometer gate-length CMOS circuits on 100 mm diameter silicon wafers. Lithography was done mainly with a I-line (365 nm wavelength) stepping aligner. Low-pressure chemical vapor deposition (LPCVD) processes and plasma etching processes for typical IC materials have been also available. Standard metrology and wafer level characterization methods available include optical microscopy, reflectometry and profilometry. Etch depths are measurements from cross-sections of cleaved or sawn samples by scanning electron microscope (SEM). Electrical measurements are performed at wafer level using a wafer probe station and standard semi-conductor parameter and impedance possible. In many cases measurements in vacuum are necessary, after which the devices are diced and wire-bonded.

Some analyses and measurements were performed by our colleagues in the VTT Microsensing research field, or in various laboratories of Helsinki University of Technology.

1.4 Summary of papers

This thesis includes six publications dealing with topics relevant to development of SOI micromechanics fabrication processes and prototype devices.

Paper I reports etching and etch rate modeling results of high aspect ratio features. The applied model describes the deceleration of the etch rate in deep silicon etching qualitatively with various pattern shapes. The limiting mechanisms for the etching of high aspect ratio features are discussed.

Paper II reports the results of characterization of loading effects in deep silicon etching.The importance of the loading effect on the silicon etch rate is compared with the aspect ratio dependent etch rate.

Paper III describes the application of near infrared (IR) microscopy for determining the sacrificial etch length of SOI buried oxide and for inspecting the release process results of SOI devices in a fast and non-destructive way.

Paper IV presents the square-extensional single crystal resonator and its application as part of a reference oscillator, an example of the promising applications of SOI micromechanics. The resonators were fabricated with methods developed during the course of this work and described in the thesis.

Paper V introduces "plug-up", a new fabrication process for SOI micromechanics. The plug-up process alleviates problems with aluminum exposure to oxide etchant during sacrificial etching. It is also shown that with this process notching and stiction problems can be avoided.

Paper VI describes how the developed plug-up process can be used as a platform for monolithic integration of SOI MEMS and CMOS integrated circuits. All types of transistors and passive devices fabricated after a plug-up sequence on wafers having vacuum cavities are shown to work similarly to devices made on standard bulk silicon wafers.

2. Silicon micromechanics

A short review of existing process technologies for making micromechanical devices of silicon is given here. The key advantages and differences of the process technologies are compared and the motivation is given for the current interest in SOI micromachining. Obviously, silicon is not the only material choice for micromechanics; there are plenty of other suitable materials such as other semiconductors, metals, ceramics, and polymers, but these are beyond the scope of this work.

2.1 Surface and bulk micromechanics

Silicon micromechanics traditionally falls into two categories. The first is surface micromechanics, where structures are based on thin films grown or deposited on the wafer surface. The most widely used material in surface micromechanics is low-pressure chemical vapor deposited (LPCVD) polycrystalline silicon as a structural material and silicon dioxide as a sacrificial layer. The silicon wafer acts merely as a carrier for the structures. The devices are made of thin films deposited on the surface; the maximum thickness of the film stack is of the order of a few micrometers. The processes are similar to those used in semiconductor IC fabrication. A schematic fabrication process flow of a polysilicon cantilever beam [3] is depicted in Figure 2.
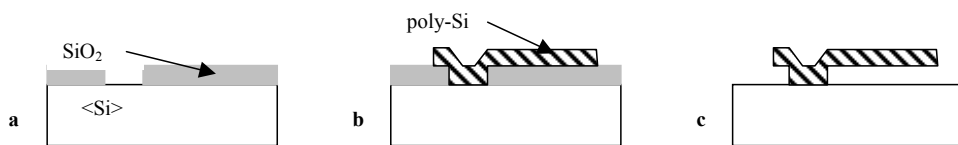
Figure 2. Simplified fabrication process of polysilicon cantilever beams; a) patterning of sacrificial layer, b) poly deposition and patterning, and c) sacrificial layer etching.

First a sacrificial oxide layer is deposited and patterned. Selection of the deposition method depends on the characteristics required on the oxide. If a high etch rate in hydrofluoric acid is required, a doped LPCVD oxide like phospho-silicate glass (PSG) is a suitable choice. The structural polysilicon is then

deposited over the sacrificial layer and patterned. After patterning of the polysilicon, the structure is released by etching the sacrificial layer beneath the structure. Despite the apparent simplicity of the above process there are many constraints and difficulties in the fabrication of such polysilicon devices. The internal film stress in the structural material should be controlled. Usually the deposited polysilicon film is originally under compressive stress and thicker polysilicon films can have non-uniform stress along the film thickness. The compressive stress causes buckling of the released bridge structures [3] and the internal stress gradient causes bending of the cantilever beams. Low tensile stress is desired in order to make the structures stiffer to avoid stiction [4] of the released structures. The internal stress in the deposited polysilicon film can be controlled by deposition conditions, post-deposition annealing [3, 5], or film doping [6]. The bridge structures, which have both ends fixed, are less sensitive to stiction and to bending by the stress gradient than cantilevers that stick to the substrate at shorter released beam lengths. Thus bridges or other structures supported at the edges are preferred over cantilever beams, which have only one support point, when structures are made of polysilicon thin films. On the other hand, cantilever beams of the same flexibility consume a smaller silicon area than do bridge structures.

The advantage of polysilicon surface micromachining is that all the fabrication methods, equipment and materials can be the same as used in standard CMOS fabrication [3, 7, 8]. With one or two polysilicon layers it is possible to fabricate various kinds of devices including motors, resonators, varactors etc [9]. With planar processes and chemical-mechanical polishing (CMP) planarization [10] it is possible to increase the number of polysilicon layers. The process developed by Sandia National Laboratories has five polysilicon layers [11].

Although polysilicon has very good mechanical properties and the processing technology is mature, the electronic properties of polysilicon are inferior compared to single crystal silicon, and the capacitance density obtainable with thin polysilicon layers is rather limited. The emerging SOI micromachining techniques are expected to alleviate some of these problems. Other ways to increase the capacitance density and the height of the structures are using a thicker film and increasing the surface area of capacitors by etching deep trenches into the substrate, which is no longer traditional surface micromachining.

The second main category is bulk micromechanics, where the devices are made of the silicon wafer material by etching, usually by inexpensive anisotropic wet etching. The structure thickness can be as high as the wafer thickness. Silicon is etched anisotropically in KOH, EDP or TMAH solutions. These alkaline solutions are convenient and highly selective etchants for silicon. All these etchants etch silicon anisotropically, which may be an advantage or disadvantage depending on desired result. The anisotropy of wet etching is a result of the crystalline structure of the silicon: some crystal orientations are more resistant to etching than others. The typical pyramid shapes or V-grooves are produced to a <100>-oriented silicon wafer by an anisotropical etchant, when the etching reaction proceeds in the <100> direction and stops when the etch front hits the {111}-planes [12, 13]. The inclined sidewalls of the etched trench restrict the freedom of structure design and can lead into excess consumption of silicon surface.

A main benefit of bulk micromachining is that large seismic mass is available for accelerometers or other inertial sensors, where sensitivity is scaled with the seismic mass.

2.2 SOI micromechanics

Silicon on insulator wafers has long been used for fabrication of high voltage, latch-up free and radiation hard integrated circuits. SOI wafers for IC use are usually made by SIMOX technology or newer layer transfer technologies [14]. They have relatively thin oxide and structure layers (100–200 nm thick). The insulating buried oxide (BOX) layer reduces leakage currents, eliminates the latch-up, and reduces the parasitic capacitances, since the devices are now isolated with an insulating layer instead of junction isolation.

Fabrication of SOI wafers by silicon fusion bonding was introduced in the eighties. In the bonding process the bondable surfaces of the two wafers are bonded together without external pressure and annealed at elevated temperature [15].

The bondable surfaces should be clean and smooth. The attraction forces utilized in wafer bonding are mainly van der Waals interaction or hydrogen bridge bonds [16, 17]. To assist the bonding the surfaces should be activated. The bonding strength (measured as surface energy) is dependent on the surface quality,

activation method, bonding atmosphere, and annealing time and temperature. The wafers that are bonded can have pre-patterned structures to form cavities during bonding.

After bonding, the other wafer is preferentially etched or ground to the desired thickness and polished. The practical minimum thickness of the structure layer that can be fabricated is in the range of few micrometers. Fusion bonding is not a preferred method for state-of-the-art VLSI SOI as the obtainable silicon layer thickness is generally too thick with minimum thickness in the 5 μm range. The thickness of the SOI structure should be scaled with device dimensions and operational voltages. The technology has been used to fabricate SOI substrates for silicon power devices, and also has wide applications in the fabrication of silicon sensors, actuators and other microstructures.

The fusion bonding method was quickly adapted to fabrication of pressure sensors because of the simplicity of making sealed cavities by bonding pre-patterned wafers [18, 19, 20]. Some bottlenecks of polysilicon surface micromachining are alleviated by wafer bonding. Superior silicon quality, low internal stress, reproducibility of mechanical properties and larger structure thickness range are obtained with bonded SOI.

Silicon fusion bonding (SFB) has already been used in novel accelerometers, high-temperature pressure sensors, miniature pressure sensors and high over-range pressure sensors. Interest in SOI micromachining exploded as the new deep silicon etching methods evolved [21]. The Bosch patents [22, 23] on switched silicon etch process and equipment manufacturers' efforts in the area of etch reactors and plasma sources [24, 25] have enabled the development of new silicon high aspect ratio microstructure technology (HARMST). In one of the first trials of SOI micromachining using ordinary RIE, Benitez et al. [26] presented many of the features of this new SOI micromachining. The main benefits of SOI micromachining over polysilicon surface micromachining are the following: It is a mechanically excellent single crystal material; cavities can be fabricated by bonding patterned wafers; a wide range of structure thickness is available; high aspect ratio structures are possible; the oxide layer is highly versatile as a sacrificial, isolation or etch stop layer.

The main advantages of SOI micromachining over bulk micromachining are as follows: Cavities can be fabricated by bonding patterned wafers; there is effective electrical isolation and good availability of the etch stop layer; and there is freedom of shapes in dry etching. The key points of different silicon micromachining technologies are compared in Table 1.

Table 1. Comparison of micromachining technologies.

Surface micromachining	Bulk micromachining	SOI
Thin structures	Thick structures	Thick and thin structures
Low mass	Large mass	Large mass possible
IC compatibility	No IC compatibility	IC compatibility
Insulating layers available	No insulating layers	Insulating layers available
Control of thin film thickness	Thickness control by timed etching or crystal orientation	Control of layer thickness by grinding and polishing
Low price starting material	Low price starting material	High price starting material
Stress control required	Low stress structures	Low stress structures

The distinction between surface micromechanics and SOI mechanics is not clear. The fabrication methods used for SOI micromachining are mostly the same planar processes as those used for polysilicon surface micromechanics. The structure layer thickness in SOI micromachining can be almost anything above 5 μm and even thin IC SOI has been used for micro resonators [27]. The LPCVD polysilicon structures are usually limited to about four micrometers in thickness but the epipoly (thick polycrystalline silicon films deposited in the epireactor) wafers come close to SOI in all their properties except for crystalline structure [28]. The HexSil process is another way to increase the effective height of polysilicon structures [29, 30].

2.3 Monolithic integration of MEMS and ICs

As the integrated circuits are predominantly made of silicon and the new microsystem technology is also mainly based on silicon, it is only natural that methods for combining both the mechanical and electrical functions within one chip are eagerly sought after.

The compatibility of IC process and micromechanics process does not come naturally, but the integration requires modifications and compromises to either part to achieve compatibility. The fabrication process flow of an integrated microsystem should be considered comprehensively, because the processing steps are strongly correlated and a small change in one process parameter can cause a chain of changes in other parameters. Modularity is often desired for simplifying process changes and the design of possible new devices [31]. First the order in which the different elements are fabricated should be chosen. This partitioning and ordering of the main process modules can be done in several ways: the MEMS part can be fabricated before IC or vice versa or the whole process can be a mixed process where the fabrication steps are interleaved. The main points of the most common integration approaches are presented here.

2.3.1 "MEMS first"

A prerequisite for any IC process is the availability of a smooth high quality single crystal silicon surface for active device processing. The wafer surface has to be planarized if the MEMS part is done before the IC process. The materials used in MEMS parts should be IC compatible, which in practice usually makes the list of usable materials very short, leaving only polysilicon, silicon dioxide and silicon nitride as material choices. Single crystal silicon is also a possible material for MEMS structures, but planarization after fabrication of thick mechanical structures may pose problems. In every case, the structure has to withstand the harsh semiconductor fabrication process conditions including high temperature steps, ion implantations, etching steps and so on. Another issue is that the MEMS structures must not unpredictably disrupt the IC fabrication. IC foundry acceptance of wafers with pre-processed MEMS structures is hard to get, and usually it is possible for high volume applications only.

The main reason for using the MEMS first approach is that the stress control of polysilicon requires high temperature annealing, which is not compatible with the IC metallization schemes or shallow junctions needed in modern circuits.

Examples of the MEMS first approach are the Sandia Laboratories process [32] and Analog Devices´ ModMEMS process [33]. The mechanical parts are constructed of polysilicon and oxide layers. The polysilicon layers are protected with an oxide layer and single crystal silicon is deposited epitaxially in regions where circuits are later processed. The epitaxial layer is polished with CMP before circuit fabrication.

In another approach micromechanical devices are fabricated in a trench etched on the surface of the wafer. Once these devices are completed, the trenches are refilled with oxide, planarized using chemical-mechanical polishing, and sealed with a nitride membrane. The wafers with the embedded micromechanical devices are then processed using a conventional CMOS process. Additional steps are added at the end of the CMOS process to expose and release the embedded micromechanical devices.

A fine example of a different MEMS first approach is Infineon´s "cavity micromachining" [34], where released polysilicon accelerometer structures are embedded within a wafer-level vacuum, which also forms a zero-level encapsulation for micromechanical devices.

2.3.2 "IC first"

One main benefit of the IC first approach is that the standard IC process can be used and the IC foundry can fabricate a suitable amount of wafers for post-processing without the extra cost of IC process development. Post-processing can then be performed outside the original IC fab, but intimate co-operation between the IC foundry and MEMS post-processing design is required. In this case, more material options are available for MEMS fabrication. The thermal budget, however, is very limited, because the aluminum metallization cannot be heated above 450°C.

Small changes in the IC process are possible to make post-processing easier. Bustillo et al. [35] developed a modular integrated approach in which the aluminum metallization of CMOS is replaced with tungsten to enable the CMOS to withstand subsequent micromechanical processing steps up to 700°C.

In the IC first approach one can use the IC metallization layers as structural layers or one can use the polysilicon gate material as mechanical material. However, these materials are not optimized for mechanical operation and typically one must use post-processing of CMOS wafers to achieve the desired mechanical properties. The extra metal and insulator layers can be deposited and patterned after the IC process, but great care must be taken not to exceed the allowed thermal budget and to use etching methods that do not attack the CMOS parts. A new structural material choice for post-CMOS MEMS integration is polycrystalline silicon-germanium, which can be deposited and annealed at temperatures below 450°C [36].

The post-processing of IC can also be some kind of etching and release of single crystal structures, like QinetiQ´s thick film SOI approach [37] or the SCREAM (Single Crystal Reactive Etching and Metallization) process for isolating structures from a bulk silicon wafer [38].

2.3.3 Mixed processes

Mixed processing is the most difficult way to fabricate integrated microsystems. Both the MEMS and IC parts should be designed at the same time, which makes the modular design difficult. Mixed processing is an expensive solution and suitable only for high-volume applications. Most mixed processes try to preserve the modularity.

A rather obvious approach to mixed processing is to insert deposition and patterning of MEMS parts between the front and back ends of the IC process, as in done by Analog Devices and Siemens [39]. However, they fail to report how the aluminum metallization and oxynitride passivation are realized after release of the micromechanical structures. In Motorola´s process [40] for monolithic tire pressure sensor fabrication, polysilicon MEMS structure fabrication is inserted between gate stack formation and temperature-sensitive source/drain formation.

For thick SOI MEMS Lemkin et al. [41] has designed a mixed process where isolation trenches are etched and backfilled before fabrication of integrated circuitry. In Analog Devices in the SOI MEMS process by Lewis et al. [42], poly-nitride insulation plugs are fabricated before the circuitry. This thick SOI approach allows the use of multi-level metallization in ICs, thus utilizing the full performance of a modern fine-line, high-density IC process. The post-processing steps for MEMS are all low temperature steps. The circuits must be protected during the final sacrificial oxide etching HF.

In a merged process by Weigold et al. [43], which uses bulk silicon for micromechanical elements, deep wells are made before the IC process to form pn-junctions that work as a chemical etch stop during release of the mechanical structures. VTT`s plug-up process [Paper VI], which is described later in this work, uses prefabricated vacuum cavities and isolation trenches before integrated circuit fabrication, which eliminates the need for wet etching of sacrificial oxide after CMOS.

3. Silicon plasma etching for micromachining

In this chapter deep silicon etching and its most important non-idealities are reviewed and the results of studies on etching and developments obtained during the course of this work are presented.

3.1 Plasma etching

Silicon plasma etching has long been the preferred method for patterning polysilicon gates of MOSFETs in fabrication of integrated circuits. Wet etching of conductors in liquid solutions was widely used in the past until requirements for line-width control necessitated the use of dry plasma etching. Plasma etching can offer better reproducibility and dimensional control because the etching can be anisotropic. In principle, plasma etching can be purely physical (sputtering), purely chemical, or ion-driven etching. Furthermore, ion-driven etching can be complicated by an etch inhibitor mechanism by addition of extra feed gases in the reaction chamber or by sputtering from the mask material. The anisotropy in plasma etching is a result of complex interactions of ion bombardment, chemical etching by neutrals, and deposition of sidewall passivation layers into etched features. Traditionally, plasma etching was used to pattern thin films, but with the success in etching of deep capacitor trenches for memory circuits [44] the interest in micromechanics applications and HARMST has also grown.

Traditional parallel plate-reactive ion etchers (RIE) [45], inductively coupled plasmas (ICP) [24, 46], and microwave plasmas [25, 47, 48] have been used for etching high aspect ratio trenches in silicon. The most typical plasma etcher configuration is the parallel plate etcher, but inductively coupled plasma arrangements have gained popularity for generating high density plasmas suitable for fast etching with relatively low voltage bias [24]. The generation of plasma further from the wafer surface helps to reduce the adverse effects of ion bombardment and sample heating. Some of the etch processes have been cryogenic [25, 49]. The chemistry has been based on halogens, fluorine being the most used because of its highest reactivity with silicon. Room temperature operation has been more popular than cryogenic, because the cryogenic fluorine

process is more temperature sensitive than a room temperature ICP process [50]. Chlorine and bromine have been used when suppression of lateral etching or undercut has been required [51].

In deep silicon etching for MEMS, typical etch depths are in the range of 10–500 µm. Fluorine based chemistry has been shown to achieve etch rates of several microns per minute, making deep silicon etching in plasma a viable alternative for KOH or TMAH based wet etching. With the high-density plasma generated in the ICP reactor it is possible to etch through the wafer [52], as shown in Figure 3. The etching is almost independent of the crystal orientation; it has excellent selectivity against masking oxide and photoresist layers and has a nearly vertical sidewall profile.
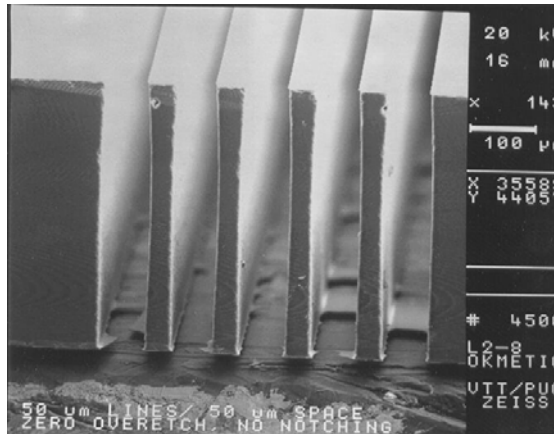

Figure 3. Vertical through-wafer trenches etched with a modern ICP reactor.

3.2 The Bosch process

An important invention in the development of deep silicon etching for micromachining is the Bosch process [22, 23], which enables etching of vertical sidewalls with a high etch rate and high selectivity against oxide and photoresist mask materials [24]. It is based on alternating silicon etching with SF_6 and fluorocarbon film-forming passivation steps with C_4F_8. The cyclic nature of the process is depicted in Figure 4. The Bosch process is sometimes also called the time domain multiplexed process, switched process, or deep reactive ion etching (DRIE), and the equipment manufacturers call the process by their trademarks.
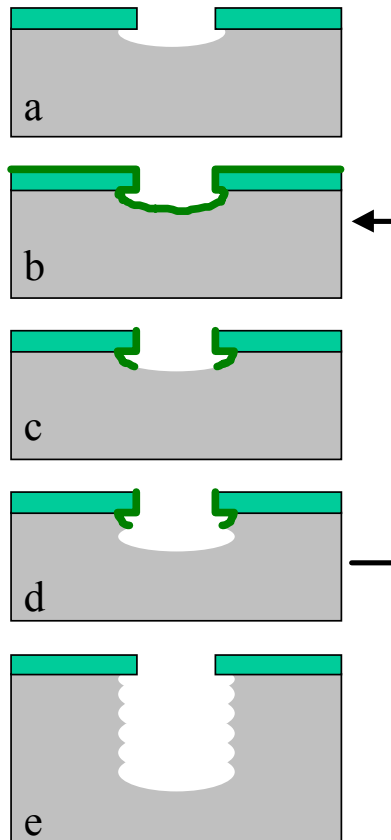
Figure 4. Deep silicon etching using the Bosch process: a) isotropic etch step, b) passivation deposition, c) removal of passivation layer, d) etch step, and e) resulting trench after repetition of steps b-c-d.

Traditional non-switched processes rely on simultaneous etching and deposition of the sidewall passivation layer. Different chemistry is then used, O_2 can be added to SF_6 for aiding formation of the passivation layer, and the use of CHF_3 is also popular in silicon trench etching [45]. Anisotropy can also be achieved by suppression of spontaneous isotropic etching by cooling the wafer to cryogenic temperatures or by using a more aggressive ion bombardment component in the etching process.

In a typical etching system for the Bosch process, two 13.56 MHz generators are employed: a high-power coil generator for creating an intense inductively coupled plasma (ion concentration above 10^{11} cm^{-3}), and an independent low-

power generator for biasing the wafer electrode (platen). Despite high power and high plasma intensity, the bias voltage is relatively low. The wafer is cooled during the process by helium backside flow. The wafer can be clamped to chuck either electrostatically or mechanically to ensure thermal contact to the electrode. Electrostatic clamping is used in this work. If thermal contact is lost or otherwise insufficient, the wafer temperature can rise too high for passivation deposition. The system configuration is described elsewhere [24], as are thorough process responses for main parameters [53–55].

The etching begins with an isotropic etch step, during which the exposed silicon is isotropically etched with SF_6 (sulfur hexafluoride) plasma. During the following passivation step a thin fluorocarbon film is deposited from C_4F_8 (octofluorocyclobutane). The fluorocarbon film acts as a sidewall passivation. The passivation layer is removed from the horizontal surfaces at the beginning of the next etching step. The alternation of etching and passivation steps produces the typical scallops on the sidewalls. The scallops and other typical undesired features of the switched process are shown in Figure 5.
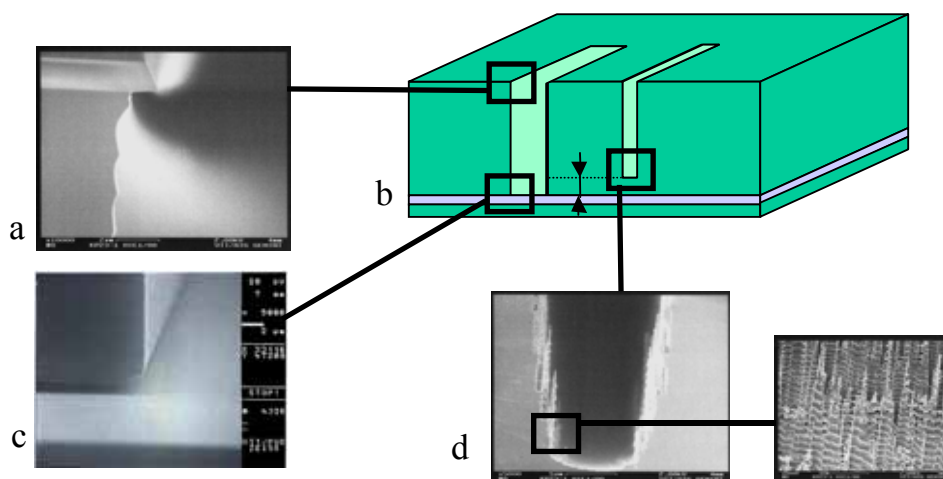

Figure 5. Typical features of the Bosch process: a) mask undercut and scallops, b) aspect ratio dependent etch rate, c) notching, and d) sidewall roughness.

The system is very versatile and the etching process can be tailored for various applications. The main parameters of the two baseline processes used in this work are tabulated in Table 2.

A high rate process [56] is targeted for through-wafer etching. It has a long etch pulse followed by a shorter deposition pulse, at a pressure of 40 mtorr. The maximum etch rate is more than 7 μm/min. The etch rate uniformity, profile, and undercut of this process are compromised for the high etch rate [56].

The SOI or low etch rate process is used for etching the device layers of micromechanical SOI wafers which are typically 5–15 μm thick. The maximum etch rate is 1.6 μm/min in our process. The process pressure is 15 mTorr with equal etch and deposition pulse lengths. Its main characteristics are good profile control and small aspect ratio dependent etch rate (ARDE).

Table 2. Parameters and performance of baseline etch recipes used in this work [56].

Process	SOI	Deep
Target depth	5–20 μm	380–525 μm
Pressure (mTorr)	15	40
SF_6/C_4F_8 pulse times (etch: pass)	5 s : 5 s	13 s : 7 s
SF_6/C_4F_8 flows (sccm)	129/120	129/85
Coil/platen power (W) (etch)	600/8	600/10
Maximum etch rate (ER) (for 128 μm feature, μm/min) Average ER (AR=10:1)	1.6 1.35	7 4.85
Si:Ox selectivity	150:1	250:1
Si:Photoresist selectivity	80:1	Not measured
Undercut (micron)	0.25	2
Sidewall profile (angle)	Positive	Retrograde/barrel

3.3 Aspect ratio dependent etch rate (ARDE)

The first non-ideality observed is the ARDE or RIE lag. While etching high aspect ratio trenches into silicon with reactive ion etching (RIE) using an SF_6/O_2

chemistry, it is observed that the etch rate depends on the mask opening. This effect is known as RIE lag and is caused by the depletion of etching ions and radicals or inhibiting neutrals during their trench passage [57].

Ideally etched depth should increase linearly with the etch time, but in practice there is a slowdown as etch time and the aspect ratio increase. Initially ARDE and the RIE lag were considered by many to be phenomena specific to submicron features [58, 59], but recently they have been encountered also in micromechanical applications with pattern dimensions of tens and hundreds of microns.
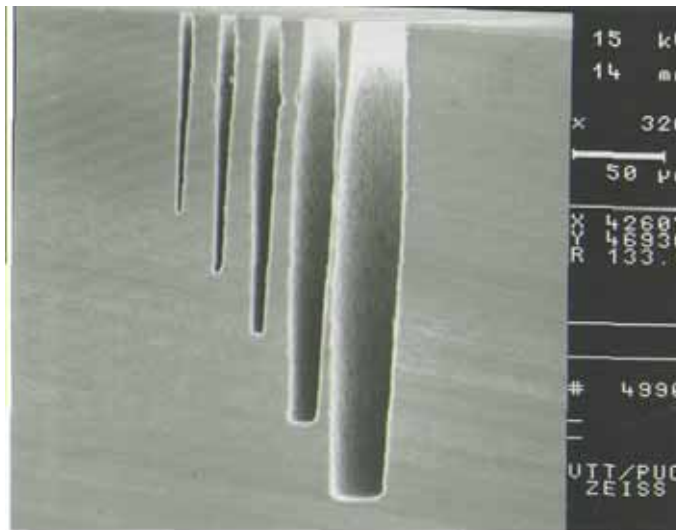

Figure 6. SEM micrograph showing the ARDE effect. Nominal widths of the shown features are 1, 2, 5, 10, and 20 μm.

A typical aspect ratio dependency in deep silicon etching is shown in Figure 6. The etch depth of a nominally 1.0 μm wide trench is less than half the depth of a 20 μm wide trench. The etch profile is also dependent on the width of the trench. Narrow trenches have positively tapered sidewalls whereas wide trenches typically show re-entrant angles. As the aspect ratio increases, the profile turns into positively tapered, resulting in bowing. With high aspect ratios the feature closes up at the bottom and the etching stops. In the reactor and processes used

in this work, the limit of this aspect ratio was 10:1 for circular holes and about 25:1 for long trenches [Paper I].

ARDE in plasma etching has been attributed to a wide range of physical mechanisms. An excellent review of this topic has been published by Gottscho et al. [60], which the main mechanisms for aspect ratio dependent etching are reviewed: differential charging of insulators, field curvature near conductors, image force deflection, ion shadowing with ion angular distribution, radical/inhibitor shadowing, molecular flow, bulk diffusion, and surface diffusion. Jansen et al. [57] studied RIE lag in high aspect ratio silicon etching using SF_6/O_2 chemistry. They concluded that ion depletion is probably the main cause of RIE lag. Coburn and Winters [61] introduced a simple conductance model based on Knudsen transport of particles in etched trenches, where the molecular flow conductance limits the etching species arriving at the bottom of the feature. They derived the following equation for the ratio of the etch rate at the bottom of the feature $R(A)$ to the etch rate at the top of the feature $R(0)$:

$$R(A)/R(0) = K /(K + S - K \cdot S) , \tag{1}$$

where S is the reaction probability on the bottom surface and K the molecular flow transmission probability for a given tube or trench. A is the aspect ratio: depth/diameter for a circular hole or depth/width for a long trench. We have shown previously [62] that the simple conductance model can be used to predict the etch rate of a Bosch process with good results, when applied to line widths typical of MEMS at moderate aspect ratios.
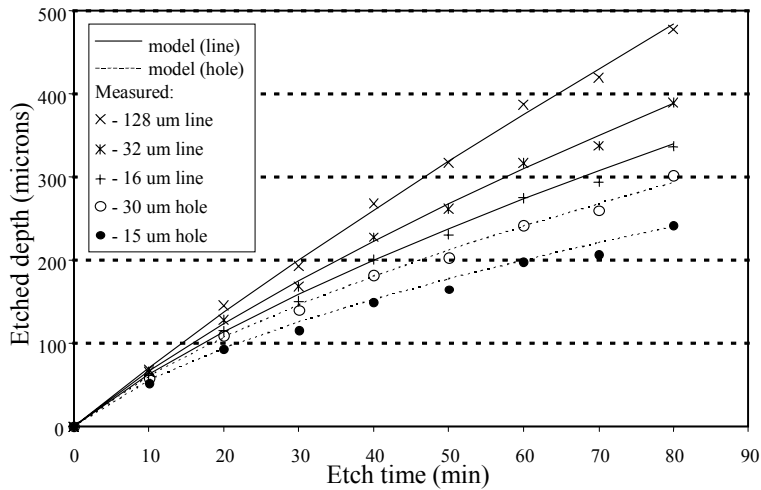
Figure 7. Etch rate modeling results using molecular flow conductance for circular holes and long trenches with initial etch rate R*(0) of 7.27 μm/min, and reaction probability* S *of 0.27 [62].*

The modeled scaling of the etch rate is correct. The Knudsen model is consistent with our experimental data. The simple flow conductance model [61] describes the etch rate qualitatively for a large range of aspect ratios and line widths. Simple line-of-sight models, which effectively take only the ion shadowing into account, do not model the etch rate correctly. The conductance model does not give correct results in situations where mechanisms other than neutral transport limit the etch rate [57]. The empirical model by Muller et al. [63] that fits the RIE etch rates generally well with a second-order polynomial does not fit the Bosch process results properly. Blauw et al. [64] investigated the dry etching of deep silicon structures in SF_6/O_2 plasma at cryogenic temperatures. They studied the etching of both vertical and horizontal trenches. The ion bombardment was excluded in the horizontal structures. Their results indicated that ARDE is due to Knudsen transport of fluorine radicals.

With the molecular flow conductance model, the effect of the etching process and the feature shape and size are decoupled. The only process parameters used are the initial etch rate and the etch reaction probability. The etched feature is characterized by the transport coefficient only. The instantaneous etch rate is easily calculated with formula (1), but unfortunately the calculation of the etch

depth is not possible in closed form; however, it is easily calculated with a spreadsheet program when tables or formulae for transport coefficients are available. For calculation of the transport coefficient of the results in Figure 7, analytical formulae of infinite slots and circular tubes [65] were used. For other shapes of interest no practical analytical approximations were available. A simple Monte Carlo program was written to obtain the transport coefficient for rectangular tubes [Paper I]. The transport coefficients as function of aspect ratio are plotted in Figure 8. With the obtained coefficients the etch rates of rectangles of varying length to width ratio could be modeled. Previously measured etch depths [62] are tabulated in Table 3. The modeled and measured etch depths are plotted in Figure 9a. Again the model describes the etch rate with surprising accuracy when shorter (30 and 60 minute) etch times are used.
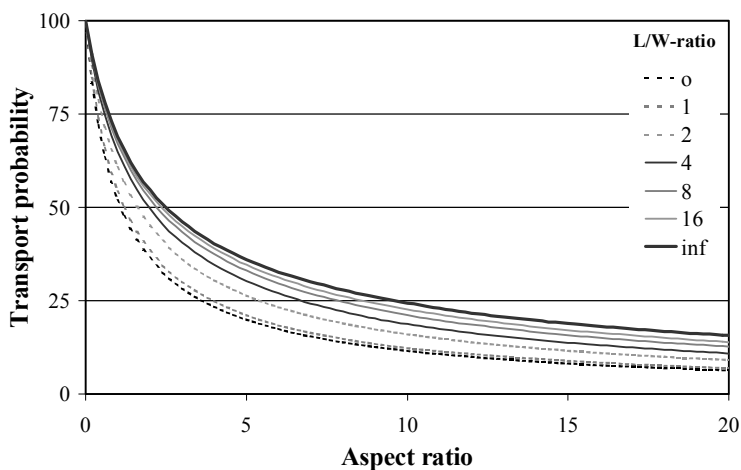

Figure 8. Transport coefficient for different rectangular tubes, length to width ratio as a parameter ("o" in the legend denotes the circular hole and "inf" the trench of infinite length).

Table 3. Measured etch depth of 20 μm wide rectangles obtained with the recipe "deep".

Etch time: L/W ratio	30min	60min	90min	120min
1	135	220	283	308
2	145	243	309	341
4	154	265	329	370
8	158	278	339	381
16	165	278	378	410
32	163	278	385	417

Calculation of the transport coefficients above does not take etching reaction on the sidewalls into account. The undesired lateral silicon and passivation layer etching, which cause undercut and bowing, consumes fluorine and lowers the portion of the free fluorine from the plasma that reaches the bottom of the etched feature. In the Monte Carlo simulation a loss mechanism was implemented to take sidewall reactions into account, for a given probability in each sidewall collision the particle under calculation was deleted. The etch rates and depths were recalculated using new lossy transport coefficients. Best fit to our earlier experimental data [62] was obtained with a sidewall reaction probability of 1.5%. The modeled results compared to measured etch depths are shown in Figure 9. Later Volland et al. [66] simulated etch profiles in a two-dimensional simulator with a similar approach to neutral transport. In their case the best fit was obtained with 2% sidewall reaction probability. The sidewall reactions are probably etching reactions of the passivation polymer because the sidewalls are covered by the passivation polymer and usually there is negligible silicon etching occurring because the sidewalls remain nearly vertical. Ayón et al. [67] have reported the etch selectivity between silicon and the passivation polymer as being 25:1 on horizontal surfaces, which is quite close to the ratio of reaction probabilities that give the best fit to our data (0.27 : 0.015).
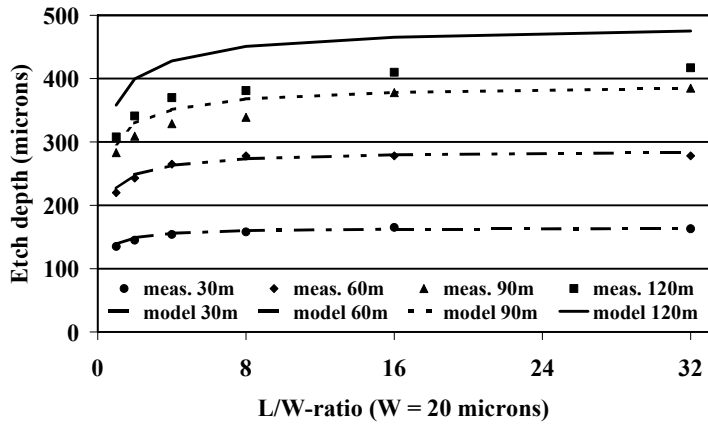
a)
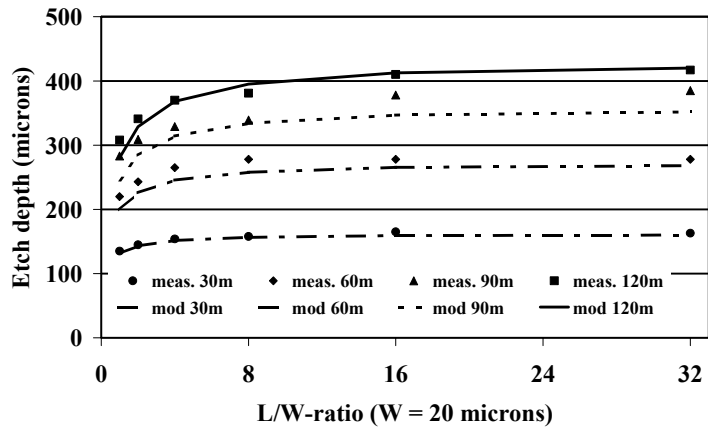
b)

Figure 9. Modeled vs. measured results of etching rectangle with varying L/W ratio. a) model with no sidewall reactions, b) model with sidewall reaction coefficient of 0.015.

When trying to maximize the aspect ratios, the ion energies should be increased and angular distribution should be narrow so that the passivation polymer is effectively removed from the trench bottom. However, the increased ion bombardment reduces the mask selectivity. Obviously the balancing of passivation and etching components is very important [68].

Sometimes changes in etch process parameters are desired to compensate for changes in the aspect ratio of an etchable feature. For such etching, multistep recipes or parameter ramping can be used [69, 70]. We have not tried to model

the etch rates with parameter ramping because one would need the parameters E_0 and S for each process point. It would be possible to determine the parameters by measuring the instantaneous etch rate of a large test pattern by reflectometry [71] and then use the data to model the etch rate of different shapes.

At low aspect ratios (< 2:1) ARDE is not a serious consideration, and may be hidden by local pattern density or within-wafer variation, but in micro-mechanical structures typical thicknesses are 5–500 μm and the minimum line widths are few microns; i.e. aspect ratios are 5:1 to 20:1 and size-dependent etch depths are encountered.

In the literature there have been claims that RIE lag has been eliminated both using traditional RIE [72] and the Bosch process [53]. However, that only seems to be the case for single process time, and it is very much dependent on the design [72]. Aspect ratio independent etching can be obtained if the depletion of fluorine radicals due to Knudsen transport is compensated by a mechanism with other kind of aspect ratio dependency. RIE lag or ARDE can be inversed if polymer deposition is enhanced by high pressure [73]. Process conditions for inverse RIE lag has also been obtained with a simulation approach [66].

3.4 Loading effects

Large exposed areas cause slowdown of the etch rate and can adversely affect the radial uniformity. Reduction of the etch rate with increasing etchable area is called the loading effect, and it is an important source of etch depth non-uniformity. It is caused by depletion of the etchant species. The effect is extremely severe in high etch rate processes where chemical etching is the main etch mechanism. The switched process with isotropic etching of silicon by fluorine is especially prone to the loading effect. Loading, or pattern density effect, can be seen on different scales, from wafer scale to feature size scale, depending on the particular reactor configuration/etch chemistry.

A general model for the effect of loading on etch rate was developed by Mogab [74].

$$ER = \frac{\beta\tau G}{1 + \beta\tau\dfrac{A_w d}{V}} \quad , \tag{2}$$

where β is the proportionality factor describing the affinity of the material being etched (silicon) to active species (fluorine), τ is mean lifetime, G is the generation rate of active species in plasma, d is a constant containing constants of chemical reactions and materials being etched, A_w is the etchable area, and V is the plasma volume.

It is known that time-domain multiplexed deep silicon etching suffers from serious loading effects typical to reactant transport-limited chemical etching. We have investigated the magnitude of the loading effect with test structure designs at both micro and macro scale [Paper II]. Our test results with a large test pattern stepped with varying density over a wafer are shown in Figure 10, together with the results of 100 μm wide trenches and the modeled result using equation (2). The last data point is from a blank wafer. The blank wafer etch rate is calculated from weighting the results before and after etching, the other values are from SEM cross-sections.
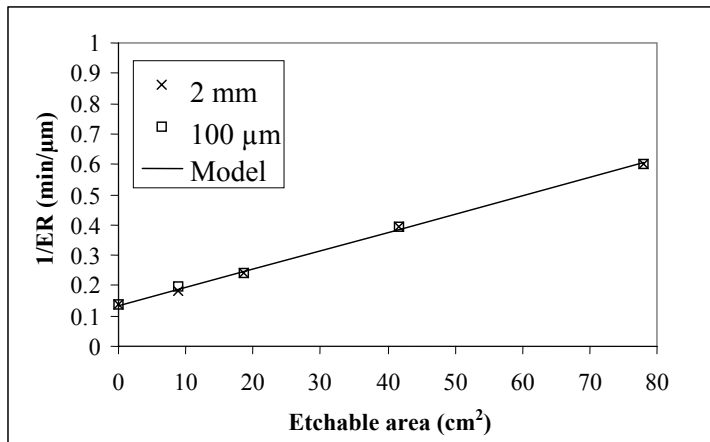

Figure 10. Modeled inverse etch rate as function of Si load. (The solid line is the modeled result, ×-marker 2 mm square and □-marker is for 100 μm wide trench).

The model gives very good fitting. At large loads it has to be considered that etch rate non-uniformity across the wafer is significant. Another important consideration is that the maximum aspect ratio was only 3:1. At such low aspect ratio structures ARDE is insignificant and therefore etch rates of 2 mm squares and 100 µm lines are almost identical.

A comparison of the ARDE and the loading effect is shown in Figure 11. For long etch times and high aspect ratio the ARDE has a stronger effect on etch depth non-uniformity than loading.
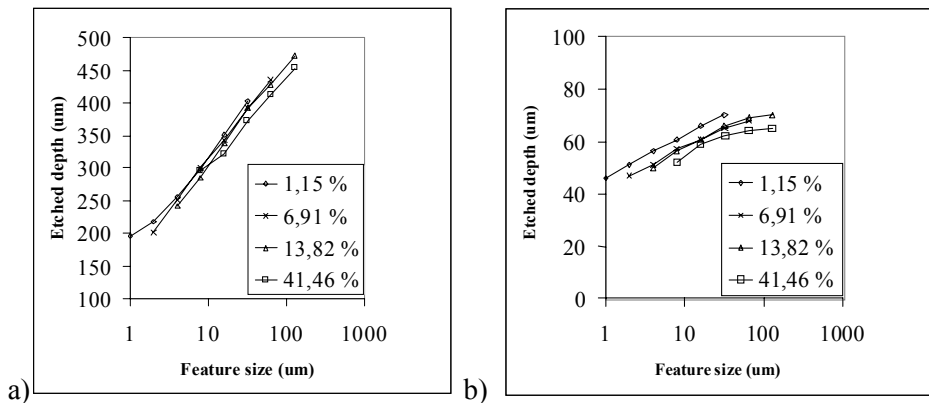

Figure 11. a) 80 min etch time: feature size effect dominates over loading, b) 10 min etch time: microloading and feature size effect both affect etched depth. Local load is varied from 1.15% to 41.46%.

A macro scale side-effect of the loading is, because of the reactor geometry, that fluorine starvation is more severe at the center of the wafer than at the edges. This leads to non-uniformity of the etch rate at high etchable areas, and the edges are etched faster than central parts of the wafer.

At micro scale our test structures gave a null result: in a group of five similar trenches all of them were of equal depth. If microloading were noticeable the outermost trenches would have been etched deeper. A group of five trenches does not from a notable sink for etching gases; a more substantial etchable area is needed to induce the loading effect. In order to determine the scale at which the loading effect becomes notable we used different sized squares (2 mm,

4 mm, 6 mm, and 8 mm side length) stepped on a wafer. The etch depth of a 100 μm wide trench adjacent to each large square was measured. The etch depth of the trench near the 2 mm square was 2% lower than etch rate of an identical isolated trench and the etch depth of the trench near 4 mm square was 7% lower compared to the isolated trench. In the chip scale test we used different sized (2.5 mm, 5.0 mm 10 mm) chips with varying pattern load. The pattern load in the smallest chip had no effect on etch rate whereas the larger chips had a notable effect. We estimated that the reactant depletion distance for our baseline process is therefore somewhere between 3 to 5 mm.

Similar results have been obtained by Jensen [75] and by Rickard and McNie [76]. Jensen has also found that normal microloading behavior can be turned into inverse microloading by process conditions: with high fluorine flows it is possible to shift the etching to an ion-limited regime where fluorine starvation does not cause a loading effect [77].

The etch rate reduction in the largest chip with 40% load was about 10%. Hedlund et al. [78] studied the loading effect of silicon etching with RIE. They concluded that the effect is relatively small (< 10%) compared to other pattern dependent effects like ARDE. However, they did speculate that the loading effect would be more pronounced for high aspect ratios. Our experience with deep silicon etching does not support this. On the contrary, it seems that as the etch rate is reduced at high aspect ratios the consumption of fluorine decreases, which should reduce the loading effect.

Another effect of the loading on a small scale is shown in the drawing of Figure 12. The bottom of the etched feature is concave for narrow features and becomes convex for wider trenches. The convex bottom observed [79] is caused by local depletion of the etchant species at the center of the large area feature, while narrower features exhibit the normal ARDE behavior.
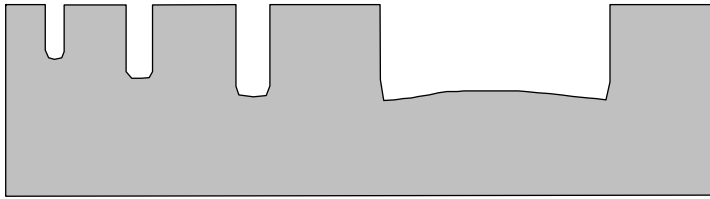
Figure 12. Schematic presentation of appearance of the aspect ratio dependent etch rate and loading in a very large feature.

From our results [Paper II] it can be seen that oxide etch rate uniformity is better than silicon etch rate uniformity. Oxide etching is not affected by silicon load. Therefore the apparent oxide selectivity decreases mainly because of silicon ARDE. Because of this, selectivity needs to be defined for specific line widths.

At macroscopic scale the loading effect is unavoidable but at microscale the adverse effects of loading can be alleviated to some extent by clever design. The behavior of the loading effect at macroscopic scale is well described by the model of Mogab, and in our ICP reactor the etch rate dramatically decreases when the etchable silicon area exceeds 20%.

The silicon etch uniformity is severely affected by loading. The radial etch non-uniformity causes extra requirements for etch selectivity against the etch stop layer. To be able to correctly predict the etch depth of arbitrary features the models for pattern dependent etching and the loading effect should be coupled at both micro and macro scales.

3.5 Charging effects

Feature charging and notching are well-known effects in gate polysilicon and conductor metal etching [80, 81]. Incoming ions from the plasma alter the electric fields near the wafer surface. When etching a conductive layer on an insulating layer, the accumulated charge is discharged until the insulator layer is reached. When the positive charge is accumulated on the bottom of the etched trench, the incoming ions are deflected by Coulombic repulsion to the lower part of the sidewall, where the passivation layer is thinner than in the upper sidewall. The increased ion bombardment with weaker passivation deposition results in

excessive etching at that point. Moreover, as the notch is not in line of sight from the plasma the passivation deposition is reduced, causing positive feedback in notching, and the amount of available etchant species is also increased as the consumption of etchants is reduced at the oxide interface. A typical appearance of the notching is shown in Figure 13.

The amount of notching is dependent on both charging and the over-etch time. There are two ways to avoid notching: either prevent the charge accumulation during etching or stop precisely at the time when the insulating layer is reached. Both of them are practically impossible. There is probably no way to totally eliminate charging in a plasma etching process, which in great part relies on ions to etch the passivation layer and ion-assisted silicon etching. It is not likely that zero over-etch would be possible because of various etch rate non-uniformities. The remaining solutions are reduction of charging during the etching process and reduction of the etch rate non-uniformities by design rules.
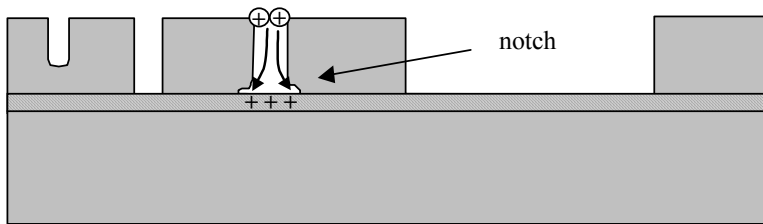

Figure 13. Schematic presentation of appearance of the notching.

Measurement of the amount of notching is difficult. Notching is strongly affected by the pattern shape, and generally it is impossible to know for how long a feature has been over-etched, because both the etch rate and feature charging are aspect ratio dependent. The notch develops very quickly in high aspect ratio features, so the over-etch time should be minimized. As a simple rule of thumb, there is no notching when the spect ratio is less than 1:1. A clear example of this is seen in Figure 14.
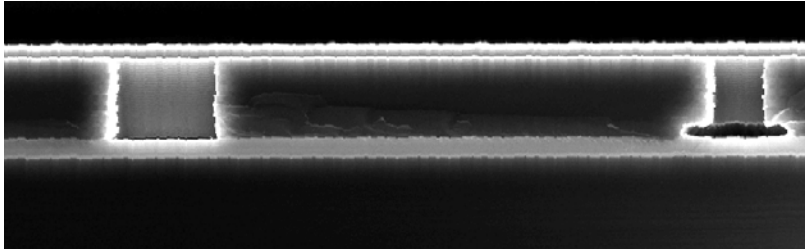
Figure 14. SEM micrograph of notching on 10 μm thick SOI (picture courtesy of Antti Lipsanen).

An alternative way to avoid etching is to use a separate pulsed low frequency (LF) generator (380 kHz) for biasing the platen. This method is patented by STS plc. [82]. The LF frequency option called "SOI upgrade" allows ions to escape more readily from deep trenches when the etching cycle is done. From this the over-etch sensitivity decreases, and the notching or "footing" of silicon structures is minimized.

Typically SOI etching can be done using high frequency bias until the largest features are cleared and the insulating layer is exposed; at that point the etching is continued with low frequency bias. The starting point for low-frequency biasing is determined by time or by end-point detection. A laser interferometric technique has been shown suitable for end-point detection when using the Bosch process [71].

During a semiconductor equipment assessment project Microspect [83], the performance of the STS´s high rate etch tool was evaluated in narrow trench etching for resonators [84]. Submicron etching resulted in unexpected charging on the top portions of the SOI structure layer when the high frequency bias source was used. When a LF bias source was used no damage occurred. This is shown in Figure 15. The geometrical characteristics of this type of damage were not investigated and the origin of this damage remains unclear. The damaged structure also shows unexplained signs of crystal orientation dependent etching. The charging seems to prevent the passivation layer deposition. The amount of fluorine locally available for etching is excessive and the surface reaction rate probably becomes the limiting factor. In silicon plasma etching, crystal orientation dependence is usually seen in cryogenic etching [64].

Again, the notching effect can be useful as shown by Ayón et al. [85] and
Docker et al. [86]; they have used the notching to dry release beams.
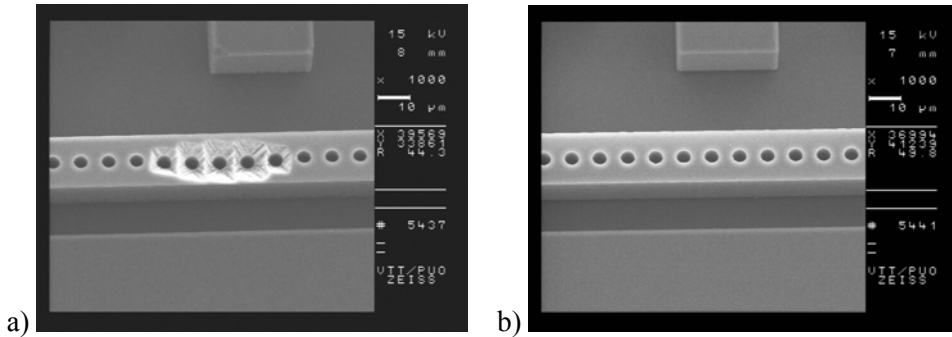

a)   b)

*Figure 15. Charging damage on top of the SOI structure layer: a) charging
damage when RF biasing used, b) charging damage eliminated with low
frequency biasing [83].*

3.6 Future challenges in deep silicon etching

Device designers' desires for higher etch rates, higher aspect ratios, and
narrower features place growing challenges on equipment and process
development. Higher etch rates are needed to increase the throughput of etch
tools to lower the cost of ownership. Higher aspect ratios are needed in through-
wafer vias, which are essential for three-dimensional integration of
microsystems. In applications that use electrostatic actuation, narrow gaps in the
submicron range are desirable to lower the operational voltage to CMOS
compatible levels.

These goals are continuously pursued by equipment manufacturers [84, 87]. The
first brute force approach is to increase the power of the equipment, which
means that more powerful RF sources in the 3–5 kW range and higher mass
flows are used together with improved cooling systems. Process control is
improved by shorter gas delivery and pumping lines, together with faster mass
flow controllers and pulsed RF sources. End users do not have much control of
these changes other than adapting to the situation. The etching non-idealities
discussed in this thesis confound the results and complicate the device design.

The poorly understood non-idealities and new requirements for higher aspect ratios and etch rates place both process and equipment designers in a very challenging position. The possibility for real-time measurement of etch rates and end-point detection techniques could help in alleviating problems caused by various non-uniformities and over-etching.

There are also emerging plasmaless silicon etch technologies for micromachining, like neutral beam etching using F atoms [88] and isotropic vapor phase etching using XeF_2 [89]. These might replace plasma etching in some applications where for example charging has to be avoided and where isotropic etching is acceptable.

4. SOI process development and process integration

During wafer processing both the films and structures have to withstand extreme conditions. Patterning of one material may be detrimental to other materials. High temperatures used for diffusion of dopants and thermal oxidation of silicon can harmfully melt or alter some of the structures or their properties, especially metal films on wafer surface. Therefore the fabrication process, even for simple structures, has to be designed carefully to avoid all pitfalls, some of them non-evident. This chapter describes process steps developed for or utilized in SOI device fabrication. A simplified fabrication procedure is depicted below in Figure 16.
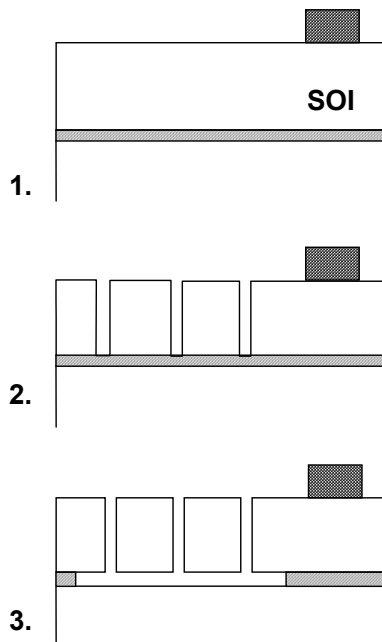

Figure 16. Simple SOI device fabrication procedure: 1) patterned metal conductor on SOI, 2) structure layer etching by DRIE, 3) release of structure by sacrificial layer etching.

4.1 Substrate contacts

The simple structure of Figure 16 is in many cases not good enough. Some kind of electrical contact to the substrate from the top surface is usually needed for enabling wafer probing or easier encapsulation without backside contact. This helps in reducing the effects of temperature and stray capacitances by grounding the substrate. Forming of the contact hole through the BOX requires an access hole through the overlaying structure layer, which requires an extra lithography and deep silicon etch step.

Substrate contact is fabricated by etching a narrow trench or small hole through the structure layer, followed by wet oxide etch to expose the handle wafer. After etching and cleaning, the contact hole is refilled with polysilicon. Undoped polysilicon can be used if the thermal budget is large enough for diffusion of the dopants from single crystal regions to poly plug. In-situ boron doped polysilicon is convenient for very low resistance contacts, but the final etch-back of heavily doped polysilicon film with RIE is not as easy as etching of undoped polysilicon. This kind of contact, while not too elegant, provides a sufficiently low contact resistance (in the range tens of Ohms) for the majority of MEMS applications.

4.2 Metallization and conductors

The major problem with SOI or surface micromachining is the fact that standard aluminum films that are typically used for conductors and bond pads are not inert to hydrofluoric acid (HF) containing silicon dioxide etchants. Silicon dioxide is the most popular material for sacrificial layers and it is usually etched with either buffered HF or concentrated HF. Though HF is not a particularly strong acid, it is in many ways inconvenient, mainly for safety reasons. HF does not directly etch metals very aggressively, but it will attack the native oxide at the interface of metallic conductor films and silicon, which can cause delamination of the metal films. Aluminum is rather tolerant to HF itself, but the water-diluted HF etches aluminum. The property that pure or 70% HF does not etch aluminum is utilized and reported elsewhere [90, 91, 92]. One could use noble metals like gold instead of aluminum if contamination by noble metals were not an issue in the fabrication line. In the standard CMOS line, the use of gold is not an acceptable solution.

Our approach has been to protect the aluminum film by a thin (100 nm) molybdenum film sputtered over the aluminum without breaking the vacuum. That scheme proved to be successful. Molybdenum is tolerant against HF [93] and etching the metal stack is straightforward, as the molybdenum is readily etched in the same chlorine based plasmas as aluminum and in wet aluminum etchants.

The protective molybdenum layer can be left on bond pads and it is a possible wire bond through the molybdenum layer. However, in some cases it is essential to remove the molybdenum film. Because the molybdenum layer is not capable of protecting aluminum from horizontal etching, there remains an overhanging molybdenum film on the edges of aluminum patterns after etching, which can cause particulate problems in some devices. The molybdenum can be removed with a standard aluminum wet etchant. However, there is no selectivity between etching molybdenum and aluminum with phosphoric acid-based wet aluminum etch. The etching should be timed, which leads process control problems. The best solution so far has been to use aqueous ozone to remove the molybdenum film. Aqueous ozone is a new method for resist removal. The resist can be stripped at a rate of about 100 nm/min with ozone concentration in the range of 100 ppm. It also etches molybdenum with an etch rate of about 7 nm/min at a temperature of 5°C, which is acceptable for this purpose because the rinsing cycles take about the same time. The molybdenum etch rate is dependent on etchable pattern size; large patterns are etched more slowly than narrow ones. Aluminum oxidation by ozone is negligible at this temperature [94, 95]. The aqueous ozone step also works as an effective rinsing step. Molybdenum removal is done after HF etching and before the release drying process. The resulting metal bonding pads are shown in Figure 17, which compares the overhanging molybdenum and the pads after molybdenum etching. The molybdenum layer protects the pads effectively and aqueous ozone has proved to be a suitable method for removing the molybdenum layer.
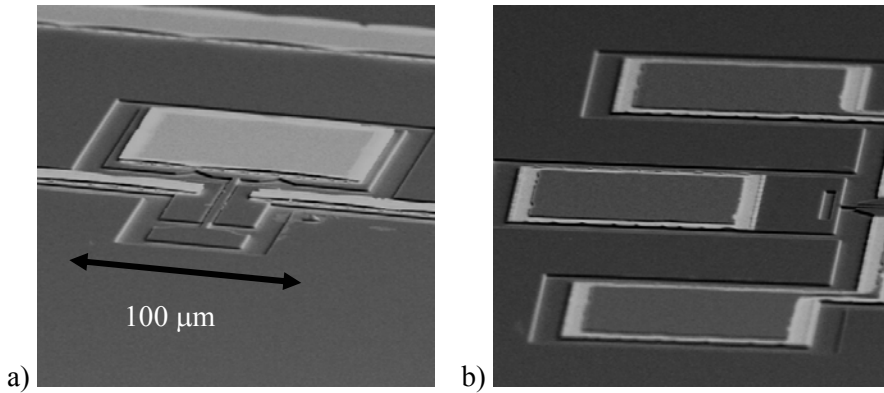
Figure 17. Bonding pads after release etching: a) without molybdenum etching, b) molybdenum etched with aqueous ozone.

A minor problem in plasma etching of aluminum against silicon is unwanted silicon etching: a thin layer of silicon is etched during the over-etch phase by chlorine used to etch aluminum or CF_4 used in TiW etching. Usually in IC fabrication metal etching is done against oxide, not silicon, and this problem does not exist. The loss of silicon layer thickness is not significant, but the smoothness of the silicon surface is compromised.

4.3 Structure layer patterning

The structure layer thickness used in this work is usually less than 20 microns. The structure layer is easily etched with a photoresist mask; no oxide or metal hard masking is required for typical structure layer thickness. In practice, the undercut typical of the Bosch process can be controlled better without a hard mask, because oxide mask etching may cause worse undercut than etching silicon with a resist mask only. The typical etch rate of structure layers of thickness 10–20 microns is 1–2 μm/min depending on other requirements on the etching profile. The smoother the sidewall the lower the etch rate is.

If submicron trenches and large features are required at the same time, extra care is needed to avoid notching and grass formation. Grass, or black silicon, is caused by micromasking when the equilibrium of passivation and etching in highly anisotropic etching is lost. In that case sharp spikes are formed on the

bottom of the etched trench. The thus roughened surface absorbs the incoming light effectively and the surface looks black.

When etching narrow trenches, the most difficult task is to limit horizontal etching at the mask opening to reduce the undercut. Use of photoresist as a mask is preferred over oxide mask because the high sidewalls of resist patterns, compared to a typical thin oxide mask, can effectively restrict the angular distribution of incoming ion flux, which helps reduce the mask undercut, and it is easier to use resist only, as there is then no need for mask oxide deposition and etching.

Because the requirements change in the course of etching, a multistep etch is used. As a first step a continuous mode, non-cycled RIE, is used to etch the upper part of the trench with minimal undercut. In the start step a C_4F_8 flow of about 30% of total gas flow is added to SF_6 to help in passivation of the sidewalls. Figure 18a shows the scallops and undercut of the switched process. In Figure 18b the undercut is almost eliminated by using continuous etching.

In the main part of etch parameter ramping [70], gradual changing of etch parameters is used. Typical parameters that are ramped are gas flows, which are reduced to achieve lower pressure, and platen power, which is increased to improve ion penetration into the etched trench of higher aspect ratio.

The last step of the etching process is done with LF bias to reduce notching at the oxide interface. Optimally, LF bias should be used only during the over-etch period. Without an end-point detection system, monitor wafers and process timing is used. Aspect ratios of 25:1 have been obtained for trenches of 0.5 μm nominal line widths as shown in Figure 19a.

Obtaining submicron trenches with very high aspect ratios (>20:1) reproducibly is difficult; other methods of fabrication narrow gaps have been attempted. One such method is to etch a wider trench of known width, then deposit a thin conformal polysilicon liner layer and etch the polysilicon from horizontal surfaces including the trench bottom. The resulting trench is then narrowed by the polysilicon layer liner inside the original trench. The result of such a process is shown in Figure 19b. The polysilicon etchback has opened the trench bottom as desired, but there is unwanted widening at the top because of ARDE and over-etching. We have not been able to utilize this procedure in practice because

of etching difficulties in plasma etching polysilicon sidewalls; though the trench bottoms are nicely etched, in some parts of the device all of the polysilicon should be etched, and our etch tools were not capable of performing single crystal structure layer etching and polysilicon sidewall etching simultaneously.
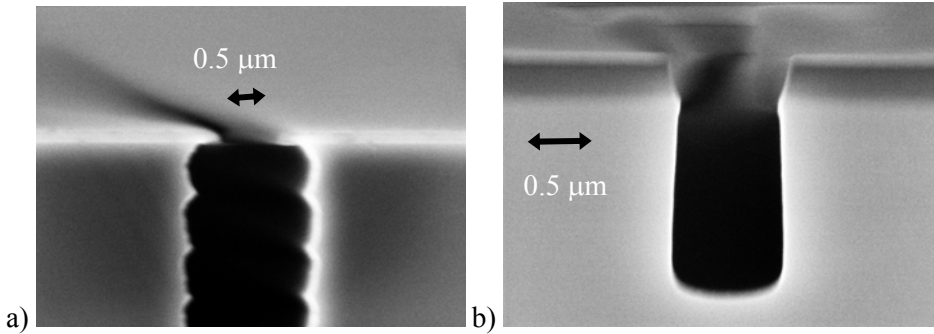

Figure 18. 0.5 μm trench etching: a) upper part of trench with switched process, large undercut with about 200 nm oxide mask; b) result with continuous mode start step, photoresist on top of oxide mask, no undercut.
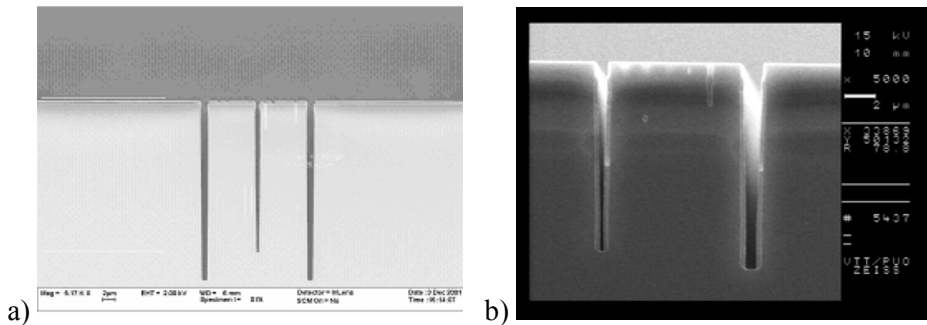

Figure 19. a) 25:1 aspect ratios are obtained for a 0.5 μm trench with a three step process, b) gap narrowing by conformal polysilicon liner: result after liner bottom etching.

4.4 Sacrificial layer etching

The buried thermal oxide of the SOI structure is rapidly etched with concentrated HF. The bulk etch rate of thermal oxide in 49% HF is 1763 nm/min

according to Kim et al. [93]. The etch rate of the buried oxide layer is different from the etch rate of bulk oxide. It varies from lot to lot but is independent of the geometry as shown in Figure 20. The apparent etch rate variation with structure layer thickness in Figure 20 is caused by variation between wafer manufacturing lots. True aspect ratio dependency would be visible in each curve of the figure if there were such a variation.
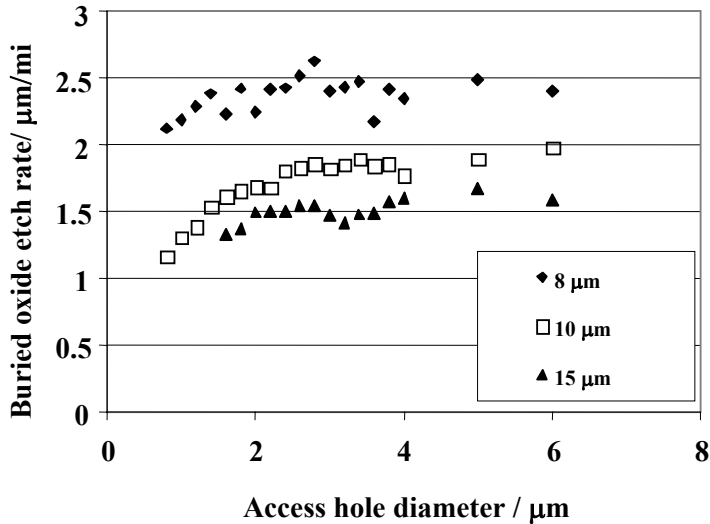

Figure 20. Average etch rate of buried oxide as a function of etch access hole diameter; the etched samples have different structure layer thickness.

The etch rate and its variation are governed by the etch rate of the bonded interface [96]. The stronger the bond the lower the etch rate is. Figure 21 depicts the dependence of etch rate of the SOI structure layer on bond strength. An etch time of 10 minutes and oxide thickness of 1 μm was used in all samples. The samples were bonded with varying activation and annealing procedures. Etch distance was taken from a SEM micrograph and surface energy was obtained with a crack opening method [16]. The data points are scattered but the trend is clear. When the bond strength is high, the etch rate approaches the etch rate of bulk oxide. A high bond strength interface is desirable for getting reproducible etching results, though there is a temptation to use structures with higher etch rate to reduce the HF etch time. The examples of buried oxide etch profiles are shown in Figure 22; the angle of the oxide edge is related to bond strength and oxide etch rate.
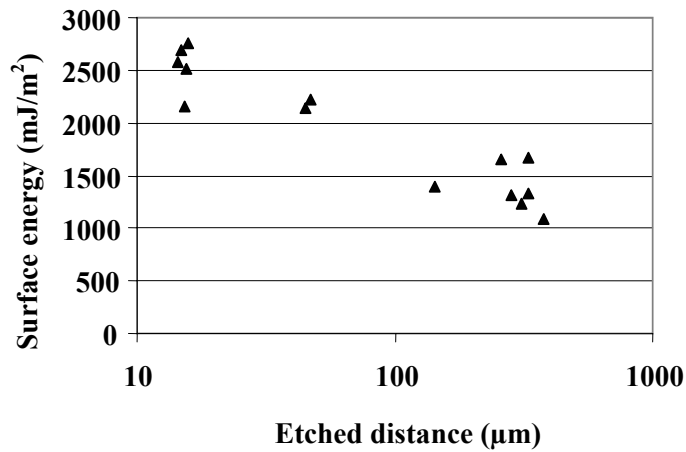
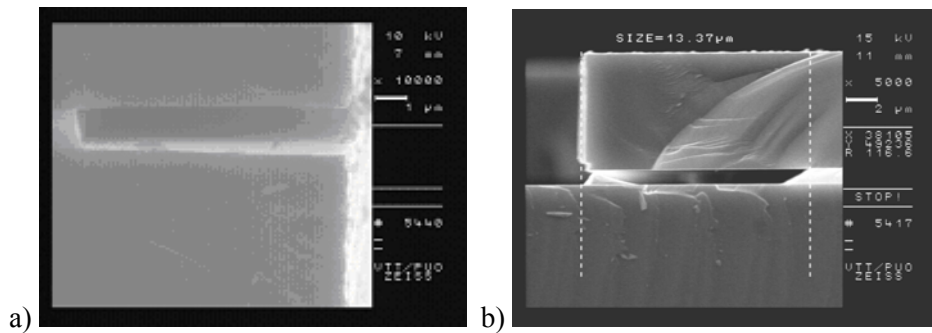*Figure 21. Bond strength vs. etch length, picture by T. Suni.*

Figure 22. SOI buried oxide etch profiles: a) very good bond strength with nearly vertical oxide edge, b) typical etch profile with tilted oxide edge.

The etch length in most of the devices in this work is designed to be five micrometers. The approximated time needed to etch 5 microns of thermal oxide is 4 minutes. Structures narrower than 10 micrometers are then released, because releasing of larger structure arrays of etch access hole is used to cover the area to be released. An array with 10 micron maximum spacing between etch holes is used; if the number of etch holes is an issue, a trigonal array which minimizes the number of holes is used instead.

4.5 Stiction and release drying

The term stiction refers to unintended sticking of moving structures. The devices are prone to stiction during drying after sacrificial layer etching. The wafer cannot be air dried because the surface tension of the liquid will pull the MEMS air bridges down [97]. Therefore a critical point drying system is used to release the MEMS air bridges [98]. The de-ionized water is replaced by isopropanol prior to the drying process, then the isopropanol is displaced by liquid CO_2 as part of the drying process. The chamber is then heated past the CO_2 supercritical point, and the pressure released. The supercritical CO_2 has no surface tension, and as a result the structures are not pulled down during the transition from supercritical fluid to the gas phase. Thus the liquid-to-gas transition interface that creates the meniscus problem is completely avoided.

Other promising process techniques have been developed for reducing or eliminating stiction [99]. A related technique to avoid the formation of a meniscus is the freeze-sublimation technique in which the release etchant is displaced by water and then by an organic solvent like tert-butanol with a high freezing temperature. The wafer with solvent is cooled until the solvent is frozen. The pressure is then dropped to vacuum levels, and the frozen solvent sublimes. In our experience the supercritical drying is superior to the sublimation technique. It produces cleaner devices with better reproducibility. In a new release method, flash release [100], the liquid is rapidly heated and vaporized. That method is not suitable for membrane type devices.

Other ways to avoid stiction include hydrophobic surface coatings [4] and dry etching with HF vapor, possibly together with methanol [101]. Matsumoto et al. [92] modified the sacrificial layer etching so that surfaces were anodized during the process. The increased roughness reduced the contact surface area and the risk of stiction.

The techniques described above avoid stiction during drying, but stiction can still be a problem during the operation of actuated MEMS. If shock, electrostatic discharge, or some other stimulus causes individual MEMS components to touch either each other or the substrate, they may become stuck. In these cases, surface treatments are needed to change the energy state of the surfaces.

After etching and drying the release result is inspected with an infrared microscope. The etch fronts are clearly seen with a near-IR camera [Paper III]. If the etch time used is not optimal, then the etch time of the next wafer can be adjusted accordingly. A detail of an etched structure is shown in Figure 23. The optical focus is on the level of the bottom surface of the structure layer, which reveals the etch front clearly and in some cases the notching also. By changing the focus it is in some cases possible to detect the difference in the etch front propagation between the bonded and the thermally oxidized interfaces.
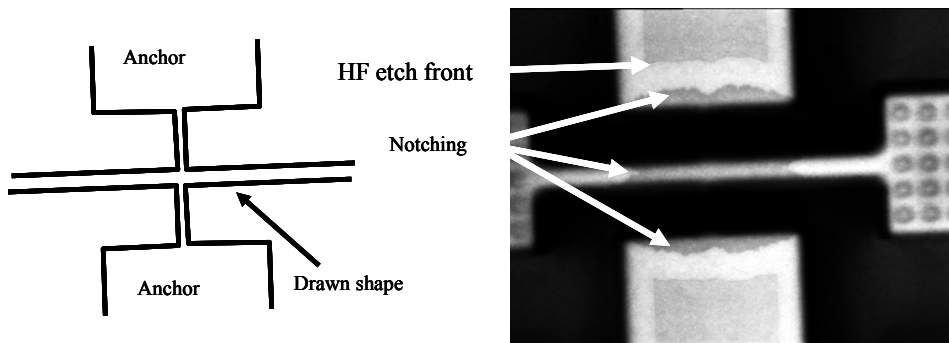

Figure 23. Example of notching seen with an IR microscope.

Besides the etch length, other details are revealed with an IR microscope. A comparison between successful and defective release etch results is shown in Figure 24. If the etching does not start at all, the reason may be insufficient cleaning after trench etching. The polymeric passivation layer residues can inhibit the wetting of narrow trenches. Also in very narrow trenches the etch time may not be long enough to clear the bottom of the trench or the etch depth may not even reach the BOX layer, which can explain the small decrease of the oxide etch rate through the smallest etch holes in Figure 20.

A high-resolution alternative to a simple IR microscope setup is a scanning IR microscope (SIRM). The SIRM offers better resolution compared to a video camera. An example of a SIRM measurement result is shown in Figure 25, with a scanning laser wavelength of 980 nm.
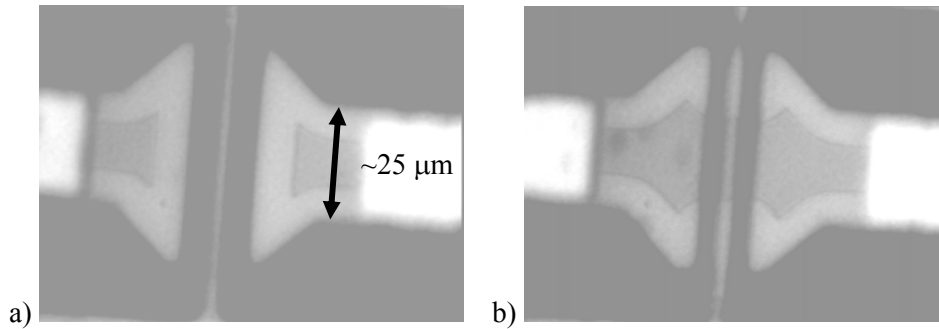
Figure 24. IR photographs of released clamped-clamped beam resonators: a) successfully released beam and electrodes, b) a result of failed release etch.
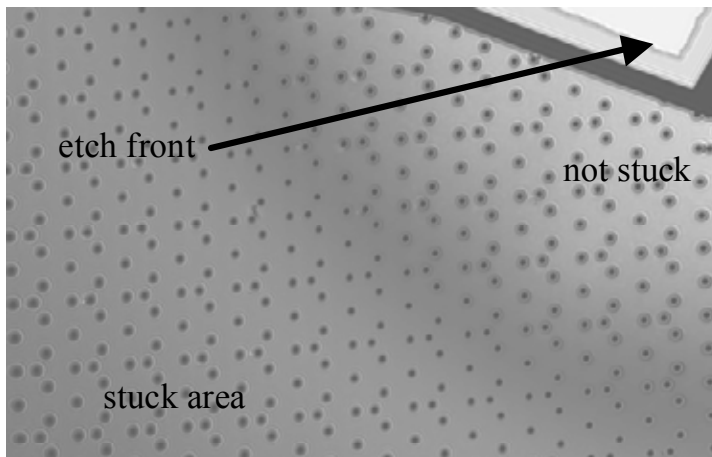

Figure 25. Details of acoustic emission sensor suffering from stiction visualized by SIRM. The HF etch front, stuck and non-stuck areas are revealed. Even the notching around etch access holes is seen. (Picture courtesy of Petteri Kilpinen and Eero Haimi, Helsinki University of Technology, Laboratory of Metallurgy).

4.6 Dicing

Dicing of MEMS devices is a major problem without a satisfactory solution. The solutions used in this work can be applied only to prototyping, where the unit assembly cost is not an issue.

Two methods for separating chips have been used. The first method is to saw the wafer half way before sacrificial etching and then cleaving of the wafer. This method is not suitable if small gaps are required, because silicon dust is generated during dicing. Moreover, this is not a particularly clean method and its use in a clean room environment is restricted.

The second method is to plasma-etch dicing trenches about halfway from the backside and then cleave the chips after sacrificial etching and drying. This method is better suited to a clean room environment. Additionally the chip shape is not restricted to orthogonal shapes or by crystal orientation, and it may be possible to dice the wafer totally before sacrificial etching if a suitable holder or dicing tape is applicable for sacrificial etching and drying steps.

4.7 Plug-up process

In view of the limitations in HF etching of metallized structures, another way to perform sacrificial layer etching was sought. However, simple reversal of the processing order to perform the etching before metallization is not viable, because it is not possible to perform the subsequent lithography over high aspect ratio structures. Thus, a way to temporarily planarize the surface after sacrificial layer etching was contemplated. The puzzle was solved by invention of the following sequence called "Plug-Up". The process is described in Paper V and elsewhere [102]. The Plug-up sequence is schematically presented in Figure 26.
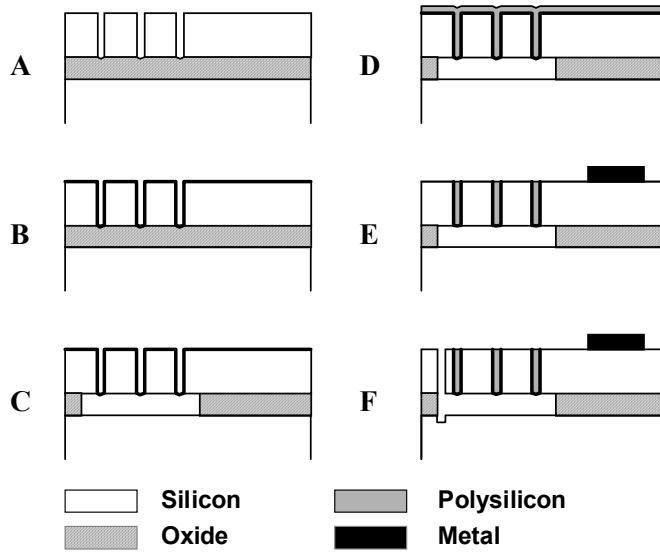
Figure 26. Plug-up sequence: a) formation of the etch hole array, b) deposition of the semi-permeable polysilicon film, c) sacrificial layer etching, d) sealing of the cavity by polysilicon deposition, e) etch-back and conductor patterning, f) optional dry release of moving structures.

The starting material is bonded SOI with a 5–20 μm thick structure layer and 1–2 μm thick buried oxide. After defining the air gap area, its interior is patterned with an array of 1–2 μm wide circular or square-shaped dots. These are replicated into the device layer of SOI by deep silicon etching using ICP. Optionally a HF dip, which attacks the buried oxide slightly, forms small holes for anti-stiction bumps, as seen in Figure 26a. A thin layer of polysilicon is then deposited using the LPCVD technique by controlling the deposition parameters in such a way that the film contains a controlled density of nanometer-scale pinholes [103] as seen in Figure 26b. The areal density of the pinholes must exceed $1/\mu m^2$ in the used geometry; at least one pinhole is needed inside each etch access hole. Immersion of the wafer in HF results in local removal of the buried oxide around the etched holes (Figure 26c). After careful rinsing and drying, pinhole-free polysilicon is deposited over the wafer to completely plug up the holes (Figure 26d). The pressure inside the cavity remains in the 100 Pa range similar to the deposition process pressure. After etch-back (Figure 26e), the cavity wafer is rigid, identical to standard SOI wafers from the fabrication point of view, and a wide variety of processing steps can be performed on it

without difficulty, including any standard metallization. Some device types like pressure sensors or ultrasonic transducers do not require further processing after this, while other applications may still call for relief of laterally moving resonators, comb electrodes or other features. Such a release step can now be made with high-yield dry processing, as shown in Figure 26f.

The Plug-up sequence makes use of liquid-permeable polysilicon to form a cavity. Vacuum shells have earlier been studied for making a wafer level vacuum environment for improving the resonator Q value or for protecting micromechanical devices from the environment [104]. The sacrificial layer is usually removed via lithographically patterned etch holes [105] or via permeable polysilicon [106]. The permeable polysilicon is a thin layer of LPCVD polysilicon, which contains pinholes with a diameter of the order of ten nanometers formed spontaneously during deposition. If a thicker layer of same material is deposited the pinholes are closed and a continuous film is obtained. One of the first applications of permeable silicon was the fabrication of a hollow beam resonator [107]; it was found that deposited oxide sandwiched between silicon layers was etched by HF during sacrificial layer etching. The process window for depositing permeable film is rather narrow. The film properties can be tuned by silane flow, deposition temperature and pressure. The properties and processing of permeable polysilicon is reviewed by Dougherty et al. [108, 109]. The permeable polysilicon can be applied to sealing of capacitive surface micromachined ultrasonics transducers [103].

Before closing the cavity it is important to be able to inspect the etching results and to be able to control the properties of the polysilicon film. IR microscopy suits this purpose, but the image is not as clear as with finished cavities, because the polysilicon closing layer scatters the light. IC-compatibility must be preserved throughout the release and drying process. We have chosen to use supercritical CO_2 for drying the cavities because of its cleanliness, although the cavities can probably be dried with other methods also. IR microscope images of fabricated cavities are shown in Figure 27; from the resulting interference patterns it is very easy to detect whether the cavity closing was successful. The vacuum of the device in 27b was intentionally broken by a dry-etched vent hole.

A slightly similar closing process to plug-up was proposed by Benitez et al. [110]. In their approach a sputtered aluminum film was used to close the

structures; no polysilicon layer was needed, because aluminum sputtering is a non-conformal process and aluminum does not enter the cavity. Also in their approach the order of sacrificial etching and metallization was reversed. Armbruster et al. [111] presented a method based on electrochemical etching and recrystallization for forming similar-sized cavities on bulk silicon. Such cavities, or the cover of the cavity, can be used as a spring in a pressure sensor, with deflection measured by a piezoresistor formed on silicon.
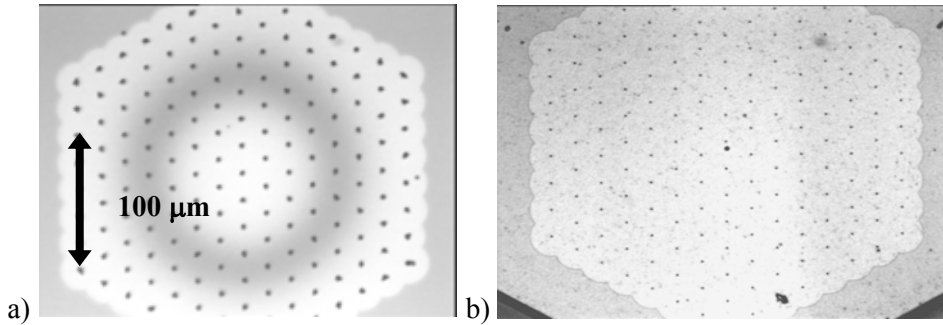

Figure 27. IR photographs of finished cavity structures: left) closed cavity, right) vented cavity.

The polysilicon plugs constitute only a minor portion of the structural material and the mechanical properties of the devices are determined mainly by the single crystal structure layer, which typically has very low internal stress. The size of the cavity is limited by the deflection caused by ambient pressure. The maximum deflection of the structure should be limited to the thickness of the buried oxide to avoid the structure touching the substrate. The thickness of the structure layer defines the maximum size of the cavity that does not touch the bottom at a given pressure. The deflection at the center of a circular plate is given by the following equation [112]:

$$\delta = \frac{3\,P\,r^4\,(1-v^2)}{16\,E\,t^3},$$

(3)

where P is the applied pressure, r is the radius of the cavity, v is the Poisson ratio, E is Young's modulus for the plate material, and t is the plate (structure layer) thickness. Because the sensitivity is proportional to the fourth power of the membrane radius and to the third power of layer thickness, the device

dimensions should be well controlled. The obtainable maximum diameter of the vacuum cavity for a given buried oxide thickness is plotted in Figure 28.
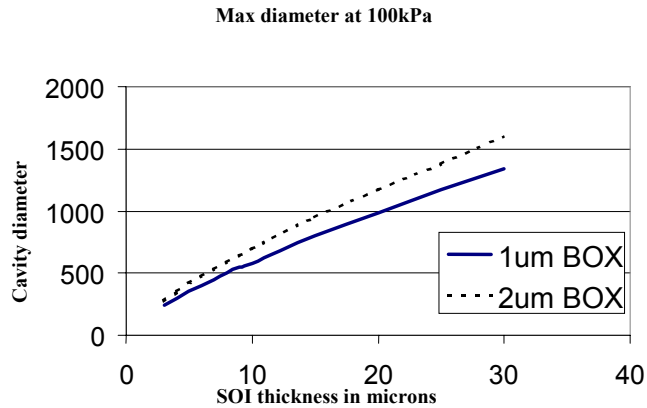

Max diameter at 100kPa

Figure 28. Maximum diameter of the vacuum cavity as a function of structure layer thickness (with 100-silicon Young's modulus of 130 GPa).

Notching is avoided when releasing the structure above the cavity, because there is no insulating layer that could be charged. The result is shown in the left part of Figure 29. There is no notching at the foot of the structure layer; the etching has been continued directly past the cavity. Polysilicon anti-stiction bumps can easily be formed on the bottom of the structure layer by slight over-etching into BOX while forming the perforation on the structure layer, as shown in Figure 29b.
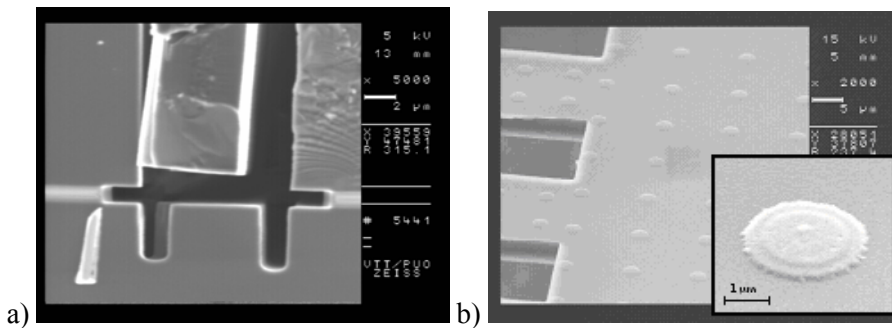

Figure 29. Some extra benefits of the plug-up process: a) elimination of notching in structure layer release etching, b) anti-stiction dimples are easily formed on the bottom surface of the released structures.

5. Device fabrication results

Three devices are presented in this chapter. Many other SOI devices have also been fabricated at VTT using the fabrication processes described in this thesis. These include various references for precision measurements. The chosen devices give an extensive view of the performance of the developed fabrication processes. Full device details or theoretical treatment of the device operation are not presented.

5.1 Acoustic emission sensor

We have fabricated prototypes of a micromechanical acoustic emission sensor (AES) [113]. Structural vibrations at frequencies over 40 kHz are called acoustic emission. Such vibrations can be generated e.g. by turbulent leak flow or by crack propagation in a damaged structure. Monitoring of acoustic emission of machinery and structures is an important tool for maintenance and online diagnostics. Micromechanical silicon sensors can offer advantages over the traditional piezoelectric sensor in miniaturization, integration with electronics and packaging. Our AE sensor is kind of a capacitive accelerometer. The piston-like movement of the proof mass is detected as a change in the sensor capacitance. Avoiding stiction in this kind of sensor is challenging due to the softness of the beams and relatively large released area of the design. The chip contains different sensors with resonance frequencies equally distributed over the desired frequency band of 100–500 kHz. The released upper electrodes of all sensors have a diameter of 360 μm and are supported by three radial beams located symmetrically at 120° angles, as illustrated in Figure 30. These beams act as vertical springs. The resonance frequencies of the sensors are adjusted by chancing spring lengths. Because the etch holes in the springs and plate have a strong effect on the spring constant, FEM calculations were used for the final design. We found that drying with supercritical CO_2 is necessary for obtaining working samples, especially devices at the lower end of the frequency band. The Q value of the mechanical resonance is limited by viscous damping in the air gap and in the perforation holes. Q values of 60 were achieved with devices in which the etch access holes formed a triangular lattice with 18 μm nearest-neighbor spacing. The diameters of the perforation holes were 4 μm in the springs and 12 μm in the plates. Avoidance of notching during the etch access

hole etching is important for keeping the sensor capacitance at the desired level. Excessive notching can reduce the capacitor surface and increase the dielectric gap between the moving structure and the substrate. The timing of etching is critical when multiple hole diameters are etched simultaneously.
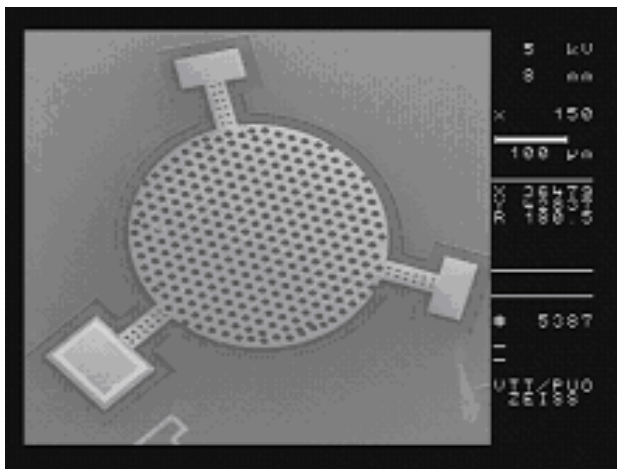

Figure 30. A piston mode resonator used as an acoustic emission sensor.

5.2 Micromechanical resonators

Silicon resonators have received a lot of attention as an important emerging application of MEMS. The resonators have been studied for constructing filters [114] and oscillators [115]. Our work with resonators focuses on studying the possibilities of replacing bulky quartz crystal oscillators with a miniaturized oscillator constructed of single crystal silicon. Though this miniaturization sounds simple, it is difficult to achieve a resonator with a high enough signal-to-noise ratio with a small vibrating mass [116]. Our first published design was the bridge resonator shown in Figure 31 [117]. The operation was based on electrostatic force bending the clamped-clamped beam. The spring coefficient and the resonator mass in this design are relatively low and the amount of mechanical energy that can be stored in the resonance is too low for achieving the high signal-to-noise ratio required for reference oscillators. An improvement to this situation is to use a different resonator configuration. By using a length extensional resonator or bulk acoustic wave (BAW) mode resonator [118],

where the silicon beam is stretched instead of being bent, it is possible to increase the amount of stored mechanical energy and thus to improve the signal-to-noise ratio. A picture of such a resonator is shown in Figure 32a. The amount of energy stored and the drive capacitance of such a resonator are still not large enough. Further improvement can be achieved by extending the movement in two dimensions, which can be thought as a parallelization of resonators. The resulting square extensional (SE) resonator [Paper IV] is depicted in Figure 32b. The figures representing the typical performance in this frequency range for these three types of resonators is tabulated in Table 4.
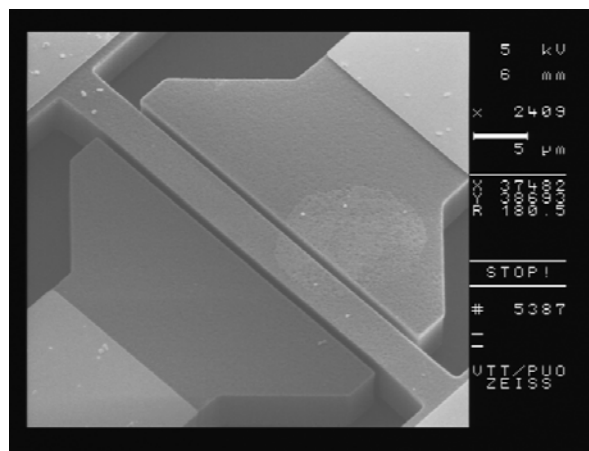

Figure 31. Clamped-clamped beam (bridge) resonator [117].
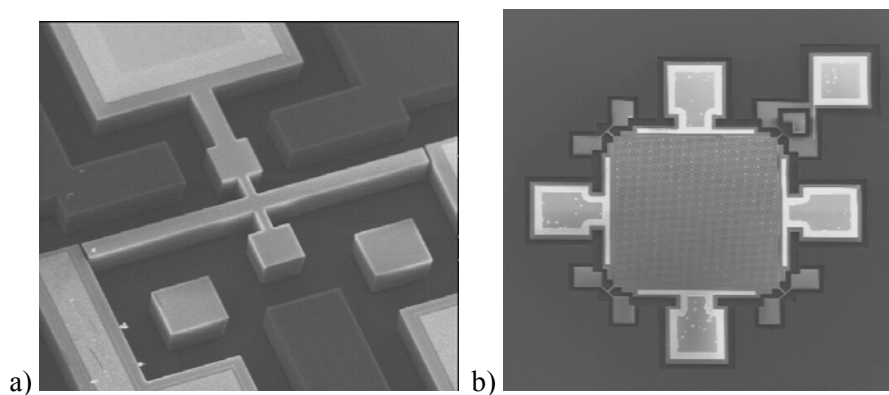

a)   b)

Figure 32. Silicon resonators: a) length extensional resonator [118], b) square extensional resonator [Paper IV].

The large size of the square extensional resonator makes it the strongest alternative for use in reference oscillators. The square extensional resonator exhibits much lower input impedance and higher energy storage compared with the bridge or one-dimensional length extensional resonator. The operation frequency of a length extensional resonator is defined by the length of the device and material properties according to the following equation:

$$f_r \approx \sqrt{E/\rho}/4L,\tag{4}$$

where E is Young's modulus, ρ is the density of the resonator material and L is the length of the resonating arm. The dc bias and the drive signal excite a sound wave in the structure; at the resonance frequency a standing wave is formed in the structure and because the supporting points are loosely coupled, or located at the nodal positions, the mechanical losses are very low.

In MEMS devices the electric signals are converted into mechanical motion and vice versa by an electrostatic transducer. A key process challenge in fabrication of electrostatically driven devices is miniaturization of the drive gap. The importance of drive gap minimization [118, 119] can be seen in the following equation of resonator motional current in a linear case

$$\hat{i}_{m,R} = Q\frac{\eta^2 \hat{u}_{ac}\omega}{k} \approx Q\frac{U_{DC}^2 \hat{u}_{ac}\omega C_0^2}{kd^2},\tag{5}$$

where Q is the mechanical quality factor of the resonator, η the electromechanical coupling factor, k the spring constant, $\hat{u}_{ac}$, the ac drive voltage, U_{DC} the bias voltage, and ω the angular frequency.

The drive gap width d has a very strong effect on the motional current, because its square is in the denominator of the above equation and it is also hidden in the work capacitance C_0. Reduction of the drive gap increases the motional current and allows one to use lower bias voltage to achieve similar resonator performance. The gap reduction helps in achieving a suitable impedance level for noise matching of the transducer and readout electronics.

Table 4. Performance comparison of different resonator types.

	Flexural [117]	BAW [118]	SE-BAW [Paper IV]
Size (width, length, height μm)	4, 44, 10	10, 320, 10	320, 320, 10
Q value	1500	180 000	130 000
Gap Coupling capacitance	- 4 fF	1.02 μm 0.69 fF	0.75 μm 140 fF
Motional capacitance	8 aF	0.05 aF	20.8 aF
Motional resistance	1 MΩ	1.49 MΩ	4.47 kΩ
Mass	1.62 ng	16.8 ng	2.39 μg
Maximum stored energy at nonlinear limit, data from ref. [119]	0.026 nJ, (length = 52 μm)	2.6 nJ	180 nJ
Noise floor	-105 dBc	-115 dBc	-138 dBc

During a semiconductor equipment assessment project, Microspect, the performance of a new etch tool was evaluated in narrow trench etching for resonator fabrication [83]. It became very clear that notch reduction is essential for obtaining high quality resonators. If notching was not reduced with LF bias there was severe notching and a coinciding decrease of the resonator Q value. In samples where notch reduction was used, the Q value remained high. The fitted parameter for narrow trench width (the electrostatic drive gap) was lower for the case without notching, though according the SEM images the physical trench width was lower in devices fabricated without LF bias. The results of notch elimination are summarised in Table 5.

Table 5. Effect of notching on the Q value of 20 μm thick resonators.

	No LF	With LF
Q value	40 000	150 000
Gap	2.0	1.15
Notching	Yes	No, 30% over etch

Promising results with new resonator designs and fabrication have already been achieved but two critical questions still remain to be solved: How to achieve the long-term stability and temperature stability required for reference oscillators is

still an open question [120]. Vacuum encapsulation and temperature compensation are probably both needed. For economic reasons, vacuum encapsulation should be a wafer-level solution. For temperature compensation a monolithically integrated solution with in-situ temperature measurement sounds tempting, but there are still a lot of economic and technical issues to be solved before commercialization of silicon microfabricated reference oscillators.

5.3 SOI ultrasonic transducers

Ultrasonic transducers were fabricated with the plug-up process. The starting material was SOI with an 8 μm thick structure layer. The test samples were hexagonal cavities with a roughly 300 μm diameter formed of trigonal arrays of etch holes (Figure 33).
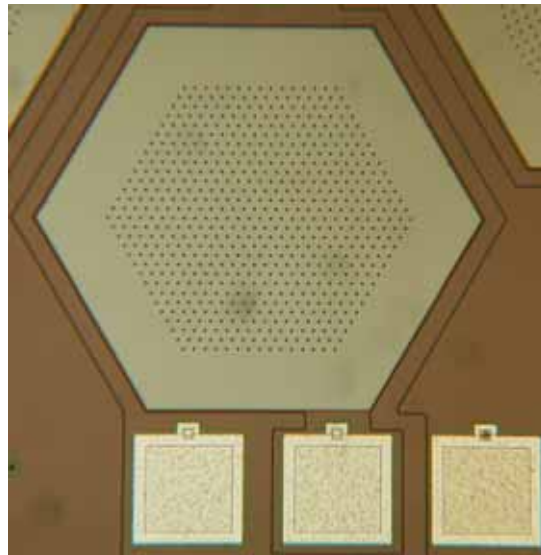

Figure 33. Photograph of a hexagonal micromechanical cavity resonator.

The etch hole diameter and their spacing were used as design variables. The typical etch hole diameter was 1.0 micrometers and the separations varied from 10 to 70 micrometers. All design parameters do not yield functional devices within a single wafer, as the etch length of the sacrificial etch is an important factor in determining the device operation. The cavity structures were electrically isolated from the structure layer by trench isolation. Instead of a single trench a double trench was used. The double trench configuration enables

guarding of sensor capacitance during the measurements. The trenches were refilled by deposited oxide to improve the isolation and allow the metal conductors to cross over the trenches.

The frequency response of a hexagonal resonator with the bias voltage as a parameter is shown in Figure 34. The resonance frequency is given by the following equation:

$$\omega = \omega_0 \sqrt{1 - \frac{k_e}{k_m}} = \omega_0 \sqrt{1 - \frac{2C_w^0 U_{DC}^2}{k_m d^2}} \ ,$$ (6)

where k_e and k_m are the electrical and mechanical spring constants, respectively, ω_0 is the nonbiased angular frequency at resonance, C_W is the working capacitance of the electrostatic transducer, U_{DC} is the applied static bias voltage and d is the electrostatic drive gap. Besides the expected frequency shift by spring softening induced by the bias voltage, the measured signal level is also increased as the capacitance of the structure increases when the static voltage is increased, as shown in Figure 34.
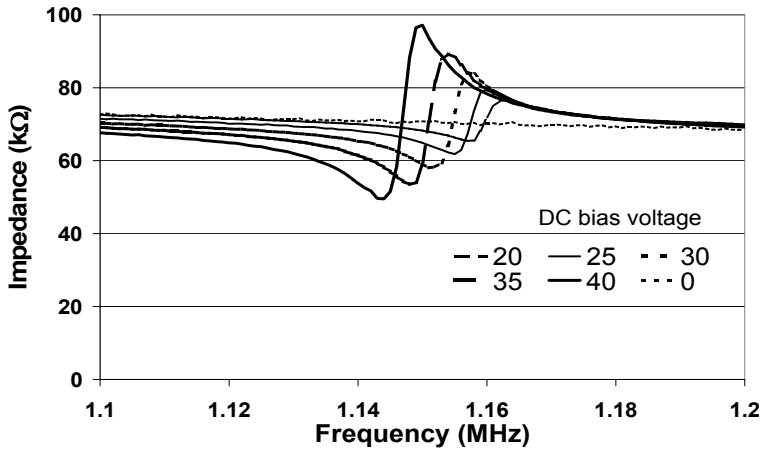

Figure 34. Spring softening effect.

The temperature sensitivity of the resonance frequency of the silicon membrane is governed by the temperature sensitivity of Young's modulus of silicon. The approximate Q value of such a resonator is in the range of hundreds when

operated at atmospheric pressure [121]. In a vacuum the Q value is in the range of one thousand. The mechanical losses are due to energy leakage at the edge of the device, where the membrane is connected to the surroundings.

The mechanical movement of the film can be measured and visualized by optically using a scanning Michelson interferometer [122]. Such a measurement was performed at the Material Physics Laboratory of Helsinki University of Technology. The measured relative amplitude of the motion in the z-direction at two different resonance frequencies is shown in Figure 35. (The measurement results of Figures 34 and 35 are not from the same device). The vibration patterns are symmetric at lower resonance modes; the higher modes show interesting modal shapes because of the hexagonal structure [123].
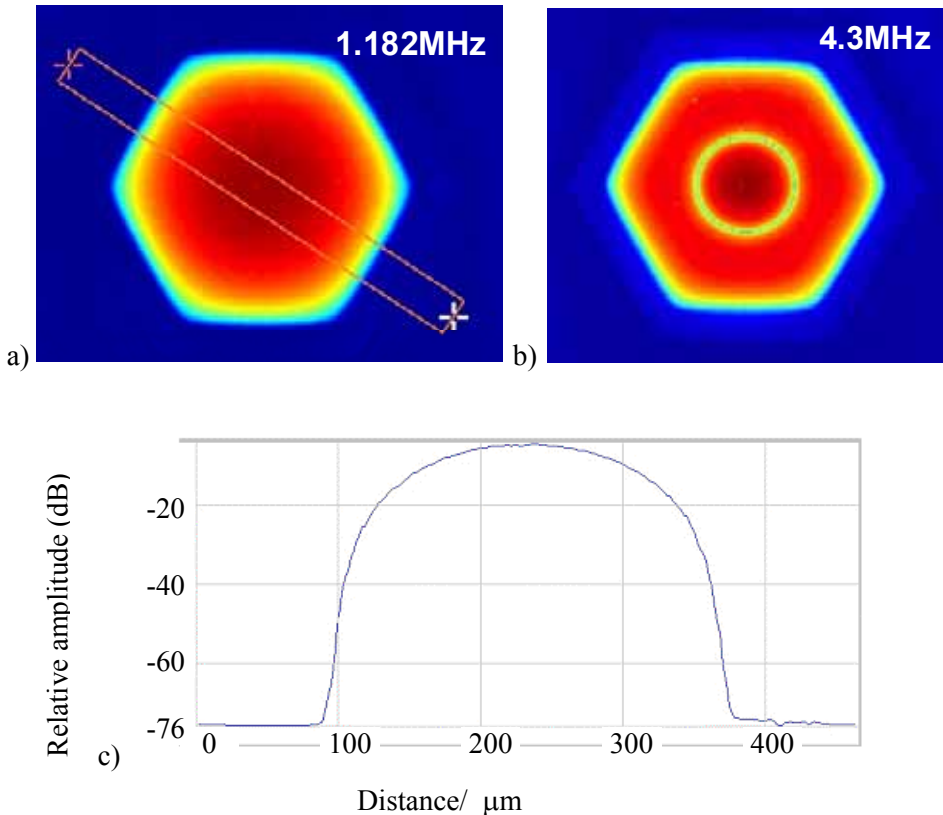

Figure 35. Basic radially symmetric resonance modes a) the first mode b) a higher mode c) relative movement of the film driven in the basic mode (picture courtesy of J. Knuuttila and O. Holmgren).

The resonator geometry has an effect on the resonance frequency; even small changes in the polysilicon plug diameter have a measurable effect [121]. The bigger the plugs, the softer the structure; the reduction in plug separation alters the resonance frequency in a similar way. The resonance frequency is very sensitive to small changes in device geometry, as shown in Figure 36.
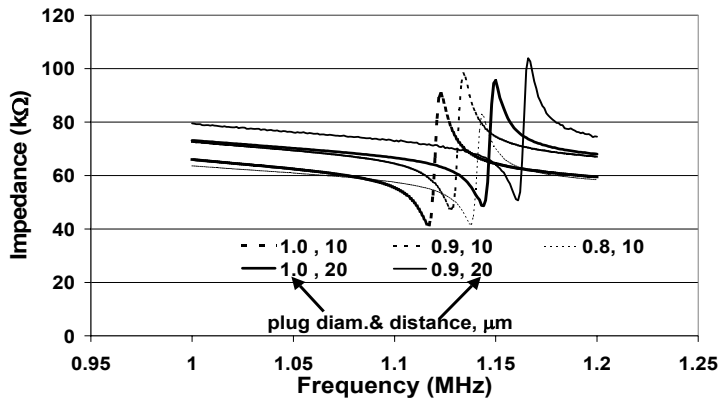

Figure 36. Effect of plug size and spacing on the resonance frequency of the cavity resonator [121].

5.4 Monolithic integration of SOI MEMS and ICs

As the plug-up process is IC compatible and the silicon surface after fabrication of the micromechanical parts is smooth single crystal silicon, it offers a possibility for modular monolithic integration of MEMS and circuitry [Paper VI]. The level of metallic impurities caused by the cavity-forming process remained at an acceptable level, verified by total reflection X-ray fluorescence (TXRF) measurement of test samples after deep silicon etching and super-critical carbon dioxide drying. Besides the plug-up cavities for micro-electromechanical devices, substrate contacts and isolation trenches are needed. Polysilicon plugs are used for substrate contacts. The DRIE etched isolation trenches are refilled with nitride and oxide after cavity formation, before integrated circuit processing. The added MEMS elements are depicted in Figure 37. During the micromechanical processing a stack of selected thin films protects the area designated for CMOS. The protection layer is needed during the polysilicon etch-back step only. The processing order of the main modules and their intended effects are tabulated in Table 6.

The integrated circuit process selected for this demonstration is nominally a 1.0 μm gate length bipolar enhanced CMOS. The BeCMOS process is optimized for analog and mixed-signal circuits. It uses a p-type substrate with a triple well. Besides the standard n- and p-wells the process has a deep n-well with a shallow p-well inside it. This structure is used for isolating analog NMOS transistors and vertical pnp transistors. An extra well was added to the MEMS region to enhance the conductivity of the structure layer. The higher doping level is needed to reduce the temperature and voltage sensitivity of the anchor area of MEMS devices. Tailoring of the structure layer doping profile by blanket implantation before wafer bonding was also used as an alternative to make the top electrode of the MEMS capacitor more conductive. The tailoring implant was the only step performed in SOI wafer fabrication that is not standard in BESOI wafer production.
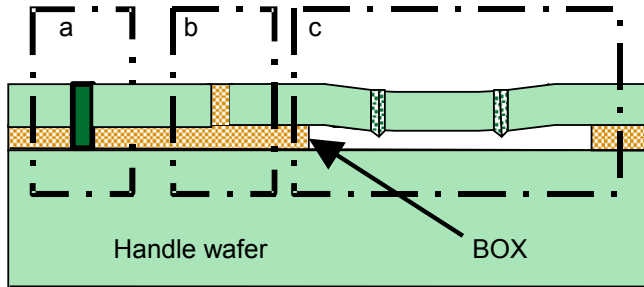

Figure 37. MEMS parts a) poly filled substrate contact, b) oxide/nitride filled isolation trench, c) vacuum cavity.

Table 6. Process modules and their main effects.

Module	MEMS	Integrated circuit
Plug-up	Cavity formation	Silicon surface under protection layers
Substrate contact	Bottom electrode contact	-
Isolation trench	Trench etch and insulator refill	Optional isolation trench formation
IC front end	Covered by field oxide	Active devices
Capacitors and thin film resistors	Covered by field oxide	Passive devices
Back end	Exposure of micromechanical silicon	Metallization and inter-level dielectrics deposition, passivation opening
Dry release	Optional release of horizontally moving structures	-

The bipolar transistors are processed before the CMOS gate process. Both npn and pnp transistors have a conventional triple-diffused structure with implanted emitters. The CMOS portion of the process uses a self-aligned molybdenum gate with 20 nm gate oxide. Molybdenum gate metal is also used as a bottom electrode for metal-insulator-metal capacitors. Stacked floating gate MOS transistors with capacitively connected control electrodes are used as EEPROM memory cells. The key parameters of the circuit elements are listed in Table 7. Most of the circuit elements are modular and can be omitted from the fabrication process if so desired. The high voltage NMOS is an important option if electrostatic drive of capacitive elements is required.

Table 7. List of processed circuit elements of the modular BeCMOS.

Element	Key parameters
NMOS	VTH = +0.60 V, molybdenum gate
PMOS	VTH = -0.65 V, molybdenum gate
Vertical npn	HFE ~ 100
Vertical pnp	HFE ~ 30, with deep n-well isolation
EEPROM memory cells	Floating NMOS/PMOS and capacitor
High voltage NMOS	Breakdown voltage 40 Volts [124]
Thin film capacitor	Metal-insulator-metal, 2 nF/mm^2
Thin film resistor	10 kΩ/sqr, TCR < 100 ppm/°C

Modular integration using the plug-up process was demonstrated in practice. The processed NMOS, PMOS, npn, and pnp operate similarly to reference devices on plain silicon wafers. The leakage currents remained practically unaltered below the breakdown voltage, so the MEMS process has no adverse effect on the IC process. The membranes within the MEMS regions are deflected downwards by ambient pressure, as was verified by profilometry and near infrared microscopy. They also resonate at the expected frequency and with the expected mechanical quality factor, which proves the ability to release structures to withstand the CMOS cycle. Photographs of two processed microsystems are shown in Figure 38.
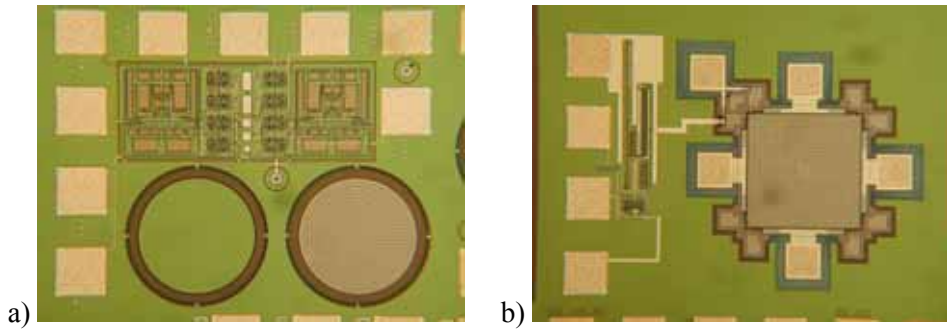
Figure 38. Photographs of monolithically integrated microsystems: a) pressure sensor, b) silicon resonator with pre-amplifier circuit.

The first application of this integration method was probably pressure sensing [125] because of the closed structure, which does not require dicing and encapsulation of open, released structures. Another interesting application is the micromechanical resonator, which could utilize the possibility of integration of a preamplifier and control electronics in the vicinity of the resonator, and thus enable good noise matching and a small size for oscillators.

6. Conclusions

The purpose of this work has been the development of new process technology and improvements of existing technology for micromachining of SOI wafers. The new process technology has been successfully employed in fabrication of various prototype devices in monolithic integration of MEMS and ICs.

Deep silicon etching using the Bosch process and its design dependent characteristics has been studied extensively. As a result of these studies a better understanding of ARDE and the capability to predict depths of etched patterns for a wide range of pattern shape and size, as well as the etch rate as a function of exposed area, has been attained.

The Knudsen flow of reactive fluorine species explains consistently most of the aspect ratio dependency of the etch rate. The validity of Mogab's loading effect model is shown for deep silicon etching. Elimination of many of the non-idealities of deep silicon etching is clearly possible, but it requires attention in device and process design. The interaction of different non-idealities can produce unforeseeable results.

With the simple SOI process, interesting demonstrator devices have been fabricated; especially single crystal resonators have provided much information on the challenges and possibilities of constructing frequency references of silicon with micromachining. A wide variety of optical methods was applied for visualization and inspection of processing results and fabricated devices. Especially near-IR microscopy was found to be indispensable to the process and device characterization of fabricated micromechanical SOI devices.

A novel micromachining process that avoids common HF etch related problems has been developed. The key advantage of the plug-up sequence is the fact that sacrificial oxide etching using HF is done prior to all metallization steps or gate dielectric growth. The interior of the closed cavity remains clean and the cavity is hermetically sealed by the deposited polysilicon film.

The complete analog BeCMOS was successfully processed on wafers having pre-processed plug-up vacuum cavities. The cavity formation by plug-up sequence was shown to be CMOS-compatible, though effort is still needed in the

development of sacrificial etching and super-critical carbon dioxide drying procedures. This method of MEMS/CMOS integration enables modular fabrication of MEMS systems and it can act as a versatile process platform for a vast range of applications.

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Appendix I

Deceleration of silicon etch rate at high aspect ratios

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The molecular-flow conductance of a high aspect ratio feature can limit the etching species arriving at the bottom of the feature and thus limit the etch rate. A simple conductance model can predict the etch rate of the time-domain multiplexed etch process with good results at moderate-aspect ratios (5–20) for trenches, but at very high aspect ratios ($>$20) the conductance model breaks down. Other mechanisms are needed to explain the deceleration of etch rate and almost complete etch stop. In this article the reasons for etch stop at the bottom of deep features are discussed. Measurement results of deep silicon etching are presented. Very deep holes and trenches were etched into silicon to study the effect of process parameters. At moderate aspect ratios the bottom of the hole is nearly flat and the sidewalls are vertical. At high aspect ratio the sidewalls start to bow and the feature bottom turns into a sharp spearhead. The shape of the feature can have an impact on the step coverage of the passivation layer deposition during the passivation step and on passivation removal during the etch step, leading to excessive sidewall etching and reduced etch rate at the feature bottom. The nonzero sidewall reaction probability and flow conductance of tapered tubes were studied by Monte Carlo simulation. The main reason for deceleration of etching seems to be the loss of etchant species due to sidewall reactions combined with feature closure by ion-limited passivation polymer etching. © *2000 American Vacuum Society.* [S0734-2101(00)07904-5]

I. INTRODUCTION

Time-domain multiplexed etching (Bosch process) has recently gained popularity in high aspect ratio silicon etching for microelectromechanical systems (MEMS). Fluorine-based inductively coupled plasmas (ICP) using the Bosch process[1] have been shown to achieve etch rates of 3–7 μm/min at room temperature.[2,3] The Bosch process involves both gas flow and bias power cycling. Etch directionality is achieved with a sidewall-protecting polymer layer, which is deposited during the C_4F_8 passivating cycle. Silicon etching proceeds during the SF_6 etch cycle. The passivation polymer is removed from horizontal surfaces by ion-enhanced etching, after which silicon is etched isotropically from exposed areas by free fluorine. Nearly vertical profiles ($90°\pm2°$) with simple photoresist or silicon dioxide masks can be achieved. Extensive presentations on etch parameter influences for resist masked processes have recently been published by Ayón and co-workers.[4,5]

Despite the merits of the Bosch process, some serious drawbacks exist such as aspect ratio-dependent etch rate and notching at the insulating etch stop layer. The aspect ratio-dependent etching (ARDE) is a serious limitation in deep silicon etching: at high aspect ratios excessive etch-rate reduction occurs with longer etch times.

ARDE in plasma etching has been attributed to a wide range of physical mechanisms. An excellent review of this topic has been published by Gottscho, Jurgensen, and Vitkavage.[6] Coburn and Winters[7] have introduced a simple conductance model based on Knudsen transport of particles in etched trenches, where the molecular-flow conductance limits the etching species arriving at the bottom of the feature. They derived the following equation for the ratio of the etch rate at the bottom of the feature $R(A)$ to the etch rate at the top of the feature $R(0)$:

$$R(A)/R(0) = K/(K+S-KS), \qquad (1)$$

where S is the reaction probability on the bottom surface and K the molecular-flow transmission probability for a given tube or trench. A is the aspect ratio: depth/diameter for a circular hole or depth/width for a long trench. It was shown previously[8] that a simple conductance model can be used to predict the etch rate of a time-domain multiplexed inductively coupled plasma etch process with good results, when applied to linewidths typical of MEMS at moderate-aspect ratios. However, at very high aspect ratios the conductance model does not predict the almost total etch stop. Other mechanisms are needed to explain this deceleration of the etch rate. At moderate-aspect ratios the bottom of the hole is nearly flat and the sidewalls are nearly vertical. At high-aspect ratio the sidewalls start to bow and the feature bottom turns into a sharp arrowhead, as depicted in Fig. 1. The reasons for etch stop at the bottom of deep features are discussed here.

In many high aspect ratio silicon-etch processes the sidewall angle is negative for high etch-rate processes and positive for lower etch-rate process. The shape of the feature can have an impact on the passivation layer deposition during the passivation step and on passivation removal during the etch step, causing excessive sidewall etching and a reduced etch rate at the feature bottom. The shape also affects the molecular-flow conductance of a trench. A simple Monte Carlo simulation code was written to study the molecular-flow conductance in such tapered trenches. The simulation results of the effects of nonzero sidewall reaction probability
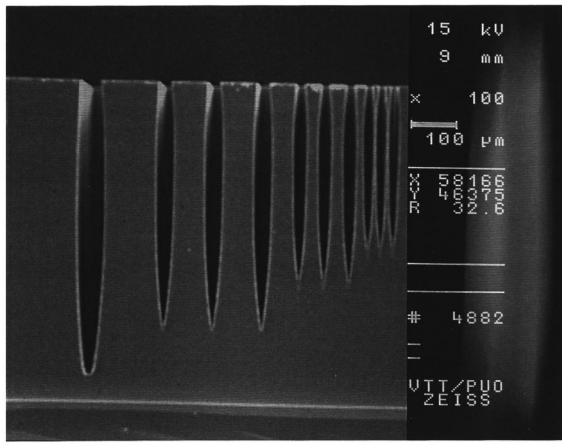
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FIG. 1. Typical change in profile of etched trenches after 180 min etch time, nominal line widths 32, 16, 8, and 4 μm, minimum depth about 400 μm, and wafer thickness 1.3 mm.

TABLE I. Summary of sample processing steps used for two different sample types.

	Standard	6 in.
Wafer size: (mm)	100	150
Thickness (μm)	525	600
Mask oxide	CVD	Thermal
Mask thickness	2 μm	2 μm
Mask etch	Plasma	BHF
Drawn hole sizes	5–50 μm	50–120 μm
Used silicon etch times	10–120 min	90–120 min
Etchable area	8% (6.3 cm^2)	6% (11.1 cm^2)

and flow conductance of tapered tubes are presented here. The model with nonzero sidewall reaction coefficients is an intermediate case between the simple conductance model[7] and neutral shadowing discussed by Gottscho, Jurgensen, and Vitkavage.[6] The simulation program was also needed for generation of transport coefficients for arbitrary length rectangular trenches, because no practical values had been published or the maximum aspect ratios used in published work[9] were much smaller compared to aspect ratios achievable by etching. The high aspect ratio trenches with relatively vertical sidewalls obtained with the Bosch process form an almost ideal platform for simulation studies of reactant transport issues. In addition to the benefits of the etch profile, the relatively simple plasma with only one input gas at a time makes the isolation of different effects easier than traditional reactive ion etching reactors, where multiple input gases and simultaneous etching and deposition reaction occur. In studies of the Bosch process it is possible to decouple etching variables from passivation variables.[4]

Very deep holes were etched into silicon to study the effect of etch time and selected process parameters. The modeling results will be compared with new deep etch results.

II. EXPERIMENT

A. Processing of samples and measurement methods

Samples were processed on 100- and 150-mm-diam highly doped p-type silicon (0.02 Ω cm) wafers of $\langle 100 \rangle$ orientation. Silicon dioxide was used for masking. A contact aligner was used for lithography. The photolithography masks used were specially designed for this purpose. Oxide masks [thermal SiO_2 or chemical vapor deposited (CVD)] were defined by either plasma (100 mm wafers) or wet etch using buffered hydrofluoric acid (BHF) (150 mm wafers). The deep silicon etching was done with an STS Multiplex ICP etcher using STS ASE recipes.[2,3] Sample processing was done at the VTT Electronics process facilities, where most of the equip-

ment is designed for 100-mm-diam wafers. A summary of the sample fabrication is shown in Table I.

Cycling conditions for our base-line high-etch-rate process were as follows: 13 s of etching with SF_6 (bias power 10 W) followed by 7 s of an unbiased C_4F_8 passivation step. The SF_6 flow was 129 sccm and the C_4F_8 flow 85 sccm. A constant coil power of 600 W and constant throttle valve position angle of 66° were used in both steps in all experiments. The additional processes used either a decreased SF_6 flow of 100 sccm or an increased rf bias of 15 W during etching, other process variables were kept constant.

The mask patterns used are described in earlier work.[3,8] The etchable area was 8% for 100 mm wafers and 6% for 150 mm wafers. The data do not allow direct comparisons over a wide range of etch times and pattern sizes because of variations in etchable area and sample manufacture. The oxide mask variations were unavoidable due to limited processing capabilities for 150 mm wafers. The different oxides behave similarly as the etch mask and have negligible or no effect on silicon etch rate, but the oxide mask etching method has an effect on the final mask dimensions.

Etched depth, the deepest point in the center of the trench, and etch profiles were determined with a Zeiss DSM 960 scanning electron microscope (SEM) from sawn cross sections from the center parts of the wafer.

B. Monte Carlo simulation of neutral transport

As flow conductances were not available for shapes other than long slit-like tubes and holes, a short Monte Carlo simulation code was written in basic-like language. The calculation was done on a desktop PC. The etch-rate modeling was later done using a spreadsheet program. The sample size N was kept at 100 000 throughout, giving an accuracy of simulation of about 0.3%.

First, the flow conductance values for rectangular tubes were calculated. Next, the same code was modified for other geometries. Particle transport was calculated using a similar method as described in Ref. 10. The maximum depth of each particle is recorded, and the molecular-flow coefficients are calculated from the particle statistics.

1. Geometrical considerations

Trajectories were calculated in three dimensions. The maximum aspect ratio, which in this case is the same as the

tube length, was set at 40. In deep silicon etching the typical aspect ratios fall within this range. In the case of infinite trenches the computation can be accelerated if the three-dimensional angular distribution is replaced by its in-plane equivalent, as discussed elsewhere.[11] This was not done here.

2. Angular distributions

The angular distribution functions for θ are generated from the following equation:

$$\frac{\int_0^\Theta \sin(\theta)\pi 2W(\theta)\partial\theta}{\int_0^{\pi/2} \sin(\theta)\pi 2W(\theta)\partial\theta} = RND, \qquad (2)$$

where RND is a random number and the weight function $W(\Theta)$ is the distribution function.

Selection of the angular distribution of incoming particles (from the plasma) has a notable effect on transport probability. The current simulations were done with a cosine distribution as this has been used in the handbook formulas[9] and in an earlier work.[8]

3. Sidewall losses

Sidewall losses were implemented using a random number generator. After each collision a new random number was generated and compared with a threshold value. If the threshold value was exceeded, the particle was deleted. No other reactions on the sidewalls or effects on the total etch rate given by Eq. (1) are assumed; the transport coefficients are merely attenuated in proportion to the number of deleted particles.

4. Tube shape

The transport probability of a tapered tube or a conical nozzle is different depending on which end of tube is the entrance. The transport probability is higher the larger the exhaust opening. Simulation results for low aspect ratio conical nozzles with positive opening angles can be found elsewhere.[10] Here, a short simulation is done for a tapered high aspect ratio slit-like tube.

5. Ion transport considerations

The depths of the first flight of particles can be used to evaluate the probability of particles reaching the bottom in one direct flight. This can then be used to estimate ion-shadowing effects, if the used angular distribution for incoming particles is realistic and ion deflection is negligible. These data are collected in each case. If ion-reflection calculations such as those done by Arnold, Gray, and Sawin[11] are needed, the number of reflections should be limited or more complete particle histories collected.

III. SIMULATION RESULTS

As a quick confidence check, the transport simulation results with cosine distribution were compared with results from handbook formulas for infinitely long slit-like tubes
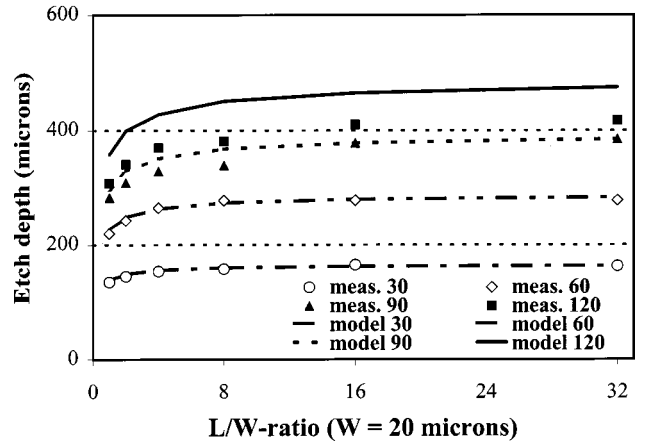

FIG. 2. Modeling results, nominal linewidth is 20 μm and etch times are 30, 60, 90, and 120 min.

and circular holes. The results were indistinguishable. An isotropic input distribution gives a much lower transport probability than a cosine distribution.

A. Rectangular patterns

After confirmation of simulation results for infinite trenches and holes, transport probabilities for rectangular trenches were calculated. The used length/width ratios are 1, 2, 4, 8, 16, and 32. When the length of the rectangular trench is 32 times the width, it can be considered an infinite length for most practical purposes. Squares and circular holes have small differences, the most notable difference occurs in lateral aspect ratios between one and two and between two and four. To ensure functionality of the etch-rate model, the new transport probabilities were inserted into the model and compared with the etching results. Model coefficients $[R(0) = 7.27\ \mu\text{m/min},\ S = 0.27]$ and part of the etch data are from previous work;[8] the etch data from the 90 and 120 min etches are new and measured from 100-mm-diam wafers. A Comparison of the modeling results and measured data is shown in Fig. 2 and shows that the pattern shape dependency is modeled qualitatively correctly, but the depth of the samples with longer etch time is coarsely exaggerated.

B. Nonzero sidewall reaction probability

The effect of the sidewall reactions was calculated with reaction probabilities ranging from 0.0025 to 0.1 for both circular holes and infinite-length trenches. The lower limit is about 1% [of the observed apparent reaction probability at the bottom of the trenches. The modeled etch depths with transport probabilities of lossy tubes are shown in Fig. 3. The effect of losses is more pronounced for holes, which is understandable because the number of reflections required for particles reaching the bottom is larger. The effect of sidewall reactions can be notable, especially in the case of a low-reaction coefficient at the bottom, when the aspect ratio dependency is not expected, the sidewall losses can be the main cause of the aspect ratio dependency.
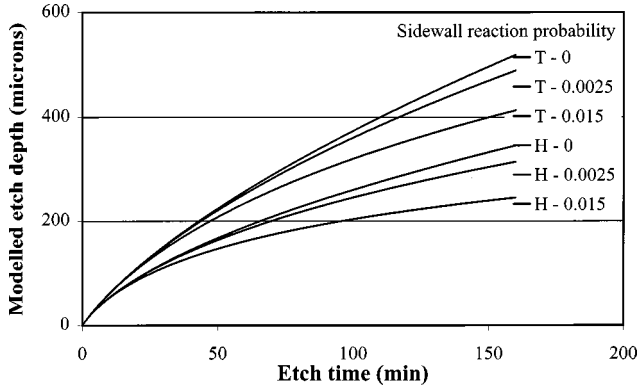
FIG. 3. Modeled etch depth as a function of time using transport probabilities of lossy trenches and holes with nominal linewidth of 20 μm, sidewall reaction probability as a parameter.

C. Effect of nonvertical sidewalls

The effect of tilted sidewalls on reactant transport was calculated. As expected, the transport probability for negatively tapered profiles was notably higher than for tubes with a positive sidewall angle. However, the effect diminishes if the transport probability is scaled with the feature width at the given depth.

For a large negative sidewall angle, the total flux to the trench bottom may rise but the flux per area unit remains roughly constant. The number of particles reaching the bottom by direct flight will increase, but only in relation to the initial angular distribution. Unidirectional ion bombardment can cause large ion shadowing on high-negative sidewall angles.

The reactant transport differences of tapered trenches cannot explain the etch-rate difference between the high-rate process that has a negative sidewall angle and lower-rate processes that have a positive one. The relative etch rate is determined by the aspect ratio only. The sidewall angle may have a more important role during the passivation step, as the deposited passivation-layer thickness may differ on differently oriented surfaces.
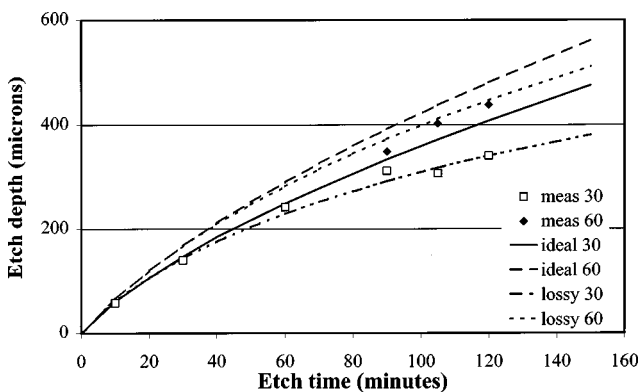
FIG. 4. Etch depths of 30- and 60-μm-diam holes as a function of etch time. The markers indicate measured data, the lines indicate the modeled data. Sidewall reaction coefficient of 0.015 is used in modeling of lossy circular tubes.
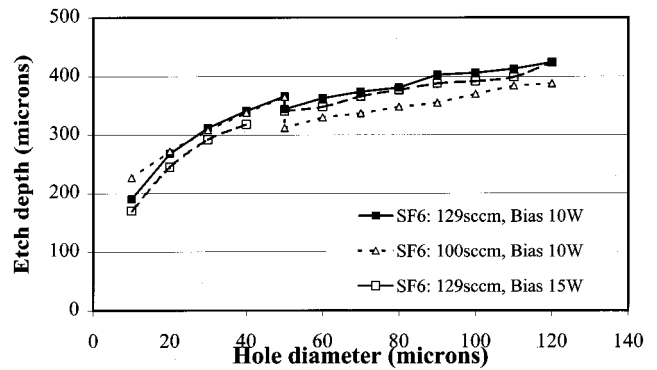
FIG. 5. Plot showing linewidth dependence of etch depth, SF$_6$ ow, and bias power as parameters.

IV. MEASUREMENT RESULTS

The measurement results of 30- and 60-μm-diam holes are shown in Fig. 4. The modeling results are plotted in Fig. 4 together with the measured data. The total width of the nominally 60 μm oxide mask opening is about 69 μm after wet etching of the mask and 90 min of dry etching. For the dry-etched mask an average of 3.7 μm total widening was observed after 10–80 min silicon etching. In modeling, a 4 μm offset was used when defining the aspect ratio. The scatter in the lower measured data curve is partly caused by positional inaccuracy of SEM cross sectioning.

The etch depth of circular holes as a function of hole diameter is plotted in Fig. 5. The discontinuity in curves is caused by the loading effect.

The SF$_6$ flow and bias power are used as parameters. The Etch time is 90 min. As Fig. 5 shows, the etch rate is slightly higher for the smallest features with the lowered SF$_6$ flow than with our standard process. For larger holes the standard process is faster. The shape of the bottom of the features is flatter for the case of lower SF$_6$ flow. The latter is true for the case of higher bias power, too.

V. DISCUSSION

Reactant transport has a major effect on the etch rate of high aspect ratio features. The modeling results of this (Fig. 2) and previous work[8] confirm that a molecular-flow conductance model can predict the etch depth correctly for a wide range of shapes. However, for the highest-aspect ratios the model gives overly optimistic etch depths. Possibly this can be attributed to losses due to sidewall reactions. At higher-aspect ratios the ion flux can deteriorate the thin sidewall passivation layer, thus making sidewalls prone to etching. Also, the surface roughness increases during etching, which can make the sidewalls even more vulnerable. In Fig. 4 the etch depths are modeled for both lossless and lossy cases. In the lossy model the sidewall reaction coefficient is set to 0.015. Using this reaction coefficient together with the earlier model parameters gives an improved fit for 60-μm-diam holes compared to lossless transport. The sidewall reaction coefficient value 0.015 may give too low a value for etch depth, because the actual depths of 30 μm holes can be

higher compared to the measured values due to positioning inaccuracy and that the 60 μm hole data are from samples with higher pattern loading. However, the trend of the etch-rate deceleration compared to the ideal case is clear and is seen also in Fig. 2.

In high-density plasmas the number of ionized particles is considerably higher than in the plasmas used in traditional reactive ion etching. Comparison of the observed high reaction probabilities (in the range 0.2–0.3) with the reaction probability data of Gray, Tepermeister, and Sawin[12] suggests that the neutral-flux-to-ion-flux ratio is very low and that the silicon etching is neutral limited.

In addition to sidewall etching, the feature bottom changes from flat-bottom sharp-edged feature to rounded-bottom corners and eventually features close up. This can be a factor causing the scatter of the measurement data of 30 μm holes of Fig. 4. In practice, the complete clearing of the trench is usually required and then a further extension in etch time is needed.

This kind of feature evolution does not arise from neutral diffusion. The most likely reason for this profile change is the deficient or slowed-down passivation polymer removal during the etch step. At high aspect ratios the ion shadowing limits the polymer etching. So the overall etch process is no longer purely neutral limited, becoming instead ion limited as the aspect ratio increases. For circular holes the critical-aspect ratio is in the range of 10:1. This figure is obtained from feature profile inspection. In earlier measurements,[8] the highest-aspect ratios obtained for trenches were about 35:1 and the critical-aspect ratio is below this for the etch process used in these studies. Determination of the critical-aspect ratio of long trenches would require more measured data on extremely deep-etched trenches or knowledge on the width of the incoming ion angular distribution. An approximation of neutral flux as a function of the aspect ratio can be obtained from the molecular-flow model.

If the incident ion flux limits the passivation removal, then a higher or more directed ion flux is needed at the beginning of the etch step. For profile control it would be ideal to keep the etching in the neutral-limited regime all the time. However, the increase of ion directivity by either increasing bias or lowering the pressure will lower the etch selectivity against the masking material. Parameter ramping schemes where, among other parameters, platen (bias) power is increased during etching to ensure profile control, while the aspect ratio is changing continuously, have been recently developed by at least one equipment manufacturer.[13,14] The simple modeling strategy used in this article may not be applicable in the case of parameter ramping where the $R(0)$ is continuously changed during the etching.

The high reaction probabilities obtained with a simple, lossless etch model may already include the effect of transport losses due to sidewall reactions. Similar modeling results may be obtained with a model utilizing low bottom-reaction probability and high sidewall-reaction probabilities. To ensure the quality of the model, realistic reaction probabilities are needed, which is probably a difficult task in the case of sidewall reactions, as the thickness of the sidewall protecting layer can be indeterminate and the reaction probabilities can vary with depth.

The tube shape can also have an impact on reactant transport. The Monte Carlo simulation shows that the tapered tube has an effect on tube directivity.[10] In the case of bowed profiles it is possible that the molecules are trapped in the middle parts of the tube, where it is widest, and cause further bowing.

Utilization of Gaussian or other applicable distributions to evaluate ion transport into trenches is planned in future studies. The most serious obstacle in improving the etch-rate model is the lack of information on aspect ratio dependency of passivation polymer deposition and etching.

VI. CONCLUSIONS

The molecular-flow conductance model is used to predict the etch depth of trenches of various shapes. The aspect ratio dependency of the etch rate of the Bosch process is explained reasonably both qualitatively and quantitatively by molecular-flow conductance. It is shown with the help of Monte Carlo simulation that sidewall reactions can have a notable effect on etch rate as the aspect ratio increases. At higher aspect ratios the passivation polymer etching becomes ion-flux limited, while silicon etching remains in the neutral-limited regime. The measurement results indicate that higher-aspect ratios can be achieved with increased ion directionality and the amount of lateral etching can be decreased at the same time.

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Appendix II

Loading effects in deep silicon etching

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ABSTRACT

Feature scale pattern dependencies (microloading and aspect ratio dependent etching) and chip and wafer level loading effects complicate the use of deep silicon etching in MEMS applications. They have major effect on uniformity and etch rate on the wafer scale and on a feature scale. The aim of this study was to find the limitations that these phenomenon set on deep silicon etching. Wafer scale (100 mm or 150 mm), chip scale (1-10 mm) and feature scale (1-1000 µm) structures were etched in pulsed ICP (Bosch process, SF_6/C_4F_8). Etched depths were 10-500 µm, and aspect ratios up to 20:1. Strong dependence of etch rate on loading was observed. On the wafer scale average etch rate was greatly reduced, from 5.4 µm/min (8% load, 2 mm feature size) to 1.7 µm/min (100% load). At same time uniformity deteriorated from excellent 2% to 35% which is too high value for practical applications. Chip pattern density did not affect etch rate on an isolated small chips (2.5 x 2.5 mm^2) but for 10 x 10 mm^2 chip 10% etch rate reduction was seen at high chip scale load. In this case wafer scale etchable area was 6%. We show that feature scale and wafer scale pattern dependies in ICP etching are strongly coupled.

Keywords: Plasma etching, pattern density, uniformity, MEMS, etch rate

1. INTRODUCTION

Single wafer etch processes must be characterized for various pattern effects: macroloading (etch rate depends on etchable area on the wafer scale), microloading (etch rate depends on etchable area on a chip or feature scale), and profile loading (sidewall angle depends on etchable area; typically array lines exhibit profiles different from isolated or edge-of-array lines). Basically they are caused by reactant depletion and can be reduced by reducing the etch rate, increasing the supply of reactants or by better control strategies [1, 2, 3]. In the ion activated, surface reaction limited, regime etching is less prone to loading effects than in mass transport limited regime[4].

RIE-lag (smaller etch rate in smaller features) and ARDE (aspect ratio dependent etch rate or etch rate decrease as a function of etch time for a given line width) are other important pattern effects in etching. In MEMS applications aspect ratios are similar to DRAM trench capacitors, 5:1 to 40:1, but feature sizes are one or two orders of magnitude larger, typically tens of microns. Much of the literature on RIE-lag and ARDE are about submicron structures [2, 5] and only recently has the importance of ARDE been recognized in MEMS-dimension structures [6].

The terms RIE-lag and microloading are often used interchangeably even though they are two are different phenomena. However, sometimes it is difficult to determine which effect is the dominant one: is the etch rate lower because of RIE-lag or because of loading effect? We have designed test structures and chip layouts in order to distinguish the two. We have characterized SF_6/C_4F_8 pulsed (time domain multiplexed) ICP etching (Bosch process) for loading effects at various scales: at feature scale (feature sizes range from tens of microns to hundreds of microns), at chip scale (1 to 10 millimeter) and at wafer scale (1-100% pattern density), and studied interactions between pattern effects.

2. EXPERIMENTAL

Silicon wafers of both 100 mm and 150 mm wafers were used. Both bulk and bonded SOI (Silicon On Insulator) wafers were used. Thermal, TEOS and PECVD oxides were used as masks. Mask oxide etching was done either in CHF3/CF4/He plasma or in BHF. Feature size enlargement due to undercutting in wet etching is usually not an issue for our feature sizes.

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2.1. Pulsed ICP etching

Pulsed SF_6/C_4F_8 process from Bosch/STS was used[7]. In this process silicon is etched in a fast but isotropic fashion during SF_6 pulse, and C_4F_8 pulse is used to passivate the sidewalls of the etched features. This results in various problems not encountered in traditional etching: pressure is not a variable in the ordinary sense because of large overshoot when gases are switched, and the etch profile is undulating due to pulsing. The baseline process (DEEP) has 13/7 ratio of SF_6 and C_4F_8 pulses and 45 mtorr pressure. Alternative process ORTOB2 has 12/12-pulse ratio and similar pressure as the baseline process, whereas SLOWNEW has 15 mtorr pressure and 5/5-pulse ratio. Our baseline process is maximized with respect to etch rate (7 µm/min maximum etch rate; 4.8 µm/min average rate in etching through the 380 µm wafer), and some profile non-idealities (barreling, retrograde profile) are accepted in trade-off[8].

2.2. Test structures

Macroloading test structure consists of large squares of different sizes (2,4,6,8 millimeter edge length) surrounded by a 100 µm wide trench at 400 µm distance. Wafer stepper lithography was utilized to vary the percentage of exposed area on the wafer. Etched depths were measured from cross section samples by SEM. Sample weighing was also used for etch rate determination. Uniformity of etching for the 100% loading was measured using special wafers with ultralow TTV values of less than 1 µm, and etched thickness was calculated from nominal original thickness from SEM cross section samples.

For microloading, traditional arrays vs. isolated lines structures of various line widths and array sizes were employed. But a new type of structure with nested broken rings, with self-similar shapes but varying local pattern density was used in majority of test runs. The structure is shown on figure 1. Local loading varied from 0.6% to 40%. This test pattern was replicated at three different scales, with maximum edge lengths of 10 mm, 5 mm and 2.5 mm. For a given nested structure, the loading percentage was constant determined by both number and width of trench. The same structure is also used for determination of ARDE, because the shape of trench is unaltered and the line width of inner rings is decreasing.
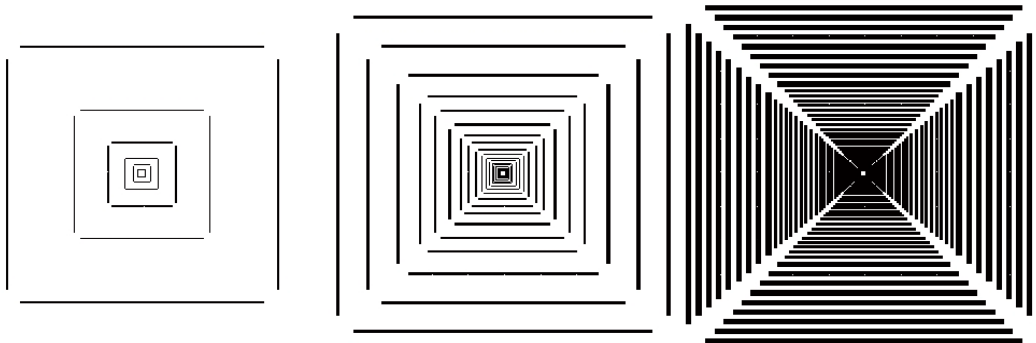
Figure 1 Nested ring test structures with 1.15 % (left), 6.91 % (middle) and 41.46 % (right) local loading.

The etch rate of mask oxide was measured from large area test sites on both macro- and microload layouts. Additionally, it was measured at the center of the nested ring microload structure, thus establishing oxide etch rate at varying local loads. Nanometrics AFT 4150 reflectometer was employed. Selectivity between silicon and oxide was calculated from silicon rates (for a fixed feature size) determined from SEM cross sections and oxide rates measured by reflectometry at adjacent sites.

3. RESULTS AND DISCUSSION

3.1. Macroloading

Wafers with very small etchable area (ca. 1%) etched for a short period approximated zero load. This gives the inherent maximum etch rate available under a chosen set of process parameters. Zero load etch rate was extrapolated to be 7.3 µm/min. Etch rate for 100% load was 1.66 µm/min from mass loss measurement, 1.5 µm/min from SEM cross sectioning.

Results are plotted in figure 2 against inverse of etch rate (ER). Large squares (2 mm) and lines (100 µm) have practically the same etch rate. The fitting line is according to a loading model by Mogab[1]. Even though the model was originally developed for batch reactors, the basic assumptions are valid for any radial reactors. G is the etchant generation rate, β is a proportionality factor to etching species, τ is the mean lifetime of active specie, V is reactor volume, and A_w is etchable area on the wafer.

$$ER = \frac{\beta \tau G}{1 + \beta \tau \dfrac{A_W d}{V}} \quad , \tag{1}$$

The model gives very good fitting. In large loads it has to be considered that etch rate non-uniformity across the wafer is significant (this will be discussed in more detail in following chapters) but in fig. 2 average etch rates across the wafer have been used. Another important consideration is that the maximum aspect ratio was only 3:1. In such low aspect ratio structures ARDE is insignificant and therefore etch rates of 2 mm squares and 100 µm lines are almost identical.
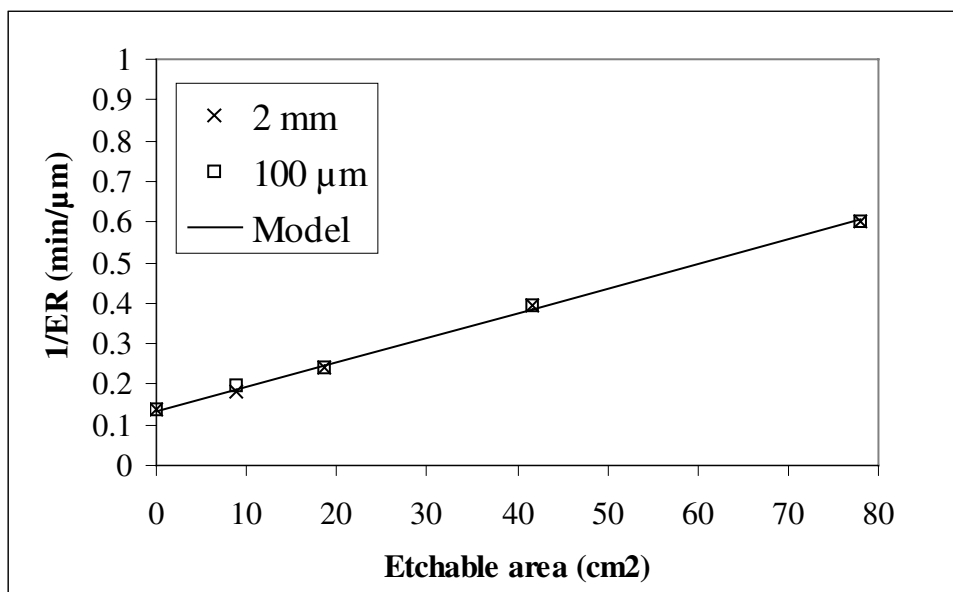
Figure 2 Inverse of etch rate in the function of loading for 2 mm square and 100 µm line and results fitted to model of Mogab.

3.2. Chip scale loading

In figure 3a we present the influence of nested ring size (2.5, 5, 10 mm edge length) on the etched depth of a 32 µm line. The etching time was 90 minutes. For the 2.5 mm rings etched depth is independent of local load percentage, but for 5 mm and 10 mm chips there is a local loading effect. The main reason for deviation of etched depths from trend line is etching uniformity across the wafer. In our etching system etch rate is typically higher at edge of wafer than at center[10].

In fig. 3b etched depths of 100 µm lines were measured from 100 mm² chips with a single square pattern in the middle (4, 16, 36, 64 mm²) (the test structures were on different wafers in 3a and 3b. Etch time was 60 minutes.
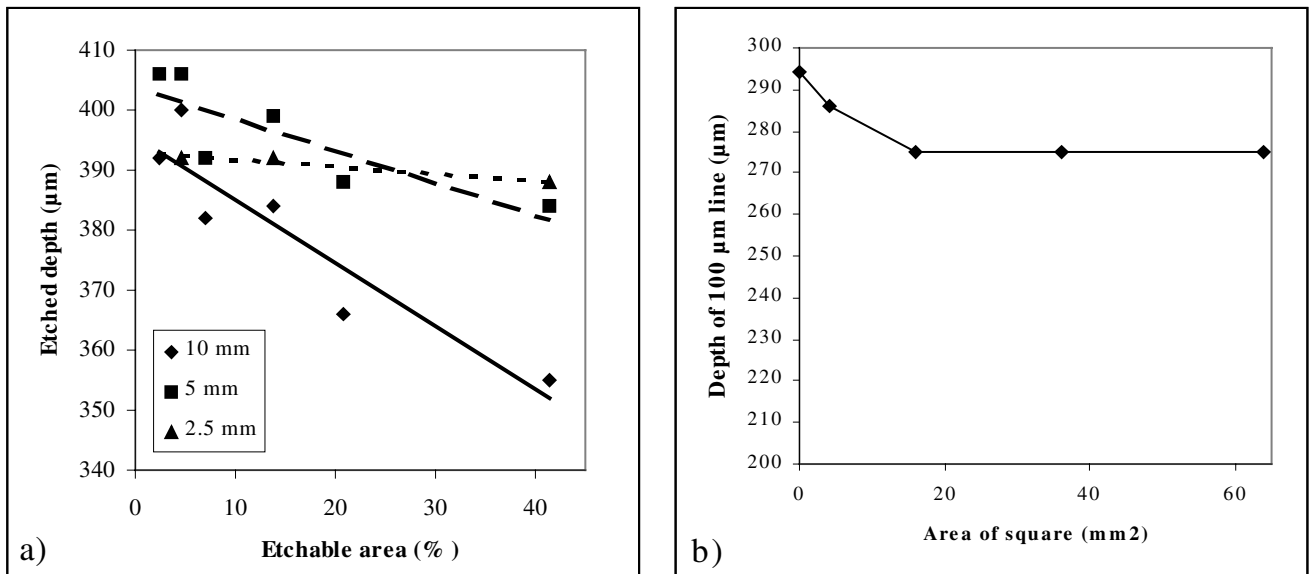
Figure 3 a) etched depth of 32 µm test line for different sized nested rings; b) etched depth of 100 µm test line adjacent to squares with different chip scale load (0 – 64 mm^2/100 mm^2 chip).

For a 2.5 mm chip size chip-scale etchable area does not have any effect on etch rate, for the 5 mm chip there is some reduction in the rate and for the 10 mm chip loading effect is large. From figure 3a we estimate that the reactant depletion distance for our baseline process is therefore of the order of 3-5 mm. Further evidence comes from fig. 3b: the effect is starting to appear when the square edge length is 4 mm.

3.3. Microloading

The traditional microload test structure of isolated and array lines gave a null result: no differences were found. The nested broken rings test structure has a much wider range of local loads, and as shown in figure 4, local load does indeed affect the etch rate. In figure 4a etched depths of different line widths with different local loading are plotted after 80 minutes of etching and in figure 4b identical structure is measured after 10 minutes of etching.

In the case of longer etching time, microloading has a minor influence to etched depth. Feature size effect is the dominant pattern effect. For 10 minutes etch time both microloading and ARDE can be seen and both have major effect on etched depth.

The traditional test structure of isolated and array lines fails to give information on microloading if it smaller than the depletion distance; and if its environment is not representative of real device design. Our nested ring structure involves local pattern density inherently, and it takes much more area but it is an essential structure for process characterization. Other investigators have used constant line patterns with varying spacings[9] but we feel that loading, which is an area effect, requires a truly 2-dimensional test structure. Additionally, the nested broken ring structure lends itself to easy SEM sample fabrication.
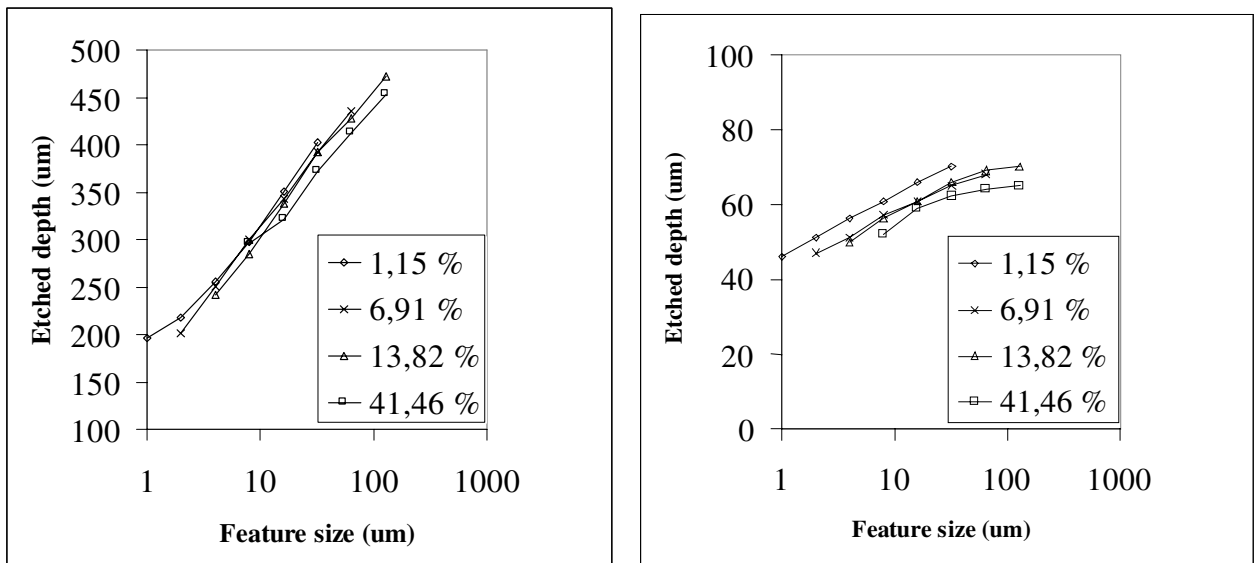
Figure 4 a) 80 min etch time: feature size effect dominates over microloading; b) 10 min etch time: microloading and feature size effect both have major effect on etched depth. Local load varies from 1.15% to 41.46%.

3.4. Uniformity

In figure 5 normalized etch rates of 2 mm squares are plotted as a function of radial distance. The etching time was 60 minutes.
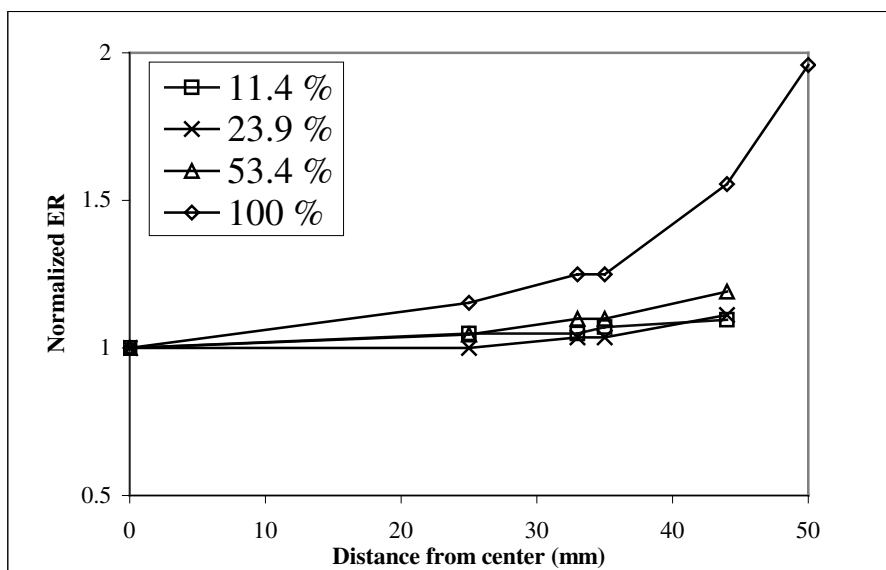

Figure 5 The effect of macroloading (11-100%) on radial uniformity. Normalized silicon etch rates.

From fig. 5 we can see that uniformity was ca. 5% for low load cases but increased to 35% for high loads. This sets serious limitations on device designs with large etchable areas.

3.5. Process variations

In order to improve uniformity, Bosch process modifications with variations in bias power, SF_6 flow, pressure, gas pulse ratios and durations were tried. Results for SF_6 flow and bias changes to our baseline process are shown in figure 6. Decreasing flow improves uniformity at the expense of etch rate, but at higher bias power improvement can be achieved at reasonably high etch rate.
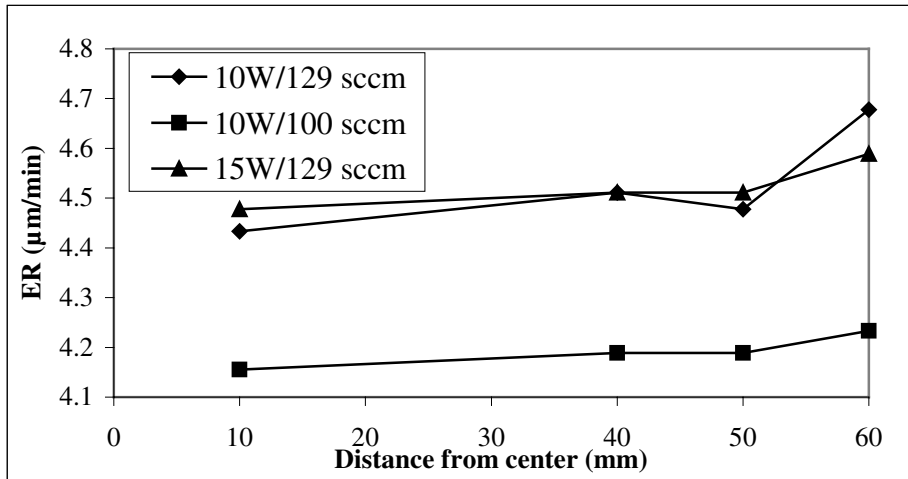
Figure 6 The influence of SF_6 flow and bias power on uniformity of 50 µm lines. Etchable area is 6 % on 150 mm wafer.

In fig. 7 alternative processes ORTOB2 and SLOWNEW[11] have been characterized with regards to uniformity. Improved uniformity has been achieved but at the expense of greatly reduced etch rate, as predicted by the model of ref. 1. In figure 9 DEEP indicates our baseline deep etching process, ORTOB2 is a process optimized for high selectivity and vertical sidewalls and SLOWNEW is a process optimized for small undercut and minimized ARDE.
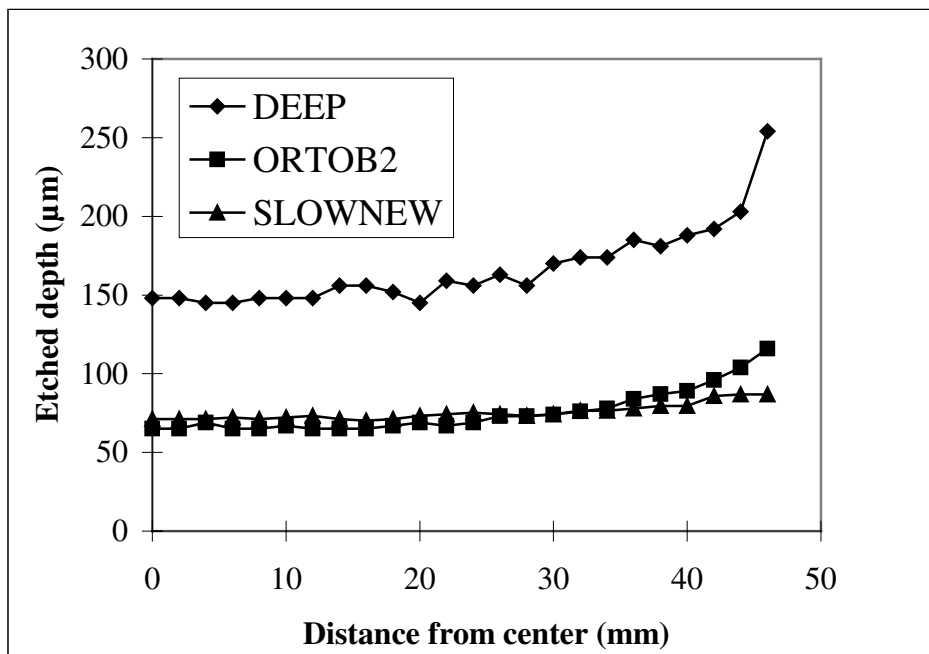
Figure 7 Etched depths and uniformity with three different processes: load 59%, time 60 min.

3.6. Oxide erosion and selectivity

Thermal, TEOS and PECVD oxides were used as masks and all were found to be practically identical as regards to oxide etch rate. Oxide etch rate in the function of silicon etchable area is shown in figure 8. Results are from same wafers than silicon etch rates showed in figure 5.
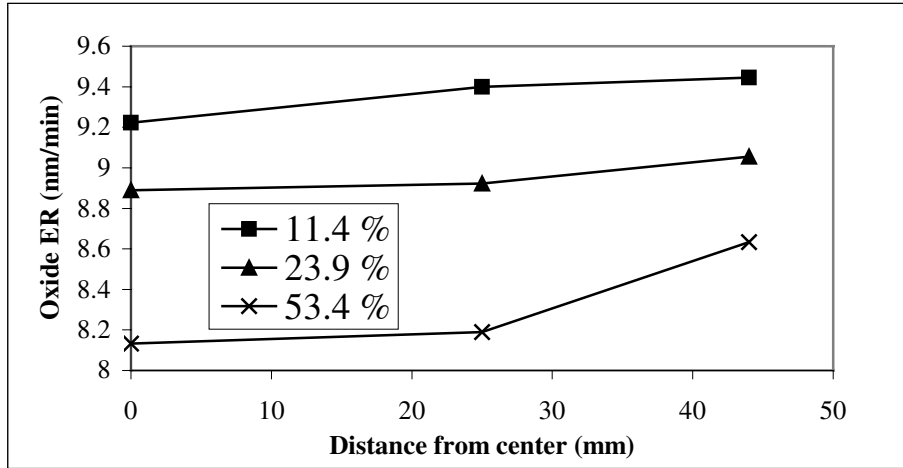
Figure 8 Oxide radial uniformity as a function of silicon macroloading.

It can be seen that oxide etch rate uniformity is much better than silicon etch rate uniformity. Oxide etching is not much affected by silicon load. Therefore oxide selectivity decreases mainly because of silicon ARDE. Because of this, selectivity needs to be defined for specific linewidths. This is plotted in figure 9.
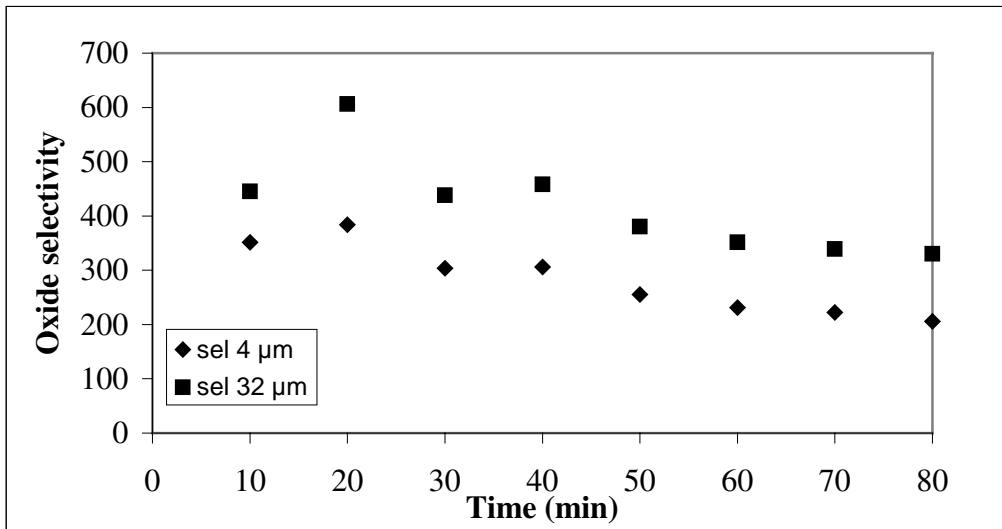
Figure 9 Oxide selectivity as a function of time for 4 µm and 32 µm wide silicon trenches.

Alternative process ORTOB2 with higher C_4F_8 ratio has been studied by us[11]. Oxide selectivities in excess of 1000:1 have been measured. However, the original oxide thickness and final oxide thickness are almost the same, which leads to large relative errors in oxide loss calculation and consequently for selectivity.

Buried oxide thickness needed to stop etching is much more complicated to determine: not only selectivity but silicon etch uniformity, RIE-lag (device design dependent) and oxide ARDE have to be taken into account. Overetch requirement is determined by silicon ARDE in low load case whereas across-the-wafer non-uniformity might be more important for higher loads.

We have observed a phenomenon that could be described as secondary microloading[5]: mask oxide etch rate is affected by local silicon load. This effect has no been seen in all experiments but only in a few series. Large area reference sites and local test sites with <15% local load had identical oxide losses, but at 20% local load there was a clear increase in mask oxide loss and at 40% local load the effect was significant, e.g. 45% increase after one hour etching. This was initially attributed to polymer confounding the oxide thickness measurement by the reflectometer, but remeasurement after oxygen plasma treatment gave unchanged results. We do not at the moment have an explanation to this secondary loading non-reproducibility but we speculate that polymer deposition in the reactor could cause it.

4. CONCLUSIONS AND SUMMARY

It is well known that pulsed (time domain multiplexed) deep silicon etching suffers from serious loading effects typical to reactant transport limited etching. We have investigated the magnitude of the loading effect with test structure design in micro and macroscale. In macroscopic scale the loading effect is unavoidable but in microscale with clever design the adverse effects of loading can be alleviated to some extent. The behavior of loading effect in macroscopic scale is well described by the model of Mogab[1] and the etch rate is dramatically decreased when the etchable silicon area exceeds 20%. Our measurement data on microloading shows that features larger than 2-3 mm or chips larger than ca. 10 mm^2 with high etchable area have an impact on etch rate of adjacent features or features within the same chip. The silicon etch uniformity is severely affected by loading. The radial etch non-uniformity causes extra requirements for etch selectivity against etch stop layer. To be able to correctly predict the etch depth of arbitrary features the models for pattern depended etching[8] and loading effect should be coupled in both micro and macro scales.

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Appendix IV

Square-Extensional Mode Single-Crystal Silicon Micromechanical Resonator for Low-Phase-Noise Oscillator Applications

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Abstract—A micromechanical 13.1-MHz bulk acoustic mode silicon resonator having a high quality factor ($Q = 130\,000$) and high maximum drive level ($P = 0.12$ mW at the hysteresis limit) is demonstrated. The prototype resonator is fabricated of single-crystal silicon by reactive ion etching of a silicon-on-insulator wafer. A demonstration oscillator based on the new resonator shows single-sideband phase noise of -138 dBc/Hz at 1 kHz offset from the carrier.

Index Terms—Bulk acoustic wave devices, microresonators, oscillator noise, oscillators, phase noise, resonators, silicon-on-insulator (SOI) technology.

I. INTRODUCTION

MODERN wireless applications are setting increasing demands for the oscillator size, power consumption, and price. The conventional quartz crystal-based low-phase-noise oscillators are typically centimeter sized and appear bulky in the otherwise highly integrated transceiver architectures. Micromechanical resonators offer a promise of compact size, low power consumption, and integrability with IC electronics, and are thus, a very attractive potential alternative for the quartz crystals [1].

A low-phase-noise oscillator requires a resonator capable of a high quality factor and a large power output [2], [3]. Both requirements are typically met using quartz crystals, in particular the large physical size of quartz resonators accommodates high drive levels. In contrast, as the resonator size is dramatically reduced in the case of microresonators, the low power capacity limits the achievable oscillator noise floor [4].

This letter describes a 13.1-MHz micromechanical resonator which, for the first time, provides oscillator phase noise performance typically required in wireless communication applications. The resonator is based on a two-dimensional (2-D) bulk acoustic vibration mode that allows a maximum drive level $P = 0.12$ mW and a quality factor $Q = 130\,000$.

II. RESONATOR STRUCTURE AND FABRICATION

Fig. 1 shows the schematic and scanning electron microscope (SEM) image of the resonator. The resonator size is $320 \times 320 \times$
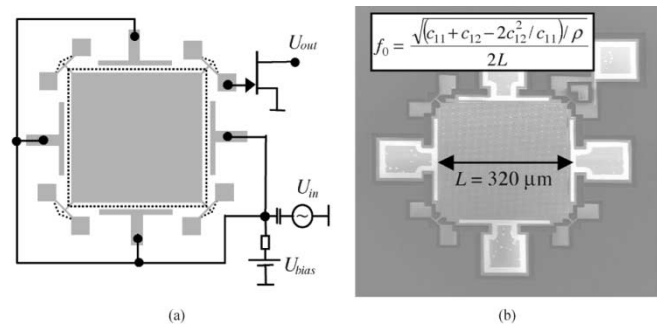
Fig. 1. Square-extensional microresonator ($f_0 = 13.1$ MHz and $Q = 130\,000$). (a) Schematic of the resonator showing the vibration mode in the expanded shape and biasing and driving setup. (b) SEM image of the resonator.

10 μm. The surface orientation is (100) and the plate sides are aligned in the $\langle 110 \rangle$ crystal directions. The T-type corner anchoring is used for reducing the energy leakage to the substrate.

The component was made by deep reactive ion etching of silicon-on-insulator (SOI) wafer. For the hydrogen fluoride (HF) release, the plate was perforated with a 39×39 matrix of 1.5 μm diameter holes. The structural silicon layer and the substrate were heavily boron-doped ($\rho_B \approx 5 \cdot 10^{18}$ cm^{-3}) for electrical conductivity.

III. RESONATOR MODEL

As shown on the schematic in Fig. 1, the vibration mode can be characterized as a square plate zooming in and out thus preserving the original shape. This is in contrast with the well-known Lamé-mode in which the square edges bend in antiphase preserving the plate volume [5]. Our resonator also exhibits the Lamé-mode (at $f_0 = 12.1$ MHz, $Q = 60\,000$), but it is not excited in the symmetrical four-electrode configuration.

The mode can be approximated as a superposition of two orthogonal sound waves with the displacements given by $u_x = A \sin \pi x / L$ and $u_y = A \sin \pi y / L$, where A is the vibration amplitude, L is the plate size, and x and y indicate the position on the plate. This biaxial motion in x and y direction, with minimal rotation and shear, is a consequence of Poisson's ratio between the [110]- and [$\bar{1}$10]-direction being very small ($\nu = 0.06$). Thus, the square resonator shape, instead of circular [6], optimally accommodates the anisotropic elasticity of single-crystal silicon. The analytical mode shape was verified with a three–dimensional (3-D) finite element model (FEM) that included the silicon anisotropic elastic properties.
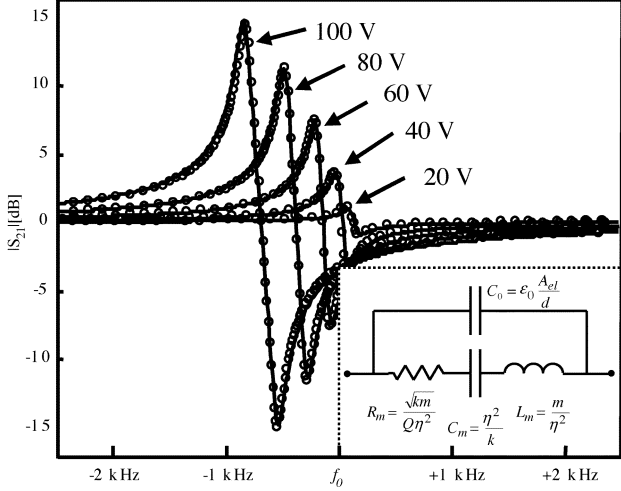
Fig. 2. (o) Measured and (−) simulated transmission response (f_0 = 13.1 MHz). Arrows indicate different bias voltages. Quality factor, gap spacing, and parasitic capacitance were adjusted for the best fit. Inset: electrical equivalent circuit.

By integrating the mode shape, a lumped one degree of freedom model shown in the inset of Fig. 2 is obtained. The circuit components depend on the effective spring constant k, the effective mass m, the quality factor Q, the electromechanical transduction factor $\eta = U_{\text{bias}}C_0/d$, the electrode area A_{el}, and the electrode gap d [4]. The effective mass and effective spring constant are related to the device geometry by

$$m = \rho h L^2$$
$$k = \pi^2 Y_{2D} h \qquad (1)$$

where ρ is the silicon density, h is the device height, and Y_{2D} is the effective elastic modulus for the 2-D expansion. For a plate without holes this is $Y_{2D} = c_{11} + c_{12} - 2c_{12}^2/c_{11} = 181$ GPa, where c_{11} and c_{12} are the silicon stiffnesses. The resonant frequencies obtained with the analytical approximation and FEM simulation agree within 0.5% for a solid plate confirming the validity of the model. The first-order lumped model has also been refined to include the effects of frequency shift due to bias voltage and capacitive and mechanical nonlinearity [7], [8].

IV. MEASURED RESONATOR CHARACTERISTICS

The prototype resonator was measured using an HP4195A network analyzer and a JFET (Philips BF545B) preamplifier [4]. The resonator was dc-biased using 100-kΩ resistors. To minimize the parasitic capacitance, the resonator substrate was grounded and consequently the largest feed through path is the work capacitance C_0. Fig. 2 shows small-signal level (u_{ac} = 50 mV) transmission curves at different bias voltages showing a good agreement with the measured and simulated data. The mechanical resonance appears at $f_0 = 13.112$ MHz, which is about 4.7% lower than the result for a solid plate without the etch holes. With increasing bias voltage, the resonator peak shifts to a lower frequency due to the first-order nonlinearity in a parallel plate electromechanical coupling that results in electrical spring softening [4]. Based on the measured data, the mechanical un-

TABLE I
RESONATOR DIMENSIONS AND CHARACTERISTIC PARAMETERS
MEASURED AT $U_{\text{bias}} = 100$ V

Parameter	Symbol	Value	Units
Resonator side length	L	320	[μm]
Electrode length	L_{el}	290	[μm]
Resonator height	h	10	[μm]
Transducer gap	d_0	0.75	[μm]
Effective spring constant	k	16.2	[MN/m]
Effective mass	m	2.39	[nkg]
Quality factor	Q	130 000	
Motional capacitance	C_m	20.8	[aF]
Motional inductance	L_m	7.07	[H]
Motional resistance	R_m	4.47	[kΩ]

loaded quality factor is estimated to be $Q = 130\,000$. The other resonator characteristics are summarized in Table I.

The resonator drive level, typically expressed as the power dissipated in the resonator, sets the oscillator noise floor and is directly proportional to stored mechanical energy ($P = \omega E/Q$) [2], [3]. For the demonstrated resonator, the energy storage was limited by mechanical nonlinearities, which caused hysteresis in the resonator transmission response at the vibration amplitude $x_{\text{vib}} = 155$ nm ($i_{\max} = 160\ \mu$A at $U_{\text{bias}} = 100$ V). This translates into maximum drive level $P = 0.12$ mW and stored energy $E = 190$ nJ. The high value arises from

1) the 2-D bulk acoustic vibration mode of the resonator that results in large effective mass and mechanical stiffness;
2) the high linearity of silicon as a mechanical material;
3) the high ratio of mechanical stiffness to nonlinear electrical coupling terms [7], [8].

Normalizing the stored energy with the resonator volume we obtain $E/V = 1.9 \cdot 10^5$ J/m^3. The corresponding typical hysteresis limit of AT-cut quartz crystal is only $E/V = 500$ J/m^3 [9]. Thus, the crucial observation is that silicon is capable of storing over two orders of magnitude higher mechanical energy densities than quartz. This partly compensates for the small size of the microresonators in their power handling capacity. It should be noted that the maximum power output is not limited by the dissipation-related self-heating effects that are not a dominant factor in the demonstrated resonator due to high thermal conductivity in silicon.

The rather high bias voltage is a direct consequence of the large 0.75-μm electrode gap used in the prototype. With an additional mask and fairly straightforward modification of the fabrication process, it is possible to fabricate 60-nm gaps [10]. The electromechanical transduction factor scales as $\eta \sim U_{\text{bias}}/d_0^2$, and thus reducing the gap to 100 nm would allow a motional impedance of 64 Ω at 15-V bias voltage.

V. OSCILLATOR DEMONSTRATION

Fig. 3 shows the noise-to-signal ratio for an oscillator based on a discrete amplifier circuit (Philips BF545B) connected in series feedback configuration with the square-extensional resonator inside a vacuum chamber ($p < 0.01$ mBar). The resonator bias voltage was $U_{\text{bias}} = 75$ V and the noise level of the dc-source was less than 1 μV/$\sqrt{\text{Hz}}$. The vibration amplitude was limited to $x_{\text{vib}} = 33$ nm by the nonlinear gain characteristics of the amplifier circuit keeping the resonator in the
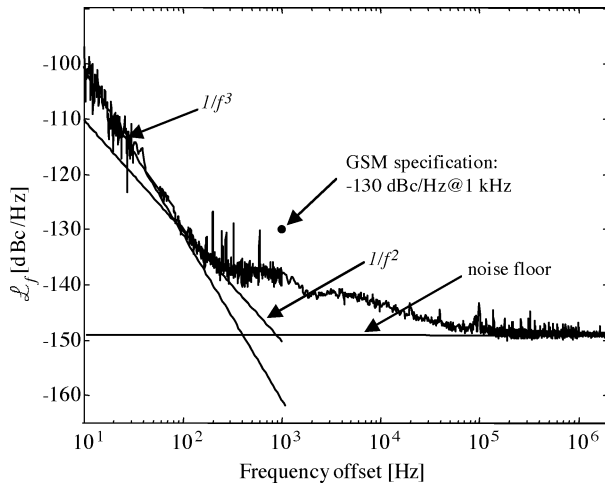
Fig. 3. Single-side band noise spectrum measured using Agilent series E5500 phase-noise measurement system. Spurious peaks have been removed. Resonant frequency is 13.1 MHz and drive level is 37 μA.

linear operation regime. To the authors' knowledge, the oscillator performance (-138 dBc/Hz at 1 kHz, noise floor -150 dBc/Hz) is the best reported for a MEMS based device and the first one to satisfy the GSM-specifications for the phase noise (typically -130 dBc/Hz at 1 kHz) typically achieved only with macroscale oscillators such as quartz crystals. Practical oscillator implementations utilize automatic gain control to limit the oscillation amplitude, which could further improve the phase noise performance.

VI. CONCLUSION

This letter demonstrates for the first time that in terms of phase noise, RF-MEMS can be a viable alternative to macroscale quartz resonators. Measured phase noise of -138 dBc/Hz

at 1 kHz offset from the carrier is made possible by a new microresonator that offers high quality factor and high maximum drive level. For reference oscillator applications the temperature and long-term stability of the resonator will need to be addressed and these issues are under investigation.

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Appendix V

"Plug-up"–a new concept for fabricating SOI MEMS devices

J. Kiihamäki, J. Dekker, P. Pekko, H. Kattelus, T. Sillanpää, T. Mattila

Abstract This paper reports a novel process sequence for fabricating micromechanical devices on silicon-on-insulator (SOI) wafers. Among the merits of the described process are its improved immunity to stiction and elimination of conductor metal endurance problems during sacrificial etching in hydrofluoric acid. With this novel process one can controllably embed vacuum cavities within SOI substrates. Further processing of such cavity wafers enables realization of a wide variety of micromechanical devices based on single crystalline silicon or even integrated read-out circuitry.

1
Introduction

In recent times, conventional surface and bulk micromachining have been rivalled by the so-called Silicon-on-Insulator (SOI) micromechanics. This technology is based on direct wafer bonding combined with advanced silicon dry-etching techniques. The buried silicon oxide is used as a sacrificial layer in an analogous way to the well-known surface micromachining technology. The use of bonded SOI wafers as starting material for micromechanical devices was introduced by E. H. Klaassen [1], as wafer bonding and new deep silicon etching [2] methods were quickly developing. SOI micromachining makes use of single crystalline silicon, which shares or surpasses the excellent mechanical properties of polysilicon and additionally carries very low intrinsic stress, which would be very difficult to reach using chemical vapour deposited thin films. In the standard approach, a SOI-based device is fabricated by pattern-etching access windows into the structural layer of the SOI, followed by local sacrificial oxide removal in concentrated hydrofluoric acid (HF), as

shown in Fig. 1. Contact metallisation is added for wiring purposes. The basic dual-mask process is very simple but suffers from certain limitations:

1) Metallisation. If the conductor and pad metallisation is formed in an early phase, as shown in Fig. 1 (Standard), it will be exposed to the aggressive HF-based silicon dioxide etchant during the subsequent release etching cycle. The selection of IC-compatible metals that are inert and well adhering in HF is very limited. Additionally, the metal should also form good ohmic contact to with silicon and be easily bondable. On the other hand, if the sacrificial etching were performed prior to depositing and pattern-etching the metallisation, lithography would be difficult over the high topography steps existing on the wafer.

2) Stiction. Another issue that has retarded the emergence of SOI micromachined devices on the consumer market is the phenomenon called stiction. It is associated with the atomic-scale smoothness of silicon-oxide interfaces in SOI. The perfectly polished wafer surface is a prerequisite for successful bonding and SOI wafer fabrication, but unfortunately it is also the most important source of failure. If the delaminated membrane or beam is intentionally or accidentally brought into direct physical contact with the carrier wafer, the micromechanical structure sticks permanently to the substrate.

The literature offers many descriptions of possible solutions to the above problems. One can use modified etching solutions that do not readily attack aluminium, or noble metals to replace Al. Stiction in SOI is more difficult to avoid. Our procedure called Plug-up and introduced in Fig. 1 tackles both of these problems. Metallisation can be prepared over smooth topography after cavity formation and polysilicon bumps limit the area in case of possible physical interface contact. The Plug-up sequence makes use of liquid-permeable polysilicon [3–5]; the details of the fabrication sequence are given in the Experimental section.

Vacuum shells have earlier been studied for making a wafer-level vacuum environment for improving the resonator Q value [5, 6] or for protecting micromechanical devices from the environment. The sacrificial layer is usually removed via lithographically patterned etch holes [6, 7] or via semipermeable polysilicon [3–5].

An optional way to make comparable cavity wafers would be pre-processing of the wafers prior to bonding and thinning [8]. The Plug-up procedure's advantages over that system include (1) membranes of constant thickness, (2) front-side alignment marks remain on the

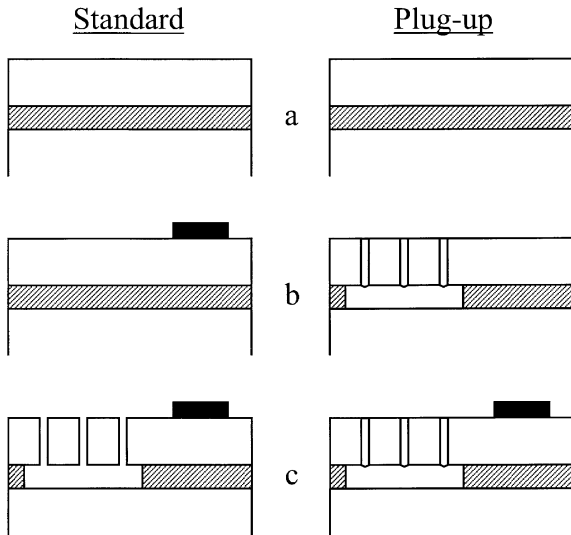Standard   Plug-up

a

b

c

Fig. 1a–c. Schematic process flow of the standard SOI process sequence (left) and Plug-up sequence (right)

wafer, (3) aligned bonding is not needed, (4) MEMS manufacturer does not need bonding, grinding or polishing equipment, (5) bumps preventing stiction are simple to prepare, and (6) pressure inside the cavity is mainly determined by the closing method and not by the atmosphere of bonding.

2
Experimental

2.1
Sample preparation
The Plug-up sequence is schematically presented in Fig. 2. The starting material is micromechanical bonded SOI with 5–20 μm device layer thickness and 1–2 μm thick buried oxide over the low-resistivity carrier wafer. After deter-
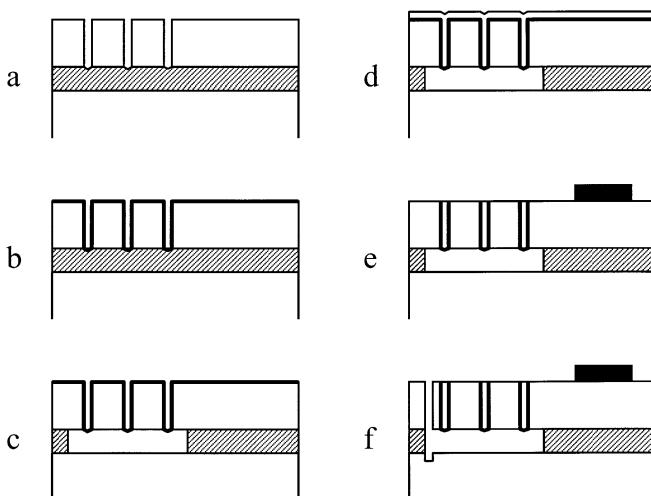
Fig. 2a–f. Schematic process flow of the Plug-up sequence. **a** Perforation of structure layer, **b** deposition of HF permeable polysilicon, **c** sacrificial etching, **d** closing of cavities, **e** metallisation (back-end) **f** optional release of horizontally moving structures

mining the area to be delaminated from the substrate, its interior is patterned into an array of 1–2 μm wide circular or square-shaped dots. These are replicated into the device layer of SOI through ICP etching using the Bosch process in STS ASE. The subsequent HF dip attacks the buried oxide slightly, as shown in Fig. 2a. A thin layer of polysilicon is then deposited using the low-pressure chemical vapour deposition (LPCVD) technique by controlling the deposition parameters in such a way that the film contains a controlled density of nanometer-scale pinholes [5]. The areal density of the pinholes must exceed $1/\mu m^2$ in our geometry (Fig. 2b). Immersing the wafer in HF results in local removal of the buried oxide (Fig. 2c). After careful rinsing and drying, pinhole-free polysilicon is deposited over the wafer to completely plug up the holes (Fig. 2d). The pressure inside the cavity remains in the 100 Pa vacuum range where the deposition process takes place. After etch-back, the cavity wafer is rigid, identical to standard SOI wafers from the fabrication point-of-view, and a variety of processing steps can be performed on it without difficulty, including any standard metallisation (Fig. 2e). Some device types like pressure sensors or ultrasonic transducers do not require further processing after this, while others may still call for relief of laterally moving resonators, comb electrodes or other features. Such a release step can now be made with high-yield dry processing (Fig. 2f).

2.2
Characterisation
After sacrificial layer etching, the delaminated area was inspected using a microscope equipped with an infrared-sensitive video camera [10]. The near-infrared wavelengths available were able to transmit the typical device layer thickness in micromechanical SOI. Membrane deflection by atmospheric pressure (LPCVD vacuum inside cavity) was measured using a stylus force of 0.5 mg in the Dektak V200 profilometer. Resonance frequencies of completed micromechanical devices were characterised at wafer level using an impedance analyser (HP4294A) and probe station. The vacuum measurements were performed on diced and encapsulated devices using a network analyser (HP4396B) and temperature-controlled vacuum chamber.

2.3
Device examples
Absolute pressure sensors were fabricated with monolithically integrated read-out electronics. These results will be reported in detail elsewhere [12]. Capacitive micromachined ultrasonic transducers were also fabricated using the Plug-up technology on SOI. Transmission and detection of ultrasound were demonstrated.

3
Results and discussion
Infrared microscopy reveals that sacrificial layer etching through the polysilicon pinholes is a reliable process (Fig. 3a). With the pinhole density produced by our polysilicon deposition, all wells are transparent to the HF etchant and the etching product flow when the well diameter exceeds about 1.2 μm. For refill and etch-back
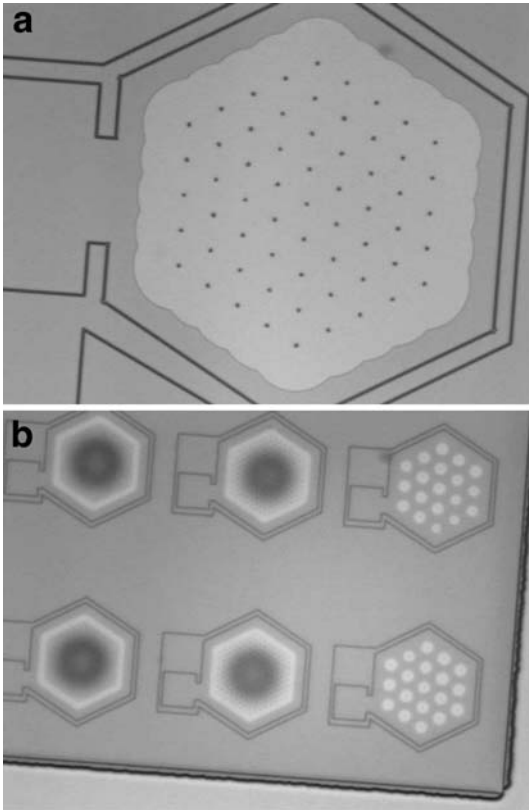
Fig. 3. a Near IR image of hexagonal cavity after sacrificial etching, **b** IR images of hexagonal cavities after closing and etch-back with different perforation hole patterns
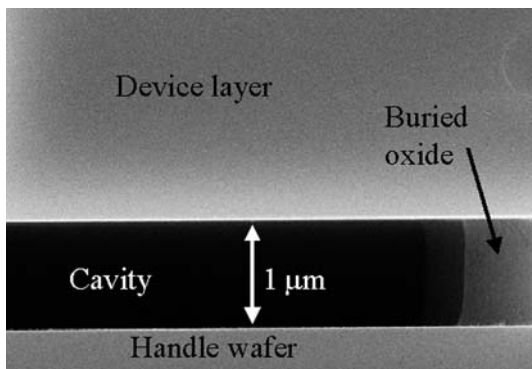

Fig. 4. Detail of the inside of the cavity. The walls of the cavity are clean and no films are deposited inside the cavity

layer thickness of 8 μm. The low accuracy of the profilometer measurement is caused mainly by difficulty in setting the scan line precisely over the centre of the cavity. During enclosure, practically no deposition occurs through the pinholes onto the cavity walls, as can be seen in the SEM micrograph of Fig. 4.

An SEM micrograph of an anti-stiction bump formed on the bottom of the membrane by a short HF dip is shown in Fig. 5. Driving a membrane with dimensions comparable to those shown in Fig. 3 electrostatically against the substrate does not result in stiction. The polysilicon plugs constitute a negligible portion of the structural layer, and single crystalline silicon dominates the mechanical properties of the devices.

No notching was seen at the bottom of the structure layer when laterally moving structures and air holes for breaking the vacuum cavity were dry-etched onto the structure layer. Typically notching is seen when high aspect ratio trenches are etched and an insulating etch stop layer is used [13]. However, when etching is done above the vacuum cavity, there is no insulator layer that can be charged and notching is avoided. A SEM micrograph of a released beam without notching is shown in Fig. 6.
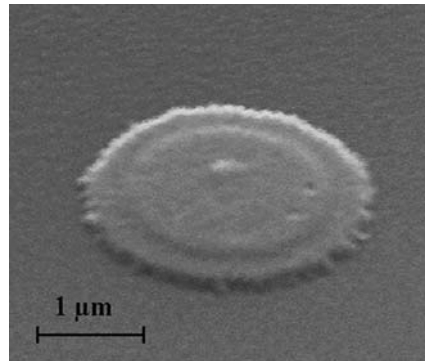

Fig. 5. SEM micrograph of an anti-stiction dimple formed by wet etching on the bottom of the structure layer
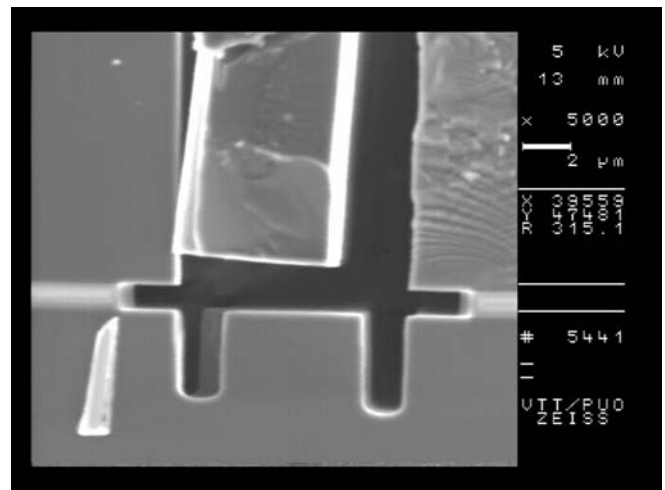
processes use of the smallest possible trenches would be advantageous, but when using sub-micron well diameters the fluid flow may be restricted at some locations and not all membranes are fully delaminated from the substrate. The reason is either inadequate deep etching or lack of pores in the thin polysilicon layer at the bottom of the small trench. In Fig. 3b, successful encapsulation of the cavities in a vacuum by a pinhole-free polysilicon overcoat is observed through membrane deflection. Grey shades resulting from interference appear in the near-infrared photograph. The deflection of the membrane was quantified with a low contact force stylus profilometer to be about 300 nm for a 250 μm wide hexagon for a device

Fig. 6. Cross-section of a beam above a Plug-up cavity. Etching is continued to the substrate and no notching occurs

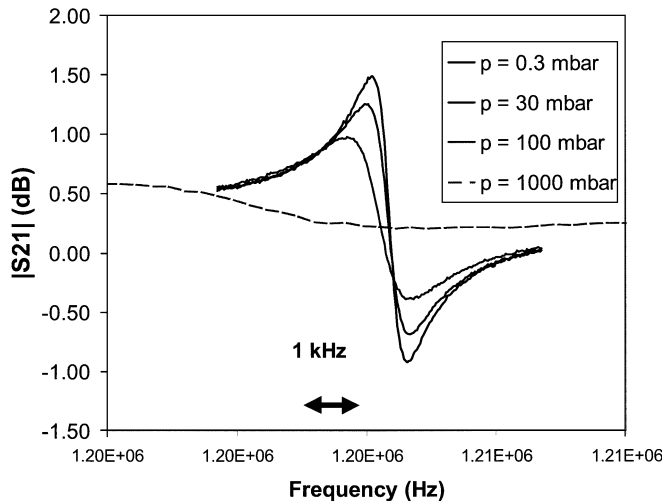**Fig. 7.** Measured resonance peak of a hexagonal cavity resonator, external pressure as a parameter

Fig. 8. (Top) Ultrasonic transmitter/receiver configuration. (Bottom) Input and output waveforms of the ultrasonic flow measurement setup

Resonance frequencies of enclosed test membranes were measured inside a vacuum chamber by varying the chamber pressure. A set of resonance curves for a hexagonal 300 μm diameter resonator of 8 μm thickness is shown Fig. 7 with the pressure of the measurement chamber as a parameter. The Q value under in an external vacuum is around 1000 and in atmospheric pressure about 200. The resonance frequency shifted with temperature according to the temperature coefficient of Young's modulus for single crystal silicon.

Absolute pressure sensors were fabricated using the Plug-up technology for pressure ranges up to 500 kPa. CMOS-based readout circuitry was monolithically integrated. For a flat circular plate of constant thickness and uniformly distributed load (pressure) over an entire surface, the deflection can be determined as follows [9]:

$$\delta = \frac{3\, p\, r^4 \left(1 - v^2\right)}{16\, E\, t^3} \quad ,$$

where p is the applied pressure, r is the radius of the cavity, v is the Poisson ratio and E is Young's modulus for the plate material, and t is the plate thickness. Because the sensitivity is proportional to the fourth power of the membrane radius, a well-controlled lateral etching rate of the sacrificial oxide is a prerequisite. Pressure sensors were successfully demonstrated [12].

Another practical device demonstrator realized using the Plug-up cycle on SOI was a capacitive micromachined ultrasonic transducer (cMUT). A matched pair of closed cavities was used as an ultrasonic transmitter and receiver at the resonance frequency of 1.78 MHz; a schematic description of such a system is given in Fig. 8. It takes about 60 μs for a sound wave to travel the separation distance of 20 mm. The dashed line is the AC voltage applied to the transmitter and the solid line is the output voltage of the detecting circuit. The receiving sensors are excited in their mechanical resonances and it takes several periods before the amplitude reaches its maximum. The bias voltage across the sensors was 60 V.
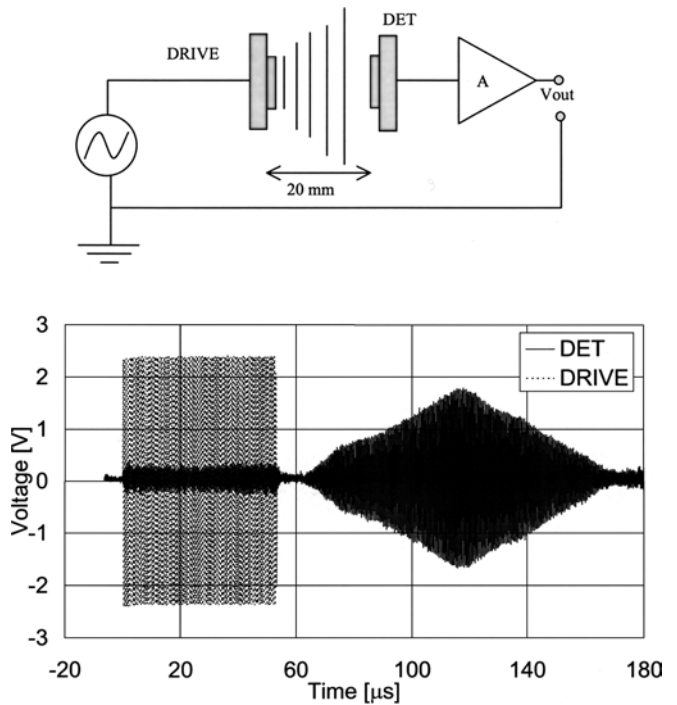
4
Conclusions

This paper describes a novel process for making micromechanical SOI devices with an abundance of advantages over the conventional methods. The key issue in this process is the controlled formation of hermetically sealed cavities in the SOI structure and the resulting clean single crystal surface after the etch-back steps, which enables versatile back-end processing. The quality of the resulting single crystal devices is good and they do not show any signs of degradation due to processing. Monolithical integration with active electronics is possible in a synergetic manner, so that several fabrication steps are common for electronic and mechanical devices [11]. An absolute pressure sensor and an ultrasonic transmitter-receiver pair are presented as device examples. Dicing and packaging of such hermetically sealed devices is quite straight-forward. Fabrication of open structures is also possible using Plug-up technology with the advantage of dry processing for structure relief.

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Appendix VI

MODULAR INTEGRATION OF CMOS AND SOI-MEMS USING "PLUG-UP" CONCEPT

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ABSTRACT

This paper reports a novel method for monolithic integration of electronics with micromechanical devices. The fabrication sequence differs from those previously described. Even though some of the elements of CMOS and MEMS fabrication are intermixed and make use of each other, they still are modular packages, which can be sequentially fabricated in separate specialized factories if both of the technologies are not available at one site. Standard or tailored SOI wafers can be used for the substrate material. Vacuum cavities are then made at predetermined regions of the buried oxide using a special technique, "Plug-up" [1]. We have demonstrated that cavity wafers of this kind can progress through the entire bipolar enhanced CMOS cycle without complications. In the end, MOS and bipolar transistors operate almost identically to reference devices on bulk silicon wafers and MEMS membranes resonate mechanically as anticipated. The proposed modular process sequence is tabulated in Fig. 1.

INTRODUCTION

Micromachined vacuum shells [2] have been studied for improving Q-values of resonators, for hermetical sealing of devices, or for realizing capacitive micromachined ultrasonic transducers [3]. The plug-up concept we have developed combines deep reactive ion etching (DRIE) of silicon [4] and SOI micromachining [5] with semipermeable polysilicon technology [2,3,6] providing a robust starting material for integrated MEMS.

There are other ways of forming buried cavities within SOI described in literature [7]. Usually they are based on making recesses on one of the wafers prior to bonding.

This approach suffers from non-uniform membrane thickness, loss of alignment marks in wafer thinning, and need for intimate discussion between wafer manufacturer and device designer.

There are some process descriptions of integrated MEMS in the literature[8,9]. Usually they suffer from compromises made between the two technologies: polysilicon MEMS is difficult to prepare over the IC, or the IC must be fabricated after making complex embedded polysilicon structures. In either case device properties are compromised or expensive process technology is needed. In our modular approach, however, there is a synergy between MEMS and IC, both MEMS and IC are made of the same material and, for example, MEMS isolation can be used also for reduction of

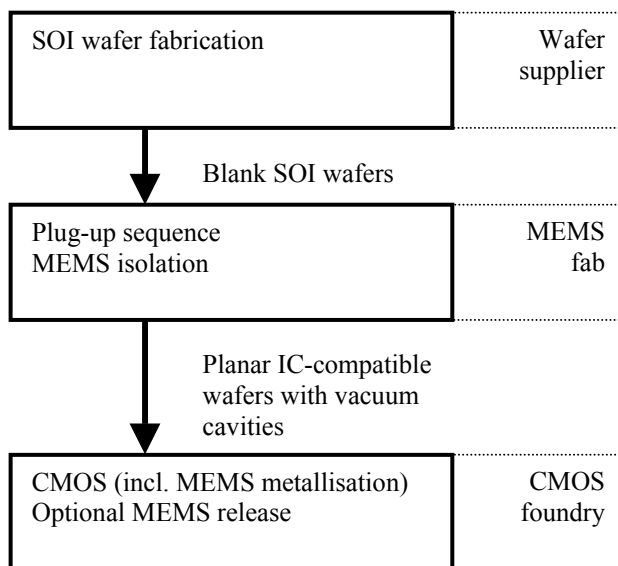transistor paracitic capacitances and the metallization structures are common for both.

Figure 1. Simplified example of modular process flow and interfaces between fabrication sites.

SAMPLE FABRICATION

Bonded silicon on inslulator (SOI) wafers are used as starting material. The handle wafer is heavily doped p-type silicon and the resistivity of the p-type structure layer is around 10 Ωcm to accommodate conventional CMOS. Structure layer and buried oxide thicknesses are 8 μm and 1 μm, respectively. The wafer processing is mostly done at VTT Information Technology facilities.

The vacuum cavities (schematically shown in Fig. 2.) are fabricated using Plug-up sequence[1] as follows:

1. An etch-stop layer is deposited on SOI wafers.
2. An array of approximately micron-sized openings is etched through the device layer of SOI with slight overetching into the buried oxide to form antistiction bumps.
3. Semipermeable polysilicon is deposited in such a way that pinholes remain at the bottom of each well.
4. Buried oxide is locally removed through pinholes and dried with super critical carbon dioxide.
5. The wells are plugged up with conformal layer of LPCVD polysilicon film deposited at 150 mTorr. The cavities remain in vacuum.
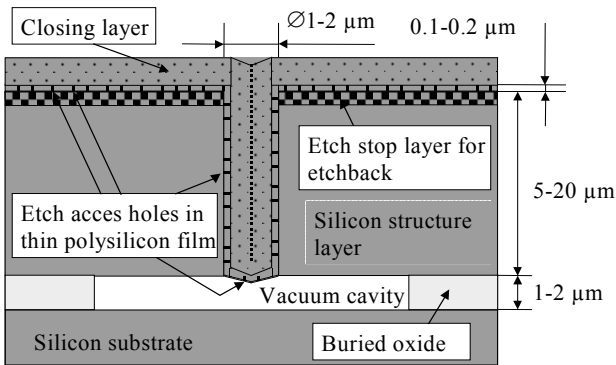6. After etchback, the IC-compatible, single crystal silicon surface is revealed.

Figure 2. Schematic cross-section of a plugged-up SOI cavity before etchback with typical dimensions.

Besides the active cavities for microelectromechanical devices substrate contacts and isolation trenches are generally needed. The shematical cross-section of these sub-modules is shown in Fig. 3. In this study the integrated substrate contacts were omitted and contacts were made externally after dicing. In the future runs in-situ doped polysilicon will be used for substrate contacts. The DRIE etched isolation trenches are refilled with oxide after cavity formation, just before the formation of CMOS wells. During the cavity formation the area designated for CMOS is protected by a stack of selected thin films. The level of metallic impurity caused by the cavity forming process remained at an acceptable level which was verified by total reflection X-ray fluorescence (TXRF) measurement of test samples after deep silicon etching and super-critical carbon dioxide drying.
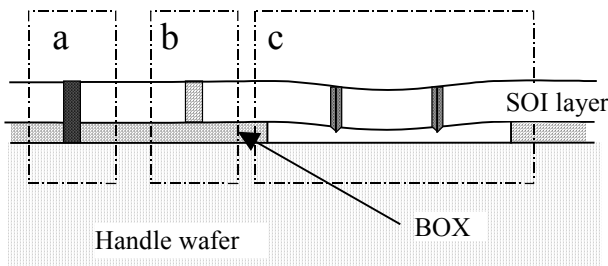
Figure 3. Breakdown of MEMS parts, a) electrical substrate contact through SOI buried oxide, b) trench isolation, c) vacuum cavity.

The top view infrared photograph of cavity test structures in shown in Fig. 4. The dark center of the hexagons indicates that the silicon membrane above the cavity is deflected by the atmospheric pressure. The light separated spots are small cavities formed from individual access holes which have not yet merged to form a continuos cavity.

The integrated circuit process selected for this demonstration is a 1 μm gate length bipolar enhanced CMOS. The BeCMOS process is optimised for analog and mixed-signal circuits. It uses a p-type substrate with triple well. Besides the standard n- and p-wells the process has a deep n-well with a shallow p-well inside it. This structure is used for isolating analog NMOS transistors and vertical pnp transistors. An extra well was added to the MEMS region to enhance the conductivity of the structure layer. The higher doping level is needed to reduce the temperature and voltage sensitivity of the anchor area of MEMS devices. Tailoring of the stucture layer doping profile by blanket implantation before wafer bonding is also an alternative to make the top electrode more conductive.

The bipolar transistors are processed before the CMOS gate process. Both npn and pnp transistors have conventional triple diffused structure with implanted emitters. CMOS portion of the process uses self-aligned molybdenum gate with 20 nm gate oxide. Molybdenum gate metal is used also as a bottom electrode for metal-insulator-metal capacitors. Stacked floating gate MOS transistors with capacitively connected control electrodes are used as EEPROM memory cells. The key properties of the processed circuit elements are tabulated in the Table 1. Most of the circuit elements are modular and they can be omitted from the fabrication process if so desired. The high voltage NMOS is an important option if electrostatic drive of capacitive elements is required.
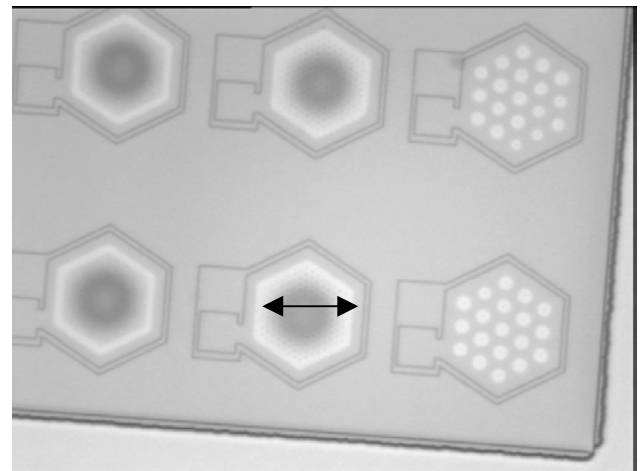

Figure 4. Near infrared photograph of hexagonal MEMS cavities with varying perforations. The marker is about 300 μm long.

RESULTS AND DISCUSSION

Modular integration using the plug-up process was demonstrated in practice. The processed NMOS, PMOS, npn, and pnp operate similarly to reference devices on plain silicon wafers. The leakage currents remained practically unaltered. The membranes within the MEMS regions are deflected downwards by ambient pressure as was verified by profilometry and near infrared microscopy. They also resonate at the expected frequency and with the expected mechanical quality factor, which proves the ability to release structures to withstand the CMOS cycle. The CV-measurement result in Fig. 5

Element	Notes
NMOS	VTH = +0.60, molybdenum gate
PMOS	VTH = -0.65, molybdenum gate
isolated NMOS	VTH = +0.60, with deep n-well isolation
vertical npn	HFE ~ 100, VA ~100
vertical pnp	HFE ~ 30, VA~50, with deep n-well isolation
EEPROM memory cells	floating NMOS/PMOS and capacitor nitride
High voltage NMOS	Breakdown voltage 40 Volt
Thin film capacitor	Metal-insulator-metal, 2 nF/(mm)^2
Thin film resistor	10 kOhm/sqr, TCR < 100 ppm/°C

Table 1. List of processed circuit elements of the modular BeCMOS

shows well behaving capacitance voltage characteristic. The apparent asymmetry is a measurement artefact of a wafer level capacitance measurement. The temperature sensitivity of the resonance frequency of the silicon membrane is governed by the temperature sensitivity of Young's modulus of silicon. Fig. 6. shows the typical spring softening effect when the dc-bias on the resonator is increased. The approximate Q-value of such a resonator is in the range of hundreds when operated in atmospheric pressure. In vacuum the Q-value is about 1000. The mechanical losses are due to energy leakage at the edge of the device where the membrane is connected to the surroundings.
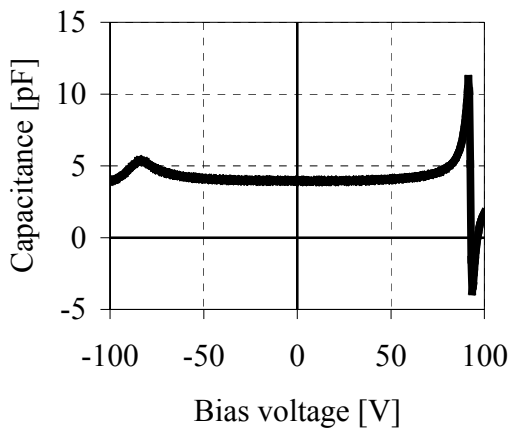
Figure 5. CV-measurement of a fabricated cavity. Mechanical resonance occurs at ± 85 V when measured at fixed 1 MHz frequency of the capacitance bridge.

Comparison of the electrical performance of SOI device with MEMS process and bulk device is shown in Fig. 7. It shows the drain leakage current in high voltage NMOS transistor with gate connected to ground. Below the breakdown voltage the current levels are the same, so the MEMS process has no adverse effecton the IC process.
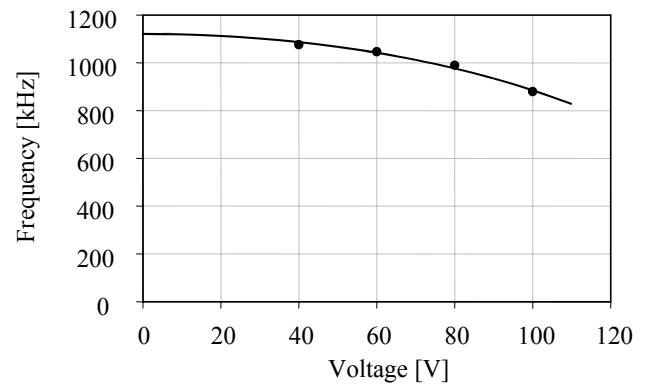

Figure 6. Resonance frequency of a hexagonal cavity resonator as a function of dc-bias voltage showing typical spring softening effect.
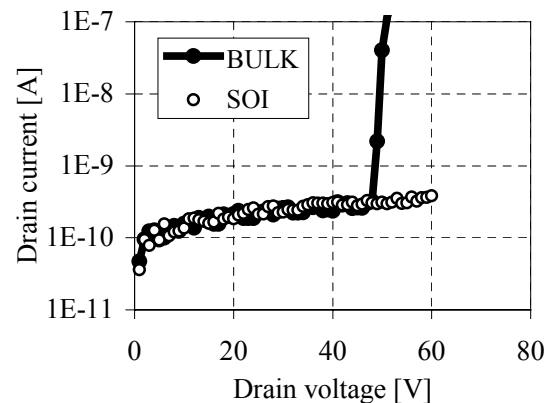

Figure 7. Drain leakage current in bulk and SOI (with MEMS) circular (outside diameter 30 μm) high voltage NMOS transistors with gate dimensions of W=27 μm and L=2.4 μm.

CONCLUSIONS

The complete analog BeCMOS was successfully processed on wafers having preprocesssed plug-up vacuum cavities. The cavity formation by plug-up sequence was shown to be CMOS compatible though effort is still needed in development of the sacrificial

etching and the super-critical carbon dioxide drying procedures.

The key advantage of the plug-up sequence is the fact, that sacrificial oxide etching using HF is done prior to all metallisation steps or gate dielectric growth. Inside of a closed cavity is clean and hermetically sealed.

This method of MEMS/CMOS integration enables modular fabrication of MEMS systems and it can act as a versatile process platform for a vast range of applications.

Acknowledgements

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Title
Fabrication of SOI micromechanical devices

Abstract

This work reports on studies and the fabrication process development of micromechanical silicon-on-insulator (SOI) devices. SOI is a promising starting material for fabrication of single crystal silicon micromechanical devices and basis for monolithic integration of sensors and integrated circuits. The buried oxide layer of an SOI wafer offers an excellent etch stop layer for silicon etching and sacrificial layer for fabrication of capacitive sensors. Deep silicon etching is studied and the aspect ratio dependency of the etch rate and loading effects are described and modeled. The etch rate of the deep silicon etching process is modeled with a simple flow conductance model, which takes into account only the initial etch rate and reaction probability and flow resistance of the etched feature. The used model predicts qualitatively the aspect-ratio-dependent etch rate for varying trench widths and rectangular shapes. The design related loading can be modeled and the effects of the loading can be minimized with proper etch mask design.

The basic SOI micromechanics process is described and the drawbacks and limitations of the process are discussed. Improvements to the process are introduced as well as IR microscopy as a new method to inspect the sacrificial etch length of the SOI structure.

A new fabrication process for SOI micromechanics has been developed that alleviates metallization problems during the wet etching of the sacrificial layer. The process is based on forming closed cavities under the structure layer of SOI with the help of a semi-permeable polysilicon film.

Prototype SOI device fabrication results are presented. High Q single crystal silicon micro resonators have potential for replacing bulky quartz resonators in clock circuits. Monolithic integration of micromechanical devices and an integrated circuit has been demonstrated with the developed process using the embedded vacuum cavities.

The work deals with microfabrication on silicon-on-insulator (SOI) wafers for micromechanical devices. Silicon microsystems technology (MST) or micro-electromechanical systems (MEMS) are emerging technologies that utilize the excellent mechanical properties of silicon, especially in its single crystal form.

Deep reactive ion etching of single crystal silicon and its applications in SOI micromachining are studied in this thesis. Its characteristics and shortcomings are reviewed thoroughly. Fabrication processes for simple SOI devices are described and the developed improvements to some common processing problems are introduced. Finally, a unique way to monolithically integrate mechanical devices and electronic circuits is presented. The performance obtained with the processed SOI sample devices shows potential for some very large volume commercial applications such as pressure sensing and frequency references.

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