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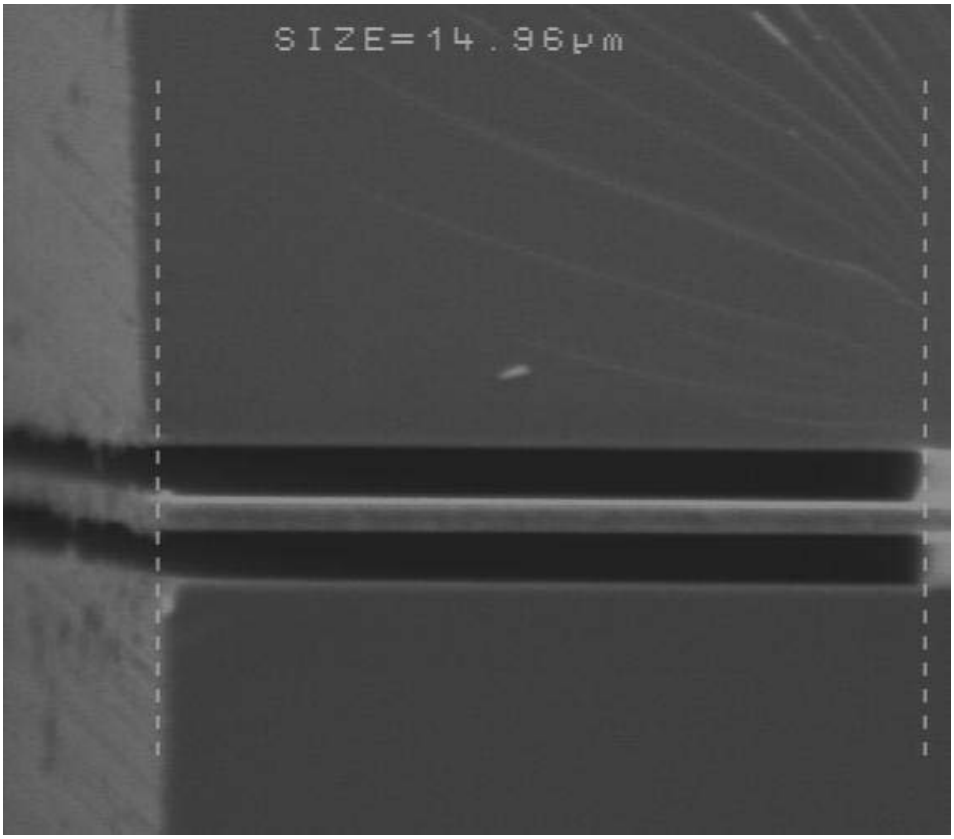

Tommi Suni

Direct wafer bonding for MEMS and microelectronics

VTT PUBLICATIONS 609

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Tommi Suni

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Keywords direct wafer bonding, MEMS, microelectronics, microelectromechanical systems, SOI, silicon-on-insulator, integrated circuits, bond strength measurement, heterogeneous integration, pre-processed SOI fabrication, wafer-scale packaging, plasma activation

Abstract

Direct wafer bonding is a method for fabricating advanced substrates for microelectromechanical systems (MEMS) and integrated circuits (IC). The most typical example of such an advanced substrate is the silicon-on-insulator (SOI) wafer. SOI wafers offer many advantages over conventional silicon wafers. In IC technology, the switching speed of circuits fabricated on SOI is increased by 20-50% compared to circuits fabricated on a bulk Si wafer. The required operation voltage is lower in ICs on SOI than in ICs on a bulk silicon wafer, which decreases power consumption and chip heating. In the MEMS industry, the buried oxide layer works as a good sacrificial layer during release etching of diaphragms, beams etc. and offers an excellent etch stop layer for silicon etching. Direct wafer bonding can also be used in the fabrication of more complex structures than SOI. The wafers to be bonded can be of different materials, can contain patterns, and may have multiple layers or ready-made devices.

This thesis reports on studies of direct wafer bonding and its use in various applications. Different bonding processes used in microelectronics are briefly described. The main focus of this thesis is on the plasma activation-based low temperature bonding process, and on the control of bond strength by surface preparation.

A novel method for bond strength measurement is introduced. This method, based on buried oxide etching, is presented and compared with other methods used in evaluating bond quality.

This thesis also contains results on research of different applications requiring direct wafer bonding. Heterogeneous integration, pre-processed SOI fabrication, and wafer scale packaging are the main application topics.

Suni, Tommi. Direct wafer bonding for MEMS and microelectronics [Puolijohdekiekkojen suoraliittäminen mikroelektroniikan ja mikromekaniikan sovellutuksissa]. Espoo 2006. VTT Publications 609. 89 s. + liitt. 34 s.

Avainsanat direct wafer bonding, MEMS, microelectronics, microelectromechanical systems, SOI, silicon-on-insulator, integrated circuits, bond strength measurement, heterogeneous integration, pre-processed SOI fabrication, wafer-scale packaging, plasma activation

Tiivistelmä

Puolijohdekiekkojen suoraliittäminen on menetelmä valmistaa kehittyneitä alustoja mikroelektromekaanisille systeemeille (MEMS) ja integroiduille piireille. Yleisin tämänlainen kehittyneempi alusta on SOI-kiekko, jossa kantajakiekon ja varsinaisen komponenttipiikerroksen välissä on eristävä oksidikerros. Verrattuna tavallisiin piikiekkoihin SOI-kiekot tarjoavat useita parannuksia. Integroitujen piirien tapauksessa kytkentänopeus on SOI:lla 20–50 % nopeampi, käyttöjännite matalampi ja energian kulutus pienempi. MEMS-teknologiassa haudattu oksidi toimii uhrautuvana kerroksena kalvojen ja palkkien vapautusetsauksessa ja myös pysäytyskerroksena piin syövyttämisessä. Suoraliittämistä voidaan käyttää myös monimutkaisempien rakenteiden kuin SOI-kiekkojen valmistamiseen. Liitettävät kiekot voivat olla eri materiaaleista, kuvioituja tai sisältää valmiita komponentteja.

Tässä väitöskirjassa keskitytään pääasiassa korkean ja matalan lämpötilan suoraliittämiseen sekä liitoslujuuden kontrollointiin pintoja karhentamalla. Kirjassa esitellään lyhyesti myös muut kiekkoliitostekniikat.

Väitöskirjassa raportoidaan myös uusi menetelmä mitata liitoslujuus kahden kiekon välillä. Menetelmä perustuu haudatun oksidin märkäsyövyttämiseen ja sitä verrataan myös muihin raportoituihin liitoslujuuden mittausmenetelmiin.

Tämä väitöskirja sisältää myös tuloksia suoraliittämisen käyttämisestä muutamiin erilaisiin sovellutuksiin, kuten kiekkotason paketointiin, heterogeeniseen integrointiin ja esiprosessoitujen SOI-kiekkojen valmistukseen.

Preface

This work has been carried out at VTT Microelectronics. I would like to thank first my co-workers at VTT for their help and support. Especially I would like to thank Kimmo Henttinen and Hannu Luoto for their assistance in the experimental work as well as in writing the articles. I would also like to thank my advisor Dr. Jari Mäkinen and my supervisor Prof. Ari Lehto for their guidance during final writing process. Thanks also to Dr. Jukka Lahtinen and Dr. Anke Sanz-Velasco for pre-examining the thesis and for Prof. Nathan Cheung for agreeing to be my opponent in the public defence of the thesis.

A lot of people have also been helping me and pushing me forward during all these years of studying making the writing of this thesis possible, so special thanks to: Äiti, T. Fält, E. Valovirta, J. Niemistö, T. Kaskiala, R. Jansson, K. Kaskiala, V. Sompa, J. Ylikerälä, J. Repo, A. Hirvonen, I. Suni, M. Kulawski, S. S. Lau, T. Penttinen, T. Tuominen, O. Alanen, A. Laukkanen, A. Saaristo, T. Tulkki, T. Karila, S. Mustala, S. Nurmi and also to my father and to my brothers.

Espoo, July 2006

Tommi Suni

Contents

List of abbreviations and terms

AFM	Atomic force microscope
APCVD	Atmospheric pressure chemical vapour deposition
BOX	Buried oxide
Cap wafer	Also known as device wafer. Top wafer in SOI wafer, thinned to desired SOI thickness
CMP	Chemical-mechanical polishing/planarization
CTE	Coefficient of thermal expansion
Device wafer	See cap wafer
DIW	Deionized water
DSP	Double side polished (wafer)
FBAR	Film bulk acoustic resonator
GaAs	Gallium arsenide
Handle wafer	Bottom wafer in SOI, the wafer that is usually not thinned
IC	Integrated circuit
InP	Indium phosphite
IR	Infrared
LPCVD	Low pressure chemical vapour deposition
MEMS	Microelectromechanical system
NIR	Near infrared
OH	Hydroxyl

PECVD	Plasma enhanced chemical vapour deposition
RMS	Root mean square
SAM	Scanning acoustic microscope
SC-1	Standard cleaning 1, also known as RCA-1. Typical cleaning bath for silicon wafers which removes particles and makes the surface hydrophilic.
SEM	Scanning electron microscope
SIMOX	Separation by oxygen implantation, one way to fabricate SOI
Si-OH	Silanol
Smart Cut™	Hydrogen implantation based method to make thin silicon layers
SOG	Silicon-on-glass
SOI	Silicon-on-insulator
SOQ	Silicon-on-quartz
SOS	Silicon-on-sapphire
sSOI	Strained silicon-on-insulator
SSP	Single side polished (wafer)
TTV	Total thickness variation
UHV	Ultra-high vacuum
Void	Discontinuation on the bonded interface

List of publications

This work is based on the following papers (Publications **A–F**), referred to in the text by the relevant letter in bold:

List of appended publications:

A. T. Suni, K. Henttinen, I. Suni, and J. Mäkinen. Effects of plasma activation on hydrophilic bonding of Si and SiO_2. Journal of the Electrochemical Society, Vol. 149, No. 6, (2002), pp. G348–351.

B. T. Suni, K. Henttinen, A. Lipsanen, J. Dekker, H. Luoto, and M. Kulawski. Wafer scale packaging of MEMS by using plasma-activated wafer bonding. Journal of the Electrochemical Society, Vol. 153, No. 1, (2006), pp. G78–82.

C. T. Suni, K. Henttinen, J. Dekker, H. Luoto, M. Kulawski, J. Mäkinen, and R. Mutikainen. SOI wafers with buried cavities. Journal of the Electrochemical Society, Vol. 153, No. 4, (2006), pp. G299–G303.

D. T. Suni, J. Kiihamäki, K. Henttinen, I. Suni, and J. Mäkinen. Characterization of bonded interface by HF etching method. In Semiconductor Wafer Bonding: Science, Technology and Applications VII, edited by C. Hunt, H. Baumgart, S. Bengtsson, T. Abe, Electrochemical Society, pp. 70–75, 2003.

E. K. Henttinen, T. Suni, A. Nurmela, M. Kulawski, and I. Suni. Mechanical delamination for the materials integration. In Semiconductor Wafer Bonding: Science, Technology and Applications VII, edited by C. Hunt, H. Baumgart, S. Bengtsson, T. Abe, Electrochemical Society, pp. 359–367, 2003.

F. K. Henttinen, T. Suni, A. Nurmela, H. Luoto, I. Suni, V.-M. Airaksinen, S. Karirinne, M. Cai, and S. S. Lau. Transfer of thin Si layers by cold and thermal ion cutting. Journal of Material Science: Materials in Electronics, 14, (2003), pp. 299–303.

Author's contribution

In **Publication A**, the author planned the experimental work together with co-authors, performed the experimental work and wrote the manuscript with the help of the co-authors.

In **Publication B**, the author planned and performed the experimental work together with the co-authors and wrote the manuscript with their help.

In **Publication C**, the author planned and performed the experimental work together with the co-authors and wrote the manuscript with K. Henttinen.

In **Publication D**, the author planned and performed the experimental work and wrote the manuscript, taking into account comments by the co-authors.

In **Publication E**, the author planned the experimental work together with K. Henttinen and performed the experimental work together with other authors. The manuscript was written with K. Henttinen, taking into account comments by the other co-authors.

Publication F is a joint paper together with researchers from VTT, Okmetic Oyj, Tampere University of Technology and the University of California, San Diego. The main experimental work was planned and performed at VTT by the author and K. Henttinen. The manuscript was written by K. Henttinen and the author with the help of the other co-authors.

1. Introduction

Direct wafer bonding means joining two surfaces without intermediate adhesives or external force. If the surfaces are flat and clean, wafers bond together when brought into contact. The initial bond strength is usually weak. Therefore, a subsequent annealing step is generally carried out to strengthen the bond.

Direct bonding was first reported by Sir Isaac Newton in the 17th century. He observed a black spot surrounded by "Newton's rings" when a flat and a convex optical surface were brought into contact. [1]

Currently direct wafer bonding has many applications in the microelectronics industry. It is used to fabricate substrates for modern integrated circuits (SOI, SOG, SOS, sSOI), to stack many processed layers (3D-integration) and as a method to encapsulate MEMS devices. These different applications require usually more than just a typical silicon wafer bonding process (wafer contacting and annealing at 1100°C). Bonding of processed wafers or wafers with a large difference in thermal expansion coefficients requires a low-temperature bonding process. Surface preparation may also be required before wafer contacting, the most typical process steps being plasma activation, chemical cleaning and chemical-mechanical polishing.

1.1 Objectives of this thesis

The main objectives of this thesis were first to study low temperature direct bonding, then to develop bonding processes suitable for various applications, such as fabrication of silicon-on-glass (SOG), silicon-on-sapphire (SOS), and silicon-on-insulator substrates with buried cavities, as well as for wafer scale packaging of MEMS components. This study also introduces a bond strength measuring technique based on the etching of buried oxide with hydrofluoric acid. This method is suitable for evaluating the bond strength easily from ready-made SOI, diced samples and from small bonded areas, which are difficult or impossible to measure with the crack opening method. This thesis focuses on bonding of silicon, but the same requirements apply to bonding of other semiconductor materials as well: surfaces have to be flat, smooth and clean.

1.2 Summary of appended papers

This thesis includes six publications on the topic of wafer bonding.

Publication A reports on the influence of plasma activation on wafer bonding and lists measured bond strengths for different bonding process combinations.

Publication B describes two different methods for encapsulating MEMS devices at wafer level utilizing plasma activated wafer bonding.

Publication C reports some design rules for fabrication of pre-processed SOI wafers for MEMS applications.

Publication D describes a method for measuring the bond strength of samples where the crack opening method cannot be used. Characterization of the bond strength by measurement of the buried oxide etch rate is, for example, applicable to small chips, silicon-to-glass and silicon-to-quartz bondings, which are difficult or impossible to measure with conventional methods.

Publication E presents a method for controlling the bond strength between two wafers. Good bond strength control creates possibilities to fabricate substrates that would be difficult or impossible to achieve with conventional methods (e.g. single crystalline silicon-on-sapphire)

Publication F describes a cold-cut process for fabrication of thin film SOI and SOG wafers. It also describes the influence of boron doping and crystal orientation on surface energy of the implanted layer after various annealing temperatures, setting the requirements for the bonding process.

2. Bonding

Bonding in general means the joining of two pieces of the same or a different material together. Bonding can be divided into three categories: bonding with a conducting interlayer, with an insulating interlayer, or without an intermediate layer. All of these categories are used extensively in the microelectronics industry. The bonding methods and their advantages and drawbacks are listed in Table 1. In this thesis, the focus is on hydrophilic direct bonding and low temperature direct bonding. Direct bonding means that there is no intermediate layer between the wafers, and the wafer surfaces bond spontaneously.

Table 1. Bonding techniques used in microelectronics.

Techniques	Advantages	Drawbacks
Bonding without interlayer	Hermetic	Flat surface required
Anodic	strong bond	high-voltage, bond time, sodium glass
Direct	strong bond	high-T, very flat surface required
Low-T direct	low-T	very flat surface required
Metallic Interlayer	Hermetic, non-flat surface ok	specific metals required
Eutectic	strong bond	flat surface required
Thermocompression	non-flat surface ok	high forces
Solder	self-aligning	solder flow possible
Insulating Interlayer	non-flat surface ok	varies
Glass frit	hermetic, common in MEMS	large area, medium to high-T
Adhesive	versatile	non-hermetic

2.1 Direct bonding (high temperature)

Direct bonding or fusion bonding generally means any joining of two materials without an intermediate layer or external force. In principle, most materials bond

together if their surfaces are flat, smooth and clean. The principle of this method is simple: two flat, clean and smooth wafer surfaces are brought into contact and form a weak bonding based on physical forces. The physical forces can be van der Waals forces, capillary forces or electrostatic forces [2]. The wafer pair is then annealed at high temperature (in the case of hydrophilic Si at >1000°C) and the physical forces are converted to chemical bonds. A typical process flow for wafer bonding is presented in Figure 1. In the case of silicon, high temperature bonding falls into two categories: hydrophilic bonding, in which the bonded surfaces are silicon dioxide, and hydrophobic bonding, in which the surfaces are silicon.

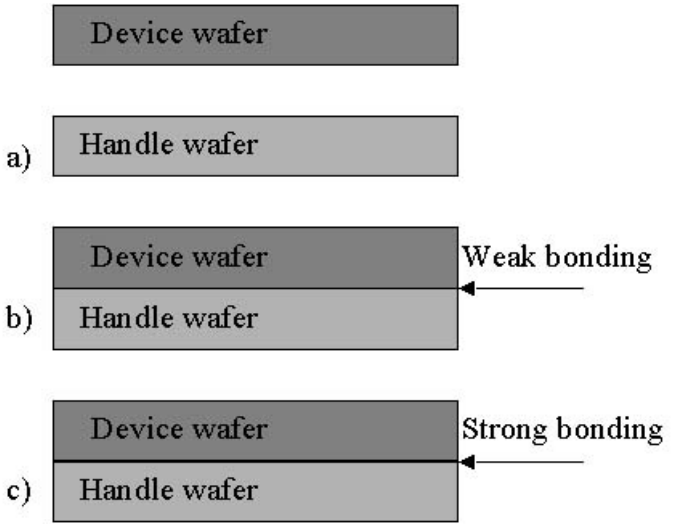

Figure 1. a) Surface preparations (e.g. cleaning, polishing, surface activation) b) Wafer contacting c) Annealing.

2.1.1 Hydrophilic high temperature bonding of silicon

Hydrophilic high temperature bonding is used commercially, for example, in SOI wafer manufacturing. The typical annealing temperature is ~1100°C. In hydrophilic bonding of silicon, the silicon wafer surface is covered with an oxide layer. The oxide can be a thin native oxide, thermally grown oxide or deposited oxide. The surface contains Si-O-Si and Si-OH bonds. It is the amount of Si-OH (silanol) groups on the surface that determines the hydrophilicity of the surface

due to polarization of the hydroxyl (OH) groups. The hydrophilicity of the surface can be enhanced with various methods, of which most popular is warm SC-1 (1:1:5 NH_3:H_2O_2:H_2O solution).

The reaction between two hydrophilic silicon surfaces during bonding is depicted in Figure 2. At the initial state after establishing contact between the wafers, water molecules form a "bridge" between the surfaces (Figure 2a). During annealing these water molecules diffuse out from the interface, dissolve into the surrounding material or react with surfaces increasing the number of silanol groups on the surface. Once these water molecules are removed, a bond is formed between silanol groups (Figure 2b). During further annealing, opposing silanol groups react according to reaction 1.

$$Si\text{-}OH + Si\text{-}OH = Si\text{-}O\text{-}Si + H_2O \quad (1)$$

During this reaction between silanol groups, more water molecules are released and Si-O-Si bonding is formed (Figure 2c).

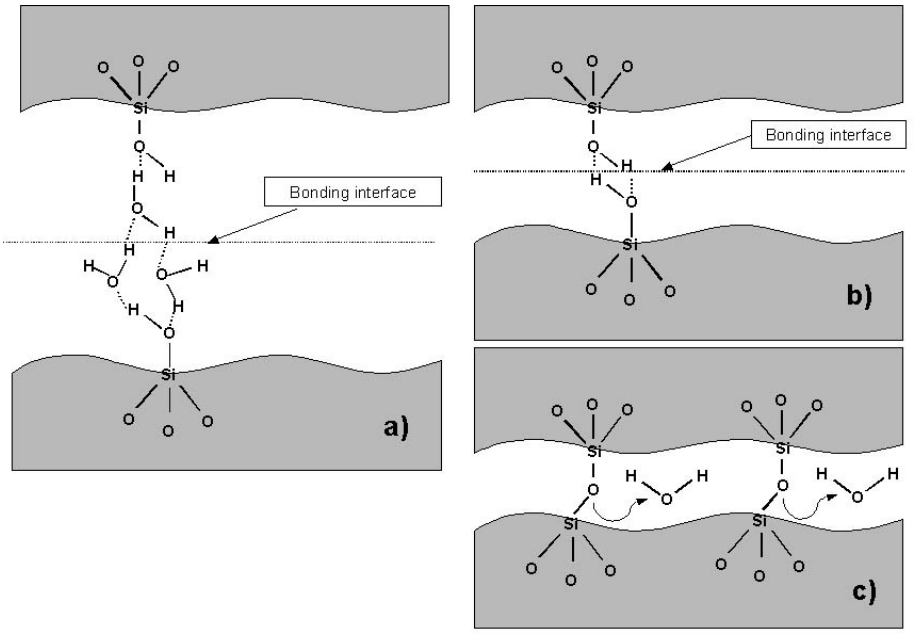

Figure 2. a) Bonding via intermediate water molecules, b) Bonding between two OH groups by van der Waals forces, and c) Formation of Si-O-Si bonds [2].

The water molecules diffuse into the silicon dioxide on the surfaces. If the water reaches the silicon, it reacts with it to form silicon dioxide and hydrogen.

$$Si + 2\ H_2O = SiO_2 + 2\ H_2 \qquad (2)$$

The remaining hydrogen does not react with silicon and may cause problems in the form of trapped gas, which is detectable with an IR camera or scanning acoustic microscopy (SAM) as voids (Figure 3). However, hydrogen has a high solubility into SiO_2 and by having an oxide layer of thickness > 50 nm on at least one wafer surface, hydrogen-induced voids can be avoided. The required amount of oxide on the surfaces for completely dissolving the hydrogen depends on the amount of water present at the interface. It can be enhanced by changing the hydrophilicity of the surfaces with different surface preparations and by using different bonding atmospheres.

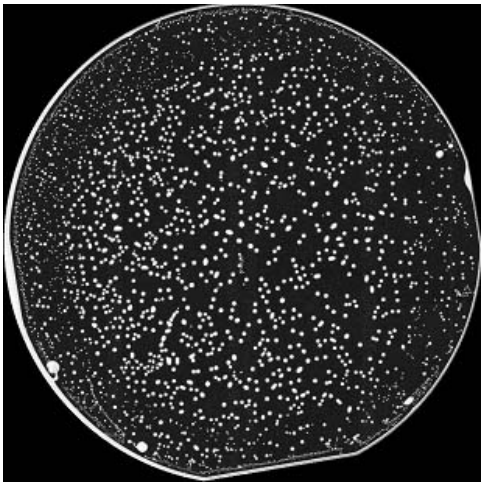

Figure 3. Hydrogen-induced voids in a bonded wafer pair. Both wafer surfaces had only ~2 nm thick native oxide, which cannot accommodate all of the hydrogen formed during the process.

2.1.2 Hydrophobic high temperature bonding of silicon

Hydrophobic bonding is a method for replacing epitaxial growth in some applications during fabrication of Si wafers with variously doped Si layers. For example, p-n junctions can be fabricated by bonding p-doped Si to an n-doped Si

wafer. It is also used to fabricate compliant substrates by twist bonding. In hydrophobic Si bonding, silicon is directly joined to another silicon wafer without an intermediate oxide.

In hydrophobic bonding, the wafers to be bonded have a bare silicon surface, which is either hydrogen and fluorine terminated or in some cases has dangling bonds on the surface. A hydrogen and fluorine terminated surface results from hydrofluoric acid etching, which is a standard process for removing silicon dioxide. The hydrophobic surface is quickly contaminated with hydrocarbons, therefore the wafers should be quickly contacted or stored in a vacuum after removal of the silicon dioxide layer [3].

The bonding process is illustrated in Figure 4. At first the HF molecules form a bridge between two silicon surfaces. At temperatures from 150°C-300°C, the HF molecules are rearranged and additional bonds are formed. During annealing at 300°C–700°C, hydrogen desorbs from the surfaces and Si-Si bonds are formed according to reaction 3 [2].

$$Si\text{-}H + Si\text{-}H = Si\text{-}Si + H_2 \qquad (3)$$

During annealing at >700°C, surface diffusion of silicon takes place and closes the microgaps between the surfaces [2]. The problem with the bonding process is again the presence of hydrogen at the bonded interface, which may cause voids.

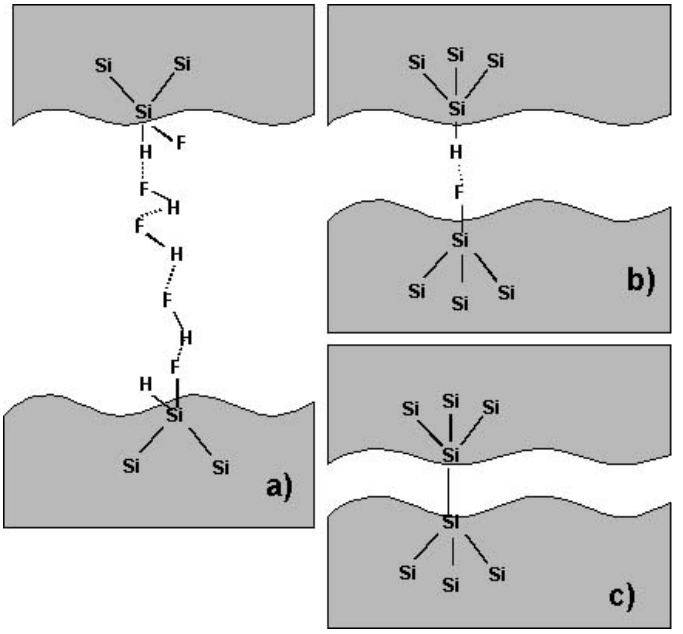

Figure 4. a) Bonding via HF molecules, b) Bonding via H & F atoms with van der Waals forces, c) Si-Si bonding formed after high-temperature annealing [2].

2.2 Low-temperature direct bonding

A low-temperature bonding process may be needed if the wafers are pre-processed, contain temperature-sensitive materials or components, or have different thermal expansion coefficients. The most common methods used for low-temperature hydrophilic direct wafer bonding are based on plasma activation [**Publication A**, 4, 5, 6, 7]. In these methods the wafer surface or surfaces is/are activated with short plasma treatment prior to wafer contacting. Numerous plasma processes have been reported for bond strengthening. The most often reported plasma gases are argon, nitrogen and oxygen. Sometimes it is advantageous to have a short wet cleaning step between activation and bonding [**Publication A**]. After this, a strong bonding is achieved at low temperatures (<400°C); even room-temperature processes have been reported [4, 5].

Different chemical activation methods have also been published [3, 2], but their effectiveness is not as good as plasma activation.

Low temperature hydrophobic wafer bonding is mainly done using ultra-high vacuum bonding [8, 9]. Other reported methods involve fabrication of an amorphous silicon layer by arsenic implantation, B_2H_6 or argon plasma treatment or sputter deposition [10].

2.2.1 Plasma activation based low-temperature bonding

The bond-strengthening influence of short plasma activation is clear and has been reported in numerous articles [**Publication A**, 4, 6, 5, 7]. However, the mechanism behind this effect is still unclear. This chapter gives an overview of the theories presented in the literature. The final answer may not be just one effect of the plasma but a combination of many.

During plasma treatment, many processes take place simultaneously. The plasma contains charged and neutral particles. The charged particles can be ionized atoms or molecules and electrons. These particles can react chemically with the wafer surface. During plasma processes a bias voltage is usually applied. This induces bombardment of the particles on the wafer surface, creating a sputtering effect. During plasma processes, UV radiation is also formed and it can have an effect on the chemistry of the wafer surface by breaking Si-O and Si-H bonds [11].

It has been reported by Farrens et al. that the oxide layer thickness on silicon wafer increases by 1–1.5 nm during oxygen plasma exposure. They believe that this oxide layer contains free radical ions from the plasma, which enhance the bond strength at low temperatures by increasing the atomic mobility of reacting species at the interface. [5]

The plasma has also been found to create highly hydrophilic surfaces. Reiche et al. have measured contact angles of below 2° between water droplet and wafer surfaces after plasma exposure. This behaviour has been found to last for several days. [7]

The influence of plasma exposure on the surface roughness has been reported by many research groups [7, 12, 13]. The data is controversial because some results show roughening [7] and some smoothening [12, 13] of the surface. In

Publication A, short Ar plasma treatments (30 s) showed no roughening or smoothening effects on Si, but prolonged (10 min) treatment increased the surface roughness slightly from ~1 Å RMS to about 2 Å RMS.

Charging of the wafer surface is also said to be the reason for higher bond energies for plasma-activated samples [5]. During plasma exposure the surface becomes charged due to implantation of the ions, ionization of the oxide and breakage of the bonds on the wafer surface, creating dangling bonds [14]. Charging of the oxide leads to electric fields which may affect the general chemical properties of the oxide and also the ion transport [15].

The intermediate water has to be removed before SiOH groups can react and form Si-O-Si bonds (Figure 2). This is assumed to take place by oxygen reacting with silicon while hydrogen dissolves into the oxide. If one of the oxides is thin, the water can reach the silicon and form silicon dioxide, even at low temperature. With thick oxides, the diffusion length for water to reach the silicon is longer, which is assumed to be the reason for weaker bond strength between SiO_2-SiO_2 surfaces than between Si-SiO_2 surfaces [**Publication A**]. It is suggested that the plasma increases the kinetics of water removal from the bonded interface [**Publication A**, 16, 13]. This is considered to take place due to a porous oxide layer formed by the plasma [**Publication A**, 13, 16]. The porosity of the layer is suggested by the increased oxide etch rate in SC-1 solution [**Publication A**, 13], by a higher etch rate during buried oxide etching with HF [**Publication D**] and by X-ray reflectivity at the bonded interface [13].

2.2.2 Ultra-high vacuum low-temperature hydrophobic bonding

Ultra-high vacuum (UHV) bonding has been reported as a method for making room-temperature hydrophobic bonding [9, 8]. First the wafer pair is bonded in the same way as in hydrophobic bonding (SC-1, HF dip, wafer contacting) but no annealing is done after wafer contacting. The bonding is done at this state only to protect the surfaces during transportation to the UHV chamber. After the wafers are placed in the UHV chamber and the base pressure is reached (10^{-10} mbar), the wafers are separated. By using an elevated temperature of 450°C the hydrogen termination is removed and the surface contains only reactive dangling bonds. The wafers are cooled to room temperature and bonded in the UHV

atmosphere. The measured bonding energy is close to the bond strength of the bulk silicon [8].

2.3 Bonding of chemical vapour deposited (CVD) oxides

Usually in SOI structures the buried oxide is thermally grown prior to bonding. Typically, deposition temperatures of CVD oxides are lower (150°C–500°C) than thermal oxidation temperatures (>800°C). Therefore, the CVD oxide layers can be grown on surfaces that contain temperature sensitive devices. Also, the growth rate is faster and the CVD process is not self-limiting like thermal oxidation (thickest thermal oxides < 3 μm). CVD SiO_2 can also be grown on non-silicon materials and therefore used as an intermediate bonding layer for heterogeneous integration. However, the CVD oxides also have some drawbacks compared to thermally grown oxide. The thickness uniformity is inferior and the as-deposited oxide surface is usually too rough for direct bonding. Electrical and physical properties are also inferior to thermal oxides.

Possible applications for bonding of CVD oxides are SOI wafers with thick buried oxides, bonding of pre-processed wafers (for e.g. encapsulation purposes), and bonding of non-silicon materials.

To study the suitability of CVD oxides for direct bonding, high and low temperature bonding tests were performed with plasma-enhanced chemical vapour deposited (PECVD) and low-pressure chemical vapour deposited (LPCVD) silicon dioxide layers. The bonding processes were carried out in vacuum. In the low temperature bonding process the wafer surfaces were activated with 30s oxygen plasma treatment followed with short SC-1 dip before bringing the surfaces into contact [**Publication A**]. The deposition temperatures were 425°C for LPCVD oxide and 300°C for PECVD oxide. For comparison, some wafers with thermally grown wet oxide were also bonded.

The CVD oxide surface roughness was first measured with AFM. The as-deposited PECVD oxide had a surface roughness of ~1 nm RMS and the as-deposited LPCVD oxide a surface roughness of ~3 nm RMS (Figure 5). From the SAM image (Figure 7a) of as-grown PECVD oxide bonded to the silicon wafer pair, it can be seen that the surface roughness is too high for direct

bonding. The as-deposited LPCVD oxide did not bond at all. Therefore, the wafers with CVD oxide went through a short oxide polishing step on the chemical-mechanical polishing (CMP) tool. After polishing, the measured surface roughness was below 2 Å RMS (Figure 6), enabling void-free bonding (Figure 7b).

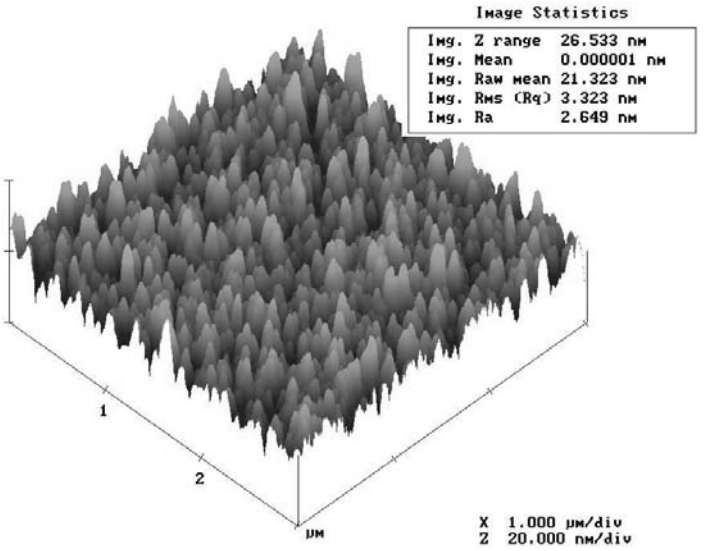

Figure 5. AFM image of as-deposited LPCVD oxide.

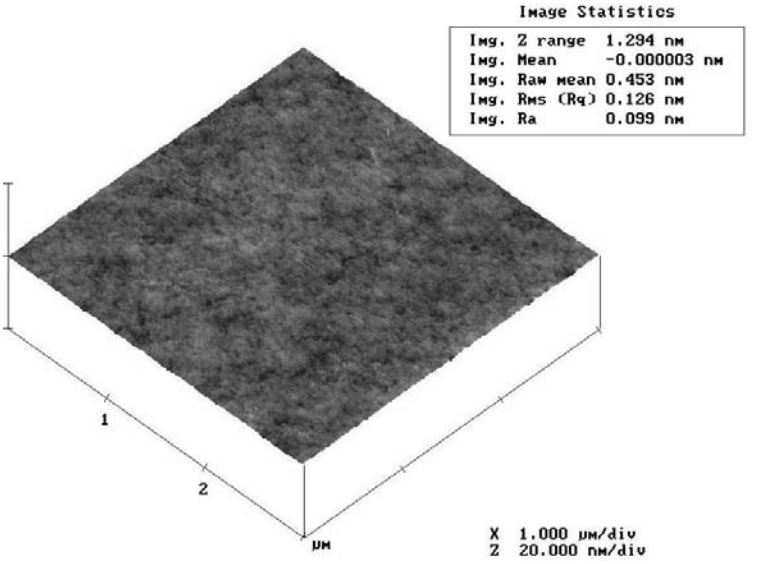

Figure 6. AFM image of polished LPCVD oxide surface.

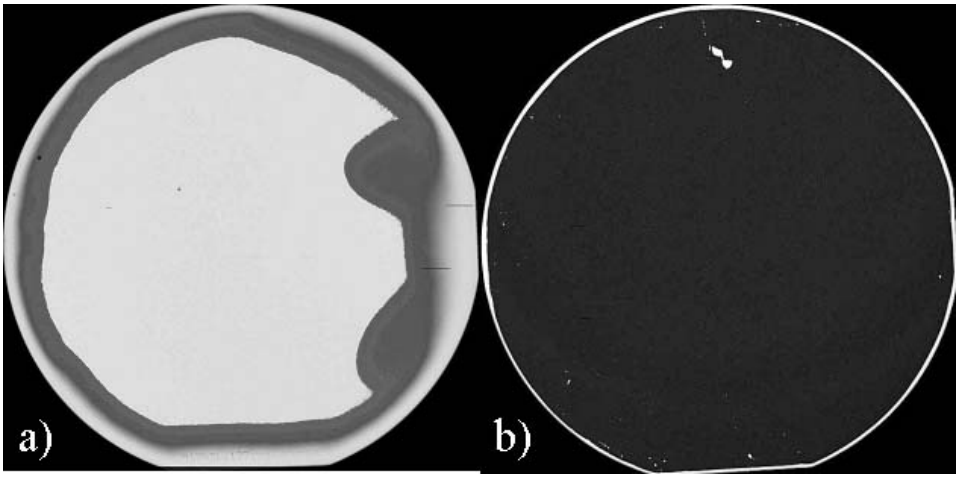

Figure 7. SAM images of a) as-deposited PECVD oxide bonded to Si wafer pair b) CMPd PECVD oxide bonded to Si wafer pair.

During bond annealing it was found that impurity outgassing takes place as the annealing temperature exceeds the deposition temperature. For example, PECVD oxide deposited at 300°C and bonded to the silicon wafer looks almost void-free in SAM after bond annealing has been carried out at 200°C (Figure 7b). When the same wafer is further annealed at 400°C, voids start to appear

(Figure 8a) and after annealing at 600°C the wafers are almost completely debonded (Figure 8b). Similar results were found with LPCVD oxide layers. When using an annealing step (2h, 1000°C) prior to bonding to outgas the impurities, no voids appear during bond annealing at temperatures between 100°C and 1100°C (Figure 9).

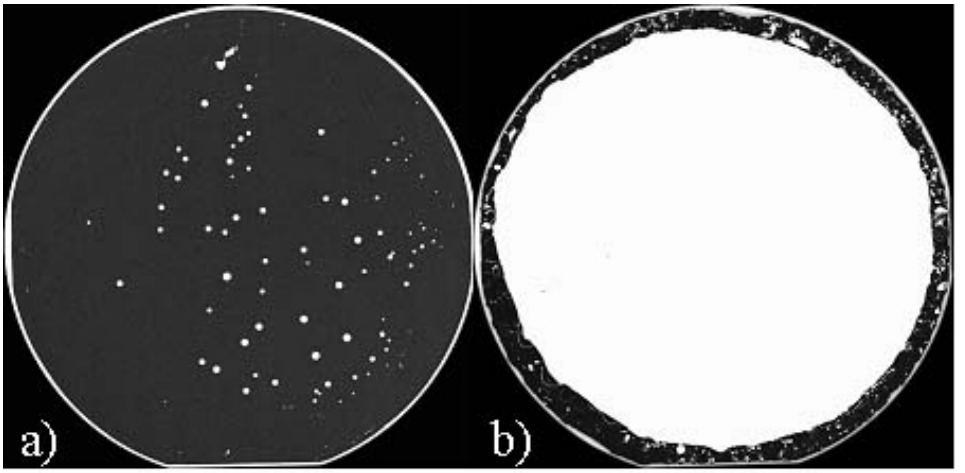

Figure 8. SAM images of Si-PECVD oxide wafer pair after annealing at a) 400°C b) 600°C for 2 h.

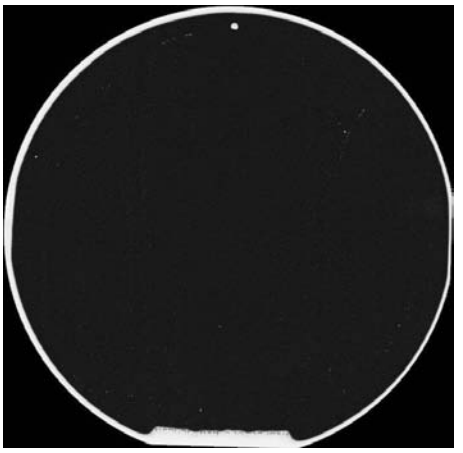

Figure 9. SAM image of Si-PECVD oxide wafer pair after annealing at 1100°C for 2h. PECVD oxide was pre-annealed before bonding at 1000°C for 2h.

Bond strength measurements were also carried out using the crack-opening method. Surface energies for different oxide-silicon wafer pairs are shown for non-activated samples in Figure 10. The CVD oxides were annealed at 1000°C prior to bonding to avoid impurity outgassing and debonding at high bond annealing temperatures. The figure shows that the strongest bonds are obtained for PECVD oxide/Si wafer pairs. It is possible that the PECVD oxide layer is more porous than LPCVD and thermal oxides. Porosity of the oxide makes it easier for bonding reaction products to exit the bonded interface. Ellipsometric film composition measurements also showed that the PECVD oxide contains excess silicon. This may also be the reason for stronger bonds, reducing the diffusion distance for the interfacial water to find silicon to react with.

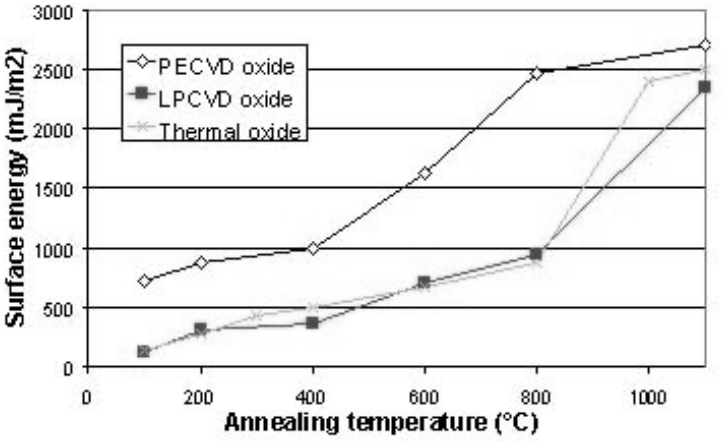

Figure 10. Bond strength as a function of annealing temperature for different Si-oxide wafer pairs bonded without plasma activation.

Figure 11 shows the surface energies for oxygen plasma activated samples. Oxygen plasma activation enables strong bonding already at a low temperature [**Publication A**]. All wafer pairs reached a surface energy of >2000 mJ/m^2 at 200°C, independent of the used oxide.

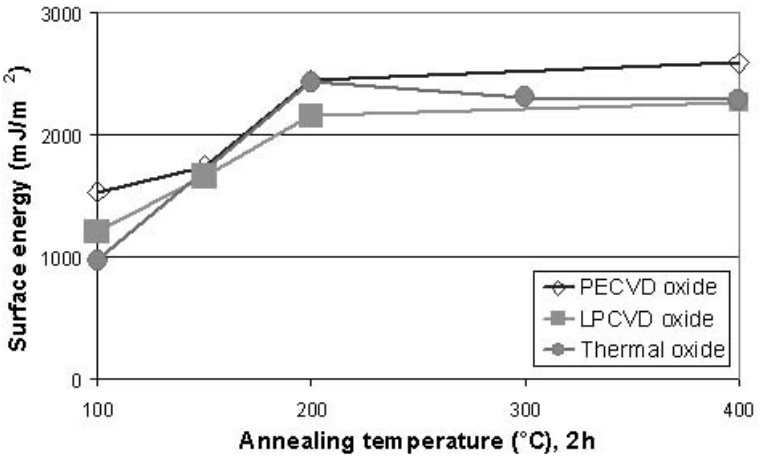

Figure 11. Measured bond strengths for plasma activated and bonded samples as a function of annealing temperature. Annealing time 2h.

2.4 Bonding of chemical vapour deposited silicon

Chemical vapour deposited polysilicon is sometimes used in MEMS applications. If polysilicon is used as the surface layer on the silicon wafer, the encapsulation is typically carried out by anodic bonding, which is not as sensitive to surface roughness as direct bonding. However, in some applications, it would be desirable to use direct bonding of polysilicon.

The first experiments were done with amorphous-like LPCVD silicon. In the as-deposited state on the oxide surface, the amorphous silicon had a surface roughness of 3–12 Å RMS. This surface roughness is not good enough for bonding, but in the amorphous state the silicon polishing with CMP was easy and required only removal of ~50 nm of silicon to achieve a surface roughness of ~1 Å RMS. The bonding was carried out in a vacuum and subsequent annealing was 2h at 1100°C, which not only strengthens the bond but also crystallizes the amorphous silicon into polycrystalline form. Measured bond strengths were high and no crystallization originating voids could be detected with SAM. The problem is the low deposition rate of amorphous films (~4 nm/min).

Tests have also been carried out on polishing and bonding of atmospheric pressure chemical vapour deposited (APCVD) and low-pressure chemical

vapour deposited (LPCVD) polysilicon films. With CVD polysilicon films, the problem is high as-deposited roughness of the films, which may be up to 10% of the final thickness. This means that during the polishing process the removal has to be much higher than with amorphous silicon. Another problem is that the chemistry of CMP attacks grain boundaries more than other areas, also causing problems in the polishing process. The advantage of growing in the polysilicon state is the increased growth rate compared to amorphous state deposition (40 nm/min with LPCVD, 4 μm/min with APCVD). The polishing process is carried out in two steps: the first step planarizes the surface (surface roughness ~12 Å RMS) and the second step smoothens the surface to the level required for bonding (~3 Å RMS). After polishing, the polysilicon surface was successfully bonded to the oxidized silicon wafer. [17]

2.5 Anodic bonding

Anodic bonding is a common method used in MEMS technology for device packaging. It was first introduced by Wallis and Pommerantz in 1969, after Pommerantz found that by applying an electric field a bond between metal foil and glass could be achieved at lower temperature than with conventional thermal bonding [18]. In anodic bonding, glass wafers can be joined to silicon wafers at low or moderate temperatures (300–450°C) and by applying a high DC voltage to the wafer pair (500–1000V) [19]. The most common glasses used for anodic bonding are Pyrex 7740 and Schott 8330, which are sodium borosilicate glasses having a coefficient of thermal expansion (CTE) close to the CTE of silicon. Sodium ions are needed for anodic bonding to take place, and matched CTEs help to maintain low stress on the bonded stack.

In anodic bonding the glass wafer is brought into contact with the silicon wafer and an external electrostatic field is applied at elevated temperature. Mobile sodium ions move towards the electrode, leaving a negatively-charged region into glass wafer, and electrostatic forces pull the silicon and glass tightly together. Next an electrochemical reaction takes place and covalent bonds are formed between the glass and silicon. Anodic bonding is less sensitive to surface roughness than direct bonding, but it requires that one of the wafers is alkali glass. It also requires high voltage and moderate temperatures.

2.6 Adhesive and polymer bonding

Adhesive bonding, as the name suggests, means that an intermediate adhesive layer is used to form bonding between two different materials. Adhesive bonding requires only low temperature annealing, if any. The bonding process is also cheap and requirements for surface smoothness are low. The disadvantages of these materials are long-term instability, a limited temperature range for their use, and the fact that they are not hermetic. However, the adhesive bonding is commonly used in applications where hermeticity is not needed. In some cases the bond hermeticity is obtained afterwards by using an additional metallization step [20]. Typical adhesives are different photoresists, polyimides and benzocyclobutane (BCB). [21, 22, 23]

2.7 Metallic bonding

Metallic bonding uses an intermediate metal layer between the wafers. It includes thermocompression, solder and eutectic bonding. In thermocompression bonding, two metallic surfaces are joined using high pressure and intermediate or low temperatures. For example, gold-gold thermocompression bonding is used by Avago Technologies to seal their film bulk acoustic resonator (FBAR) devices [24]. Bonding is formed by pressing together two wafers with gold pads at high pressure (~80 Mpa) at elevated temperature (~350°C).

In solder bonding, the solder balls are fabricated first by electroplating on one of the wafers, then the solder balls are brought into contact with contact pads on another wafer. The bonding is finished with low-temperature solder reflow. [25] The reflow process can also be carried out selectively using a laser [26]. Typical solders used in metallic bonding are SnPb and SnAg [20].

In eutectic bonding, typical metal systems are AuSi, AlGe and AuSn [20]. In the eutectic bonding carried out by Kim et al. [27], the cap wafer was covered with Cr-Au-Sn-Au layers and the handle wafer with Cr-Au layers. In the cap wafer the intermetallic reaction between Sn and Au had already occurred on the Sn-Au interface. As the bonding temperature was raised towards 250°C, the tin layer melted first and dissolved the thin $AuSn_4$ intermetallic layer. This molten Sn layer then came into contact with the thin Au layer on the handle wafer and

dissolved it. Upon cooling, the joint solidified and was expected to consist of a β-Sn matrix with $AuSn_4$ grains. [27]

Metallic bonding provides a hermetic seal at relatively low temperatures (200-400°C). Metallic bonding, however, has limitations regarding wafer topography and it is difficult to use it as a wafer-level bonding process.

2.8 Glass frit bonding

In glass frit bonding a glass paste layer is used as the bonding medium. It usually consists of finely ground (grain size less than 15 μm) lead or lead silicate glass and organic binder [28]. With inorganic additives the glass paste's CTE can be adjusted to match that of silicon. The glass paste is first deposited on the handle or the cap wafer, usually by screen-printing. After deposition the organic solvent is removed and the glass is sintered by drying and heating the sample. Then the cap wafer is placed on top of the handle wafer, the glass layer is melted at the process temperature, and the wafer pair is bonded under thermo-compression. The temperature needed is above the softening temperature of the glass used, usually still below 450°C. The advantages of the method are insensitivity to surface roughness, usability with most materials, and cheap price. The disadvantages are incompatibility with IC technology (due to Pb) and the requirement for a wide bonding rim (>200 μm).

3. Methods for evaluating bonding quality

The bonding quality is usually considered to consist of two parts: the bond strength and the amount of voids. In some applications these two quality factors are the only information needed, but in some applications it is also important to know e.g. the electrical properties of the interface and the etch rate of the buried oxide. This chapter looks at different bond quality measurements.

3.1 Methods to estimate the bondability of wafers

Especially with processed wafers, it is important to investigate the surface quality before bonding. This makes it possible to predict whether or not bonding is possible. The most important tools for this are profilometers to investigate the planarity of the wafer, and atomic force microscopy (AFM) for surface roughness measurements. Sometimes it is also important to use a particle detector to find process steps that may induce void-causing particles to the surface.

3.1.1 Atomic force microscopy (AFM)

The surface roughness of wafers is usually measured with an atomic force microscope (AFM) in tapping mode. The operating principle of the AFM is shown in Figure 12. In tapping mode, a silicon tip barely touches, or ”taps”, the surface. The system vibrates a cantilever near its resonant frequency at an amplitude of a few to tens of nanometers. Then it detects changes in the resonant frequency or vibration amplitude as the tip nears the sample surface. The changes in amplitude are measured with a laser beam, reflecting from the cantilever to a detector. The resonant frequency of the cantilever varies as the square root of its spring constant. In turn, the spring constant of the cantilever varies with the force gradient experienced by the cantilever. Finally, the force gradient changes with tip-to-sample separation. Therefore, changes in the resonant frequency of the cantilever can be used to measure sample topography. [29]

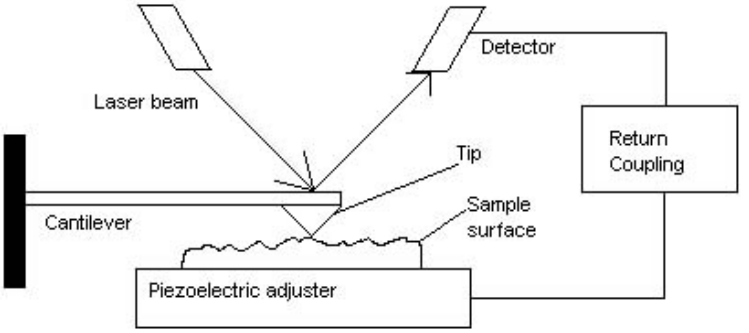

Figure 12. Operating principle of the atomic force microscope (AFM). A sharp silicon tip taps the surface and the amplitude of the oscillation is measured with a laser beam. Return coupling adjusts the height of the cantilever to keep the amplitude constant. [29]

3.1.2 Surface profilometry

Surface profilometry is of two types: contact and non-contact. The principle of contact profilometry is quite similar to AFM: a needle moves along the surface and its height is detected. The difference is that AFM usually scans areas of a few μm^2 and heights in the nanometre range whereas the profilometer's typical scan length is a few centimetres and the measured step heights are tens of micrometres.

Non-contact surface profilometry is based on optical interferometry. The interferometer splits a source beam of light into two different beams, one of which is reflected against the sample and another against a reference mirror. The two beams are then recombined and a CCD camera records the interference phenomena. Based on the interferogram the computer can calculate the distance between the sample and the objective. [30] The optical profilometry image of a cavity in a Si wafer is shown in Figure 13.

Figure 13. Optical profilometry image of an etched cavity on a Si wafer.

3.1.3 Particle detection

Particle detection on the wafer surface is usually done with methods based on light scattering. The surface is scanned with a high-intensity light spot and the light is scattered by defects (particles, scratches etc.). The scattered light is collected by a photodetector and a map is formed of the scanned surface showing locations and sizes of particles and other defects on the wafer surface.

3.2 Bond strength measurements

An important parameter that should be known in bonded wafer pairs is the amount of adhesion or the bond strength. This is because the bond strength may have a critical influence on the process steps (mechanical thinning, patterning, etching etc.) that the substrate undergoes.

3.2.1 The crack opening method

The most common method for measuring bond strength is the crack opening method [31]. A blade is inserted between two wafers, creating a crack between them. The crack length is then measured and in the case of identical wafers the bond strength can be calculated from

$$\gamma = \frac{3Ed^3 t_b^{\,2}}{32L^4} \tag{4}$$

where E is Young's modulus, t_b is the thickness of the blade, d is the thickness of the wafers and L is the length of the crack.

However, this method has its limitations. It is not suitable for measuring fragile wafers, because they tend to break during measurement. To insert the blade into the bonded surface, the bonded wafers have to be rounded at the edges. This is usually the case with two bonded silicon wafers, but it limits bond strength measurements to the areas near the edge of the wafer. It is also an inaccurate measurement, because the crack length in Equation 4 is to the power of 4 and the crack length also depends on the surrounding atmosphere. Some changes in crack length can also take place due to the force and speed with which the blade is inserted. To make the method more accurate, an automated blade insertion tool is suggested together with an environmental protective chamber [32]. Despite these drawbacks, it is the most popular method because it is cheap, simple and does not require wafer patterning.

3.2.2 Pulling test (or tensile test)

In the pulling test, as the name suggests, the bonded samples are pulled apart and the required force is measured. This method was first used for bonded silicon wafers by Abe et al. [33]. Both sides of the wafer pair are glued to the pulling rods in the test apparatus and force is applied. The force is increased until the wafers are separated. The operating principle is depicted in Figure 14.

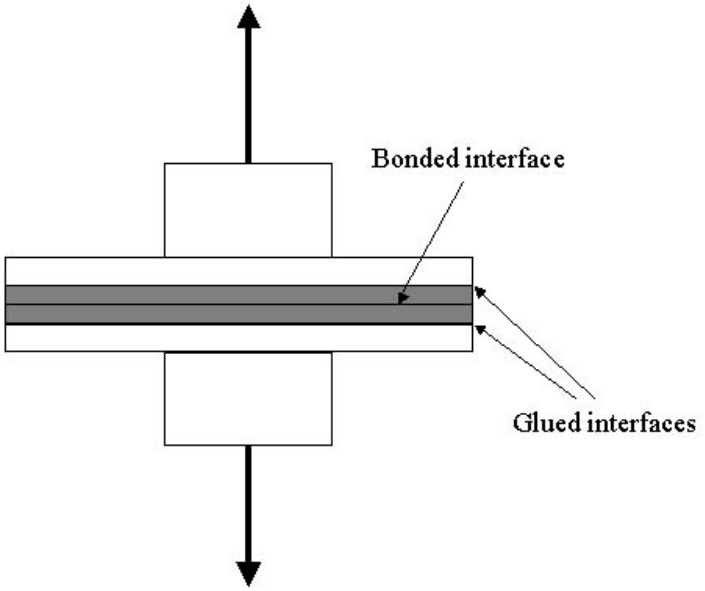

Figure 14. Set-up for the pulling test.

The pulling test is a useful method for measuring bond strength from small samples and it can be used to form bond strength maps for the wafers. The drawbacks are a more complex apparatus than in the crack opening method, and a problem with strong bonds or fragile samples in that the fracture does not occur at the bonded interface. The pulling rods should be placed into the centre of the sample and the pull axis should be perpendicular to the sample surface. Even small misalignment in the set-up may have a drastic influence on the results. Gluing is time consuming and may be the part that breaks first in the pulling test [32].

3.2.3 Blister test

The blister test has also been suggested as a method for measuring bond strength. In this test, one of the bonded wafers contains a hole and the hydrostatic oil pressure is applied through the hole until debonding takes place (Figure 15). The pressure required for debonding to occur is measured. With this pressure, the surface energy of the bonded interface can be determined from Equation 5. [2]

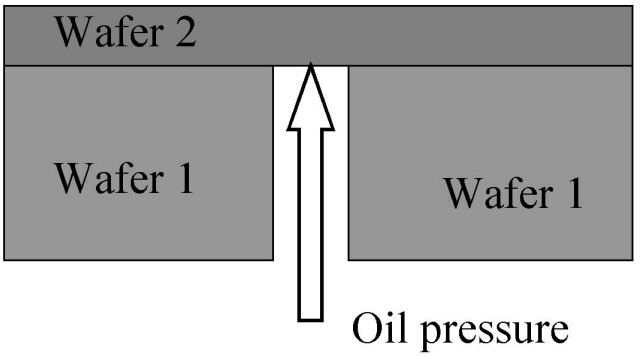

Figure 15. Set-up for the blistering test. Oil pressure on the hole is increased until debonding occurs.

$$\gamma = \frac{0.088 P_f^2 a^2}{E t_w^3} \tag{5}$$

where a is the hole radius, E is Young's modulus for the top wafer, P_f is the pressure required for debonding and t_w is the top wafer's thickness.

3.2.4 HF etching test

This bond strength measurement method is based on buried silicon dioxide etching in hydrofluoric acid (HF). It is described in more detail in **Publication D**. It has been found that the HF etch rate is dependent on the bonded interface quality. In this method the sample is dipped into 50% hydrofluoric acid for 10 minutes and the etched distance is measured with scanning electron microscopy from cross-sectional samples. A cross-sectional SEM image of strong bonding is shown in Figure 16. The etch rate at the bonded interface is close to the etch rate at the thermal oxide growth interface, which seen from the vertical oxide wall. At a weak interface (Figure 17), the profile of the oxide wall is less vertical due to a faster etch rate at the bonded interface.

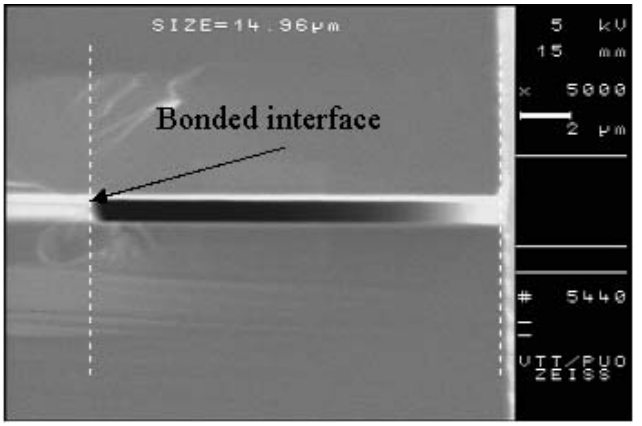

Figure 16. SEM image of buried oxide etched for 10 min in 50% HF. The etch rate of ~1.5 µm/min, and an equal etch rate on the bonded interface and the oxide growth interface indicate strong bonding.

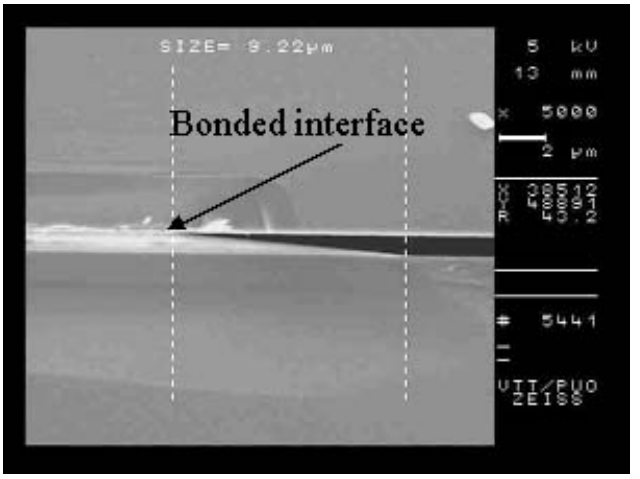

Figure 17. SEM image of buried oxide etched for 10 min in 50% HF. The higher etch rate at the bonded interface and the long total etched distance (~200 µm, not seen in the picture) indicate weak bonding.

For high temperature bonding of hydrophilic silicon wafers, the relation between bond strength and etch rate is logarithmic, as seen in the results plotted in Figure 18 [**Publication D**]. With plasma-activated samples the correlation is not as easy, because plasma creates a porous oxide layer. This porous layer has a higher etch rate than normal thermally-grown silicon dioxide, which makes the correlation more difficult.

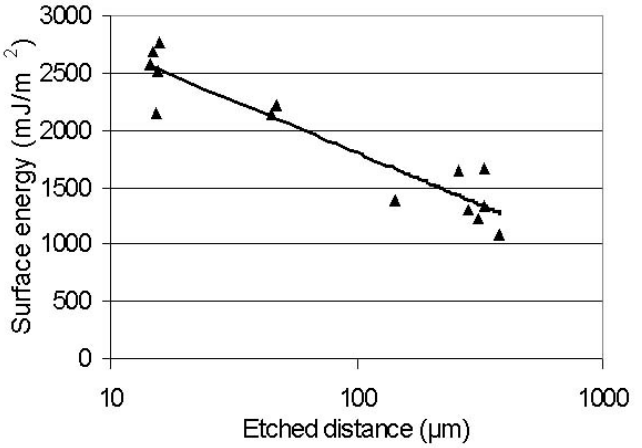

Figure 18. Relationship between etched distance of buried oxide during 10 min 50% HF etching and measured surface energy for high temperature bonded samples.

The etching method is a good method for certain samples that cannot be measured with the crack-opening method. Such samples are fragile, like quartz and glass wafers, ready-made SOI and diced samples.

The HF etching method also gives a good idea of the bond strength across the whole wafer area. The SOI layer is first patterned with standard lithography, and holes through the SOI layer are formed with ICP etching. Next the SOI wafer is dipped in 50% HF for 10 minutes, rinsed in DI water and dried. With relatively thin SOI layers (< 15 µm) and not highly boron-doped samples, the etched distance can be measured with an optical microscope attached to a near infrared (NIR) or infrared (IR) camera. By having "through-SOI" holes over the whole wafer area, the etched distance is easily measured from different locations, and variations are easily detected. A near-IR microscopic image (20x magnification) of the HF etched oxide front is shown in Figure 19.

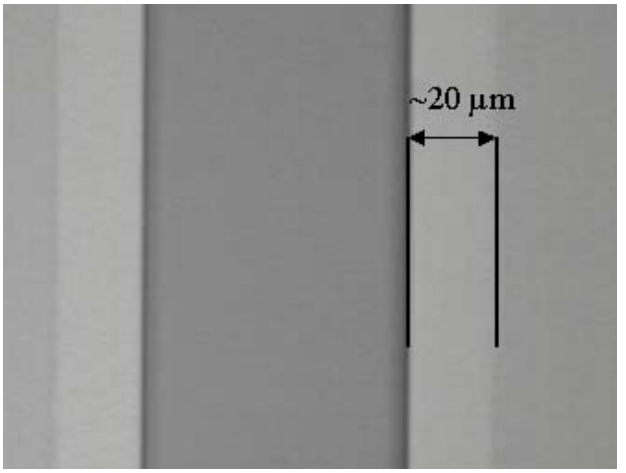

Figure 19. Near-IR image of buried oxide-etched sample. The darker area in the middle is where the SOI layer has been removed with ICP etching; the lightest areas represent the areas on which the BOX has been etched.

3.2.5 Chevron test

The chevron test is nowadays also a popular method for measuring the bond strength. It was first introduced by Rayleigh as early as 1936. It was first used for direct bonded wafers by Hoshi and Ogino in 1989 [32]. In recent years, Dr. Bagdahn's group at the Fraunhofer Institute in Halle, Germany, has been active in further developing the method, which they call the micro-chevron or MC test [34, 35].

In this method one of the wafers has chevron-shaped patterns on the surface before bonding, and it is bonded to an unpatterned wafer (Figure 20a). Pulling studs are then glued to the sample and a pulling force normal to the bond is introduced (Figure 20b). The force is slowly increased and a crack is formed starting from the tip of the chevron. While the crack propagates, the width of the crack increases according to the shape of the chevron. As the crack reaches its critical length, the crack's growth becomes unstable and instantly causes a fracture in the sample. The crack length depends only on the loading conditions and the specimen geometry, therefore the critical load for fracture to take place is the only thing needed to calculate the toughness of the bonded structure. [32]

This method is considered to be the most accurate measurement method for determining the bond strength. The measurement of maximum force is more accurate than measuring the crack length. The method is also suitable for measuring high bond strengths, because the fracture starts at the bonded interface at the chevron tip due to a high stress concentration [32]. Usually small chevron shapes are located all over the bonded area, so with the chevron test, bond strength maps can also be determined. Small chevrons can also be used on wafers containing actual devices to confirm the quality of the bonding. The only problems are the necessity for wafer patterning before bonding and gluing during loading, both of which are time-consuming.

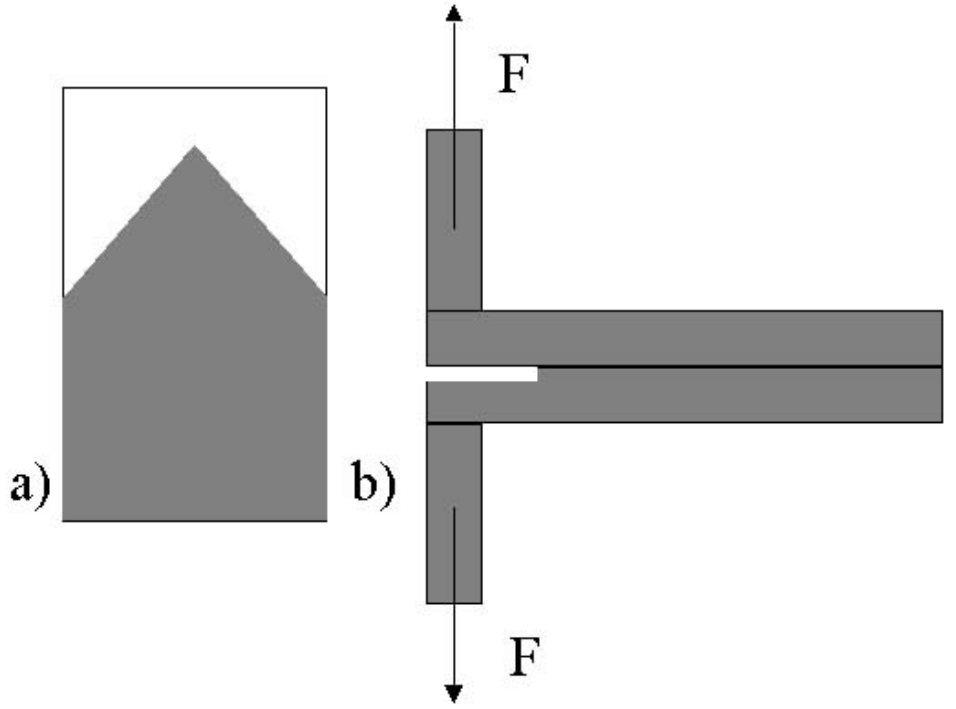

Figure 20. Set-up for micro-chevron test. a) Handle wafer with chevron shape bonded to a cap wafer b) Cross-section of the same sample with two pulling studs connected to the end with an unbonded area.

3.3 Void detection

Another important quality factor of the bonded interface is the amount of discontinuations of the bonded interface, so called “voids”. These voids may be caused by particles, chemical contaminants, poor surface quality or trapped gas. There are different methods for void detection. Optical inspection can be used in cases where at least one of the wafers is transparent to light (quartz, glass, sapphire). In the case of silicon wafers, typically the first inspection is done with an infrared (IR) camera before annealing. A final, more detailed inspection is usually done after final annealing. For this, the most widely used method is scanning acoustic microscopy.

3.3.1 Optical inspection

For instant investigation of the bonding quality, optical transmission is the most popular method. Areas that are not in contact form Newton’s rings due to the interference of light reflected on internal surfaces. The shape of the rings shows the shape of the delamination, and light and dark rings enable determination of the distance between unbonded surfaces [36].

If at least one of the bonded wafers is transparent (e.g. glass, quartz, sapphire), voids can be observed with the naked eye. For cases with two silicon wafers, IR light and an IR camera are required. Heavily doped silicon, however, is not transparent to IR light and therefore IR transmission is not suitable for wafer pairs with at least one highly doped counterpart. Figure 21 shows an IR image of a bonded 4’’ silicon wafer pair having one large and a couple of smaller voids.

The method is popular because it is fast and non-destructive. It can be used instantly after wafer contacting, so no annealing is needed before inspection. However, it is unable to detect all voids. To detect a void with IR, the surfaces must be at least one fourth of the wavelength apart and the lateral resolution is typically limited to about 1 mm. [37] Nowadays there are commercially available scanning IR tools that use light scattering over inhomogeneities. For example, Phoseon Technology [38] promises a resolution of ~5 µm.

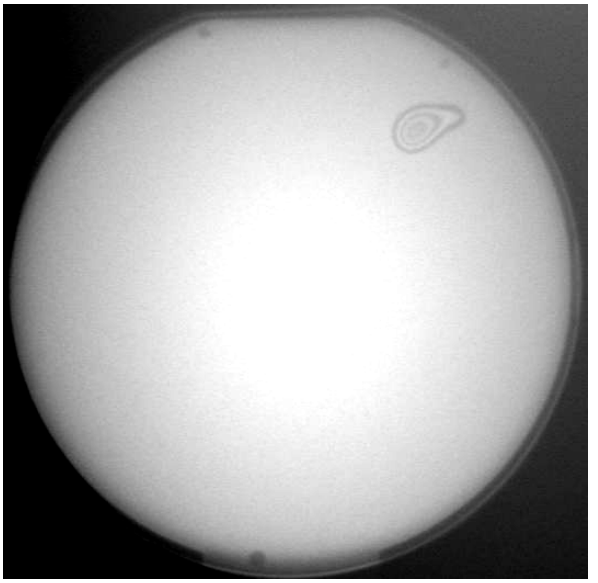

Figure 21. IR image of bonded 4'' wafer pair. At top right is a large void surrounded by Newton's rings.

3.3.2 Scanning acoustic microscopy (SAM)

Scanning acoustic microscopy is also used for void detection. It works like a sonar, sending an acoustic signal and measuring the time it takes to reflect back to the detector. The intermediate material between the sample and the emitter-receiver is water. The acoustic signal reflects back if the media it travels through changes. Interpreting the signal in the case of two bonded wafers is fairly easy. The microscope shows a signal graph in which the x-axis represents the time of delay from the transducer to the receiver, and the y-axis represents the strength of the reflection. From this graph it is easy to distinguish the reflections coming from the front and back surface of the bonded wafer pair. If there is also a reflection originating between the front and back surface reflections, it is usually caused by an interfacial void (in some cases e.g. thick buried oxide causes reflection, but it is typically weaker than the signal coming from a void).

In wafer bonding the SAM is typically used in C-mode. In C-mode, the SAM-image is formed from the reflections coming from a depth set by the user. The theoretical maximum resolution of SAM is 0.5 μm [39], but this requires high

frequency and a really thin sample. The typical scan resolution for full-wafer scans is ~100 µm to limit the scan time to a few minutes. The SAM image of patterned 30 nm oxide bonded to a blank silicon wafer is shown in Figure 22. The white areas represent reflection and therefore also unbonded areas. For comparison, an IR image of the same wafer pair is presented in Figure 23. In the IR image only the largest, particle-induced voids can be detected. The drawback of acoustic microscopy compared to IR inspection is the necessity to do bond annealing before measurement in order to avoid debonding of the wafers when exposed to water. Another drawback is throughput; IR inspection takes only a couple of seconds, whereas SAM C-scan inspection of a 4'' wafer takes a couple of minutes.

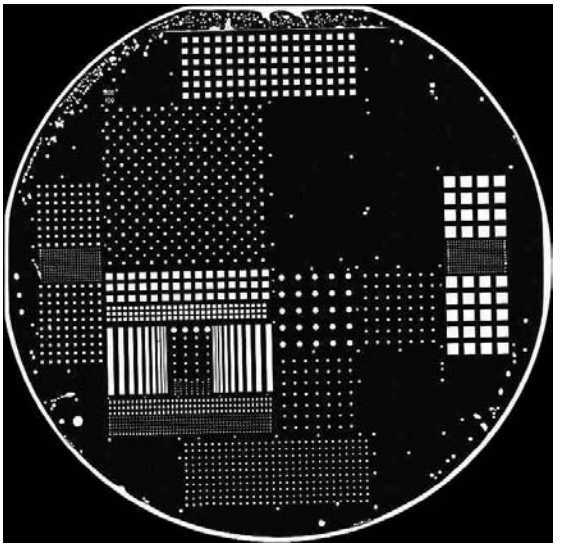

Figure 22. SAM image of a bonded wafer pair showing patterns on a handle wafer's 30 nm thick oxide layer.

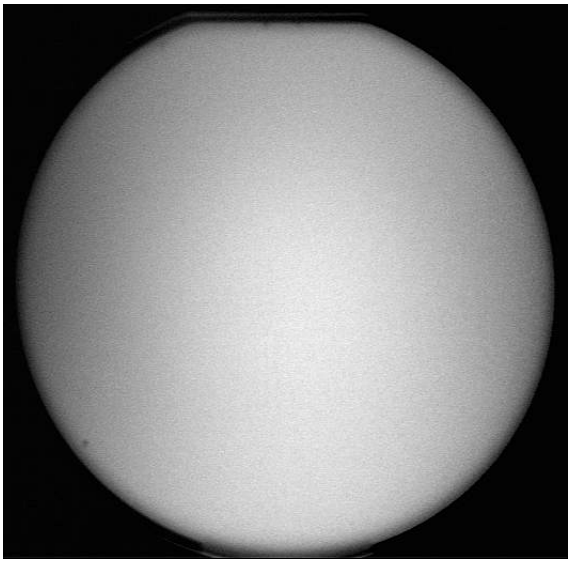

Figure 23. IR image of the same wafer as in Figure 22. 30 nm high patterns are too small to be detected by IR transmission.

4. Applications of Wafer Bonding

Wafer bonding is becoming an increasingly common method in IC- and MEMS manufacturing. It is no longer limited to substrate manufacturing, but is also used as a method to fabricate 3D MEMS devices [40], 3D integration of layers containing different devices [41], and device encapsulation [42]. However, the most common application for wafer bonding is still the fabrication of silicon-on-insulator (SOI) substrates. Direct bonding is also used for bonding of more exotic materials than silicon, such as GaAs, InP, glass, quartz, sapphire etc. Basically any material with a smooth enough surface (< 1 nm RMS) can be directly bonded.

4.1 Silicon-on-Insulator (SOI)

Silicon-on-insulator wafers consist of a silicon handle wafer, an oxide layer and a silicon device layer (SOI layer) (Figure 24). SOI wafers are basically divided into two categories: thin film SOI (device layer thickness a few nm – 2 μm) and thick film SOI (5 μm – 200 μm). Thin film SOI is mainly used in IC fabrication and thick film SOI is more for MEMS purposes. The thinning methods for these two thickness areas are quite different. However, the bonding process is quite similar.

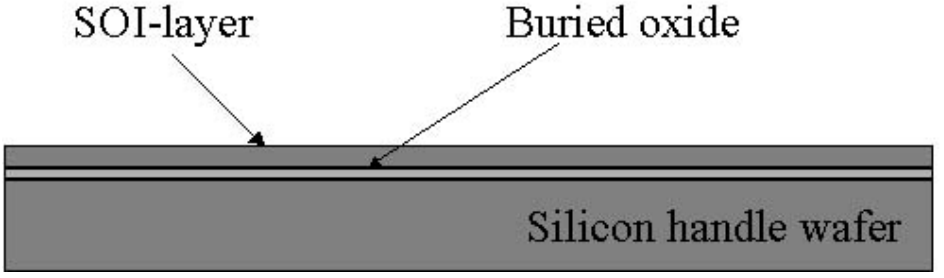

Figure 24. Typical SOI wafer. The buried oxide thickness is usually 50 nm – 3 μm and the SOI layer thickness 50 nm – 150 μm.

4.1.1 Thin film SOI

Thin SOI wafers are mostly made using ion implantation. An old method was to implant oxygen to a certain depth into the silicon wafer and then induce an oxidation process inside the silicon wafer by annealing. The process was called separation by implanted oxygen (SIMOX). However, this process had problems with implantation-induced dislocations [2] and it was also very expensive. Because of these problems, SIMOX has been commonly replaced with wafer bonding-based fabrication methods.

The most common method for thin SOI fabrication is Smart Cut™. In this method the device wafer is implanted with hydrogen before bonding. Bruel found that implanted hydrogen forms blisters (Figure 25) during annealing. [43]

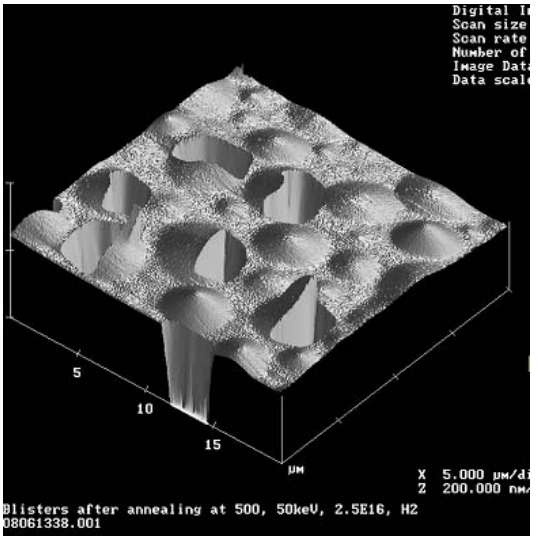

Figure 25. Exploded blisters after annealing hydrogen implanted silicon at 500°C (Picture courtesy of Kimmo Henttinen, VTT).

If another wafer is bonded to the implanted wafer, the blisters cannot "explode" but form lateral "platelets". These platelets grow in size with increasing annealing temperature. The crack is formed at the far end of the implantation damage [44, 45]. The splitting temperature is influenced by the hydrogen concentration and it can be reduced by implanting a dose of boron [**Publication F,** 46]. Boron is assumed to trap hydrogen, increasing local hydrogen

concentration and thus lowering the temperature required for blister or platelet formation [47].

It is also possible to use mechanical instead of thermal splitting. In this case the bond strength at the bonded interface should be higher than the strength in the implanted region. Figure 26 shows the development of surface energies for a plasma-activated and bonded interface and for an implanted region as a function of the annealing temperature [**Publication F**].

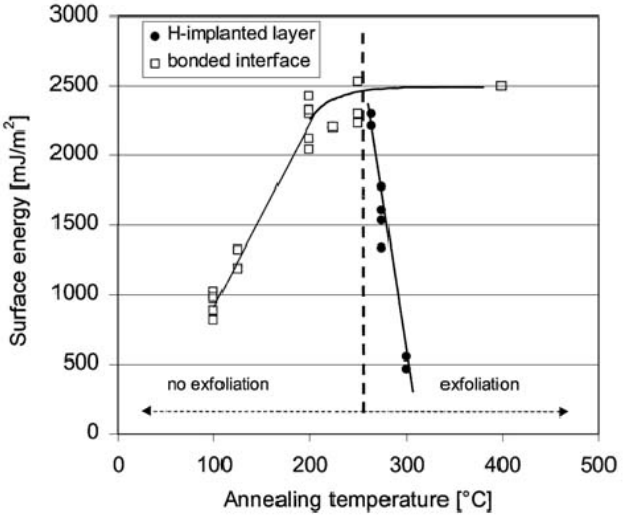

Figure 26. Measured surface energies for the bonded interface and for the H-implanted region as a function of annealing temperature. Annealing time was 2 h.

Mechanical splitting is induced by inserting a razor blade between the wafers. The wafer pair is separated from the weaker interface, so achieving high bonding energies already at low temperatures is necessary for demanding applications. One such case is silicon-on-quartz, where the annealing temperature is limited because of a great difference in the coefficients of thermal expansion (CTE) [48]. In this example, the use of boron had to be avoided, because the final application was in thin film transistors, and boron implantation changes the electrical properties of the silicon layer. Therefore, a process was applied that involves high-dose hydrogen implantation, plasma activation-based low temperature bonding and mechanical exfoliation. [48]

After splitting, the surface roughness is 5–10 nm RMS and therefore the surface should be polished before device fabrication. The device wafer can be polished and recycled over and over in the process. If the layer needs to be thinned down further, this can be done using thermal oxidation and oxide etching without loosing thickness uniformity. The process is depicted in Figure 27. The Smart Cut™ process patent is owned by SOITEC. They fabricate thin film SOI with various thicknesses (50 nm – 100 µm) on wafer sizes up to 300 mm.

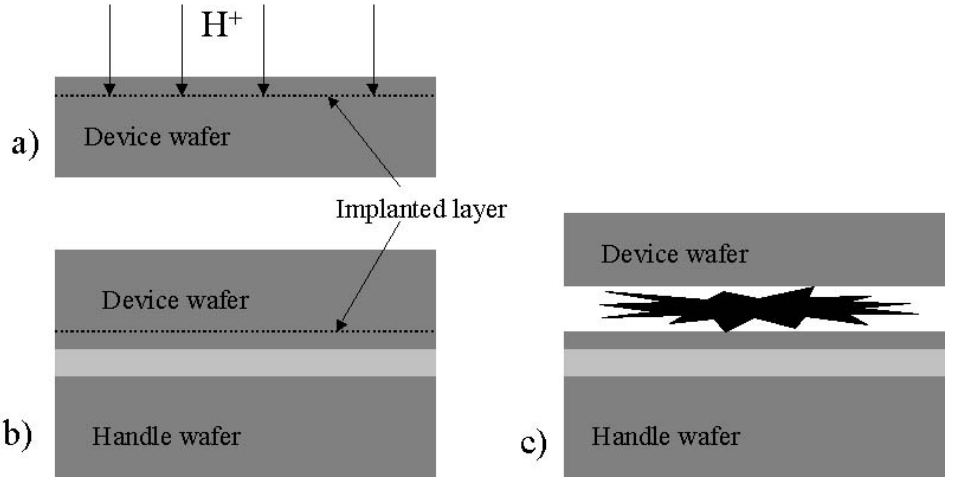

Figure 27. Smart Cut™-process: a) The device wafer is implanted with hydrogen b) The device wafer is bonded to an oxidized handle wafer, c) Thermal annealing strengthens the bond and induces splitting in the implanted region.

Canon have their own method for fabricating thin film SOI. They grow a porous layer of silicon on the device wafer using a special process, on top of which it is possible to grow epitaxially single crystalline silicon. Once the epitaxial layer is polished, it is bonded to the handle wafer and the layer can be released from the weakest region, which in this case is the porous layer. Their mechanical release process is based on a water jet. [49]

Thin SOI wafers provide many advantages for IC fabrication. The switching speed of circuits fabricated on SOI is increased by 20–50% compared to circuits fabricated on a bulk Si wafer. The required operation voltage is lower in ICs on SOI than in ICs on a bulk silicon wafer, which decreases power consumption and chip heating. The circuit packaging density is also increased due to simplification of the lateral and vertical isolation structures.

4.1.2 Thick film SOI

Thick film SOI is replacing conventional Si wafers as the start substrate for microelectromechanical systems (MEMS). The advantage of SOI substrates is that the buried oxide layer can be used as sacrificial layer, and by etching it different types of diaphragms, films and beams can be released.

Thick film SOI wafers are made by bonding, grinding and polishing. Before grinding, the edges of the bonded stack are usually ground to avoid edge chipping. The reason for edge chipping is the unbonded area near the edge due to the edge roundness of the bonded wafers. Grinding is usually done in two steps; the first is coarse grinding to remove most of the material, the second is fine grinding (10–25 µm removal) to reduce the depth of the grind lines and reduce the sub-surface damage.

A CMP or etching step is used to remove sub-surface damage. The damage layer causes stress to the SOI film and therefore, if not removed, may cause breakage of the MEMS device. CMP is also used to remove the grind lines and create a smooth surface. The CMP causes thickness variation and thus silicon removal with CMP should be minimized.

4.1.3 Intermediate SOI (device layer thickness 2–5 µm)

SOI wafers with thicknesses between 2 and 5 µm are difficult to find, because conventional thinning methods used in thick SOI fabrication cause large procentual thickness variation (0.5 µm TTV is 10% variation for 5 µm SOI layer, 25% for 2 µm SOI layer). Therefore, these layers with intermediate thicknesses are mainly made using either etching thick film SOI with etch stop layers or by growing epitaxially more silicon on thin film SOI.

4.1.4 Strained silicon-on-insulator (sSOI)

Carrier mobility can be improved by having the device layer silicon under tensile stress. [50]. This improves the performance of CMOS circuits fabricated on strained silicon. This improvement can be combined with the advantages of

SOI (e.g. reduced junction capacitance) by fabricating strained silicon-on-insulator (sSOI) substrates.

The strain in silicon is typically introduced by epitaxially growing silicon on a material with a larger lattice constant, such as SiGe. sSOI is usually fabricated by first fabricating a SiGe-on-insulator (SGOI) substrate. Three different methods have been reported for SGOI fabrication: SIMOX, Ge-condensation and wafer bonding and thinning [51].

In SIMOX the buried oxide is fabricated by implanting oxygen ions into the substrate, and during subsequent high temperature annealing the implanted oxygen reacts with silicon and forms a buried SiO_2 layer. However, this method is only applicable with low Ge concentrations due to thermal instability of SiGe at elevated temperatures [51]. Since the strain-induced hole mobility is expected to continue to improve up to about 30% Ge concentrations, other approaches for SGOI preparation have been developed.

One method for fabricating SGOI substrates with a higher Ge concentration than obtained with SIMOX is the Ge condensation method. Here a low Ge concentration SiGe layer is grown on SOI. When SiGe is exposed to an oxidant, a mixed oxide of SiO_2 and GeO_2 is formed. At high temperatures, the GeO_2 formation is replaced by SiO_2 formation and the Ge concentration at the SiGe layer increases, as shown in Figure 28. The oxidation temperature must be kept below the melting point of SiGe alloy. [51]

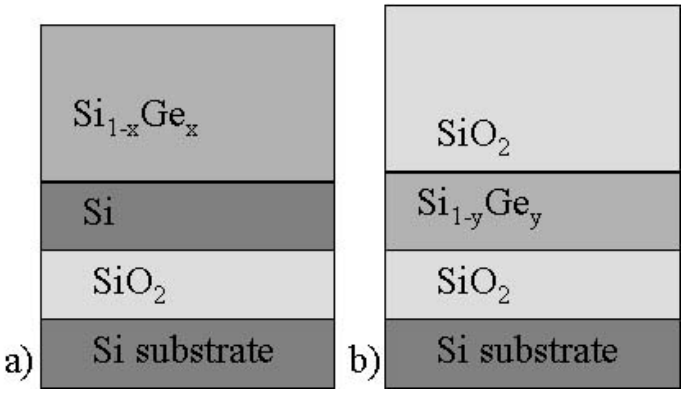

Figure 28. a) Low Ge content SiGe on SOI, x<0.1 b) At high temperature oxidation SiO_2 is formed and Ge diffuses into the underlying SiGe, increasing its Ge content, y>x [51].

A third approach to SGOI fabrication is to use wafer bonding combined with a thinning method. In this case the strain-relaxed SiGe layer is grown on a silicon wafer by ultra high vacuum chemical vapour deposition (UHVCVD). The SiGe epilayer is then polished and bonded to an oxidized silicon wafer. Thinning methods are similar to conventional SOI fabrication, including etch back (using SiGe-layer as an etch stop), grinding and polishing as well as ion-implantation based methods.

Once the SGOI substrate is ready, a thin silicon layer is grown on top of it. The silicon is strained due to a larger lattice constant of SiGe. One possible process flow for the fabrication of strained Si-on-SiGe-on-insulator with wafer bonding and ion-cut is depicted in Figure 29 [50].

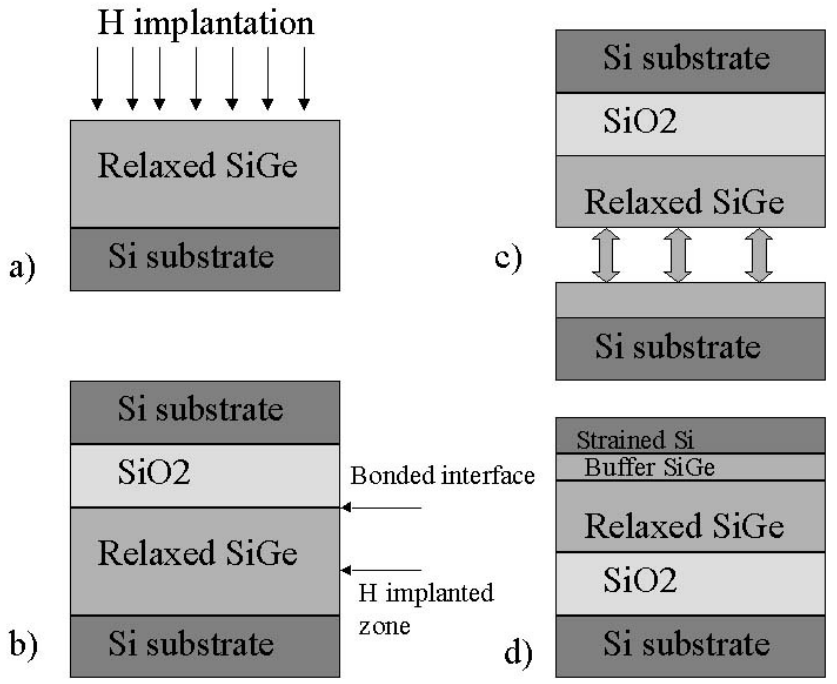

Figure 29. a)The SiGe-on-Si wafer is implanted with hydrogen b) The wafer is bonded to the oxidized Si wafer c) Thermal ion-cut enables SiGe layer transfer from the SiGe-on-Si wafer to the oxidized Si wafer, resulting in an SiGe-on-insulator structure d) Growth of thin Si layer on SGOI substrate. Si is strained due to a lattice mismatch between Si and SiGe. [50]

Having sSOI substrates with a buried SiGe layer, however, poses several challenges to further processing steps. The SiGe-strained Si stack is difficult to make below a thickness of 30 nm. Presence of SiGe layer alters the dopant diffusion and changes the contact metallurgy reactions. Ge may also diffuse into the sSOI layer. Therefore, it would be advantageous to have sSOI wafers without buried SiGe-layer.

Langdo et al. have fabricated SiGe-free sSOI substrates by wafer bonding and layer transfer [52]. They first fabricated a substrate containing a strained Si layer on SiGe-on-Si substrate (Figure 30a). They then implanted hydrogen through the strained Si layer (54 nm thick) into a $Si_{0.68}Ge_{0.32}$ layer to a depth of ~350 nm below the strained Si. Next the wafer was bonded to the oxidized silicon wafer and annealed to strengthen the bond and induce hydrogen splitting (Figure 30b).

The $Si_{0.68}Ge_{0.32}$ layer film was then removed by a combination of low temperature steam oxidation and dilute HF etching. The final result was SiGe-free strained silicon on the insulator structure (Figure 30c). [52]

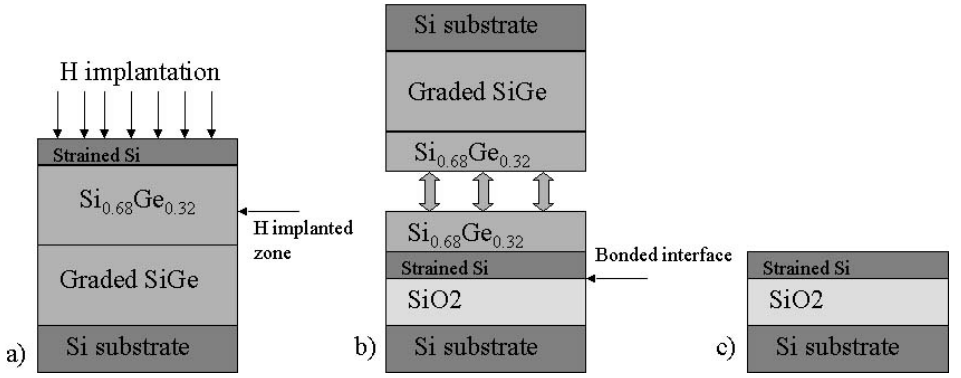

Figure 30. Fabrication process for SiGe-free strained Si substrates. a) The SiGe layer is hydrogen implanted through the strained Si layer b) Si on the SiGe-on-Si substrate is bonded to the oxidized silicon wafer and thermal ion-cut is used to transfer the strained silicon layer and part of the SiGe layer c) The SiGe layer is removed by steam oxidation and dilute HF etching. [52]

4.1.5 Cavity SOI

In order to allow greater freedom in MEMS designing, there is increasing interest in SOI wafers with buried structures (cavities, different support structures). A fabrication process for such wafers is presented in **Publication C**. Fabrication of the pre-patterned SOI wafers requires cavity fabrication on one or both of the wafers before bonding. During cavity fabrication, special care should be taken to keep the surfaces smooth and particle free. It should be emphasized that there are a wide range of different MEMS devices. Different MEMS devices place different demands on pre-patterned SOI wafers concerning cavity location (top, bottom or on both wafers), oxide location (top, bottom, both, on cavity), cavity shape and size, possible support structures (number, shape, size, locations), cavity atmosphere etc. Therefore, the fabrication process for pre-processed SOI also depends on the device. One approach to cavity-SOI fabrication is presented in Figure 31.

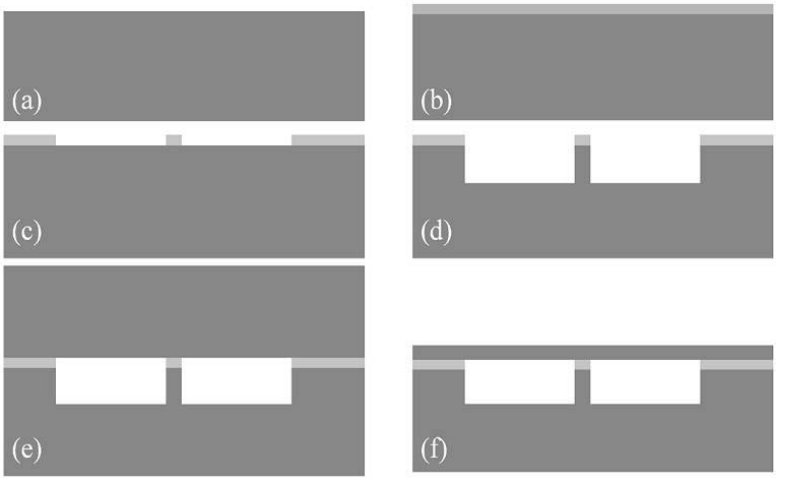

Figure 31. Fabrication process for cavity SOI a) Silicon handle wafer b) Thermal oxidation c) Patterning of the oxide d) Deep silicon etching e) Bonding of the cap wafer f) Thinning of the cap wafer.

After cavity fabrication and possible cleaning steps, the cap wafer and handle wafer are bonded. In most cases the bonding result has been good, but with a large cavity fraction (small bonded area compared to total wafer area) and air as a bonding atmosphere, large voids could be detected with SAM (Figure 32). When either a larger bonded area or vacuum atmosphere was used, no such void problem was detected (Figure 33).

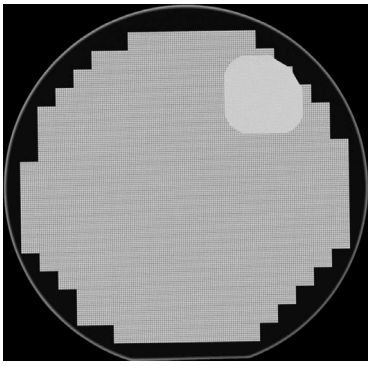

Figure 32. SAM image of air-bonded wafer pair with a cavity fraction of ~80% (500 µm wide square cavity surrounded by 55 µm wide bonding rim).

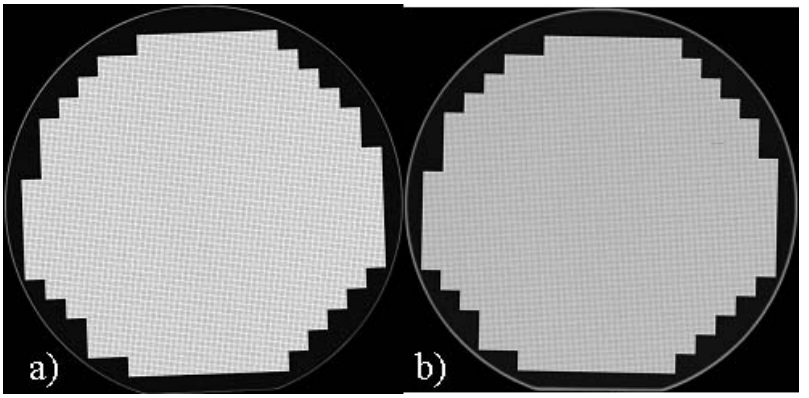

Figure 33. a) SAM image of air-bonded wafer pair with a cavity fraction of ~36% (100 µm wide square cavity surrounded by 55 µm wide bonding rim). b) Vacuum-bonded wafer pair with a cavity fraction of ~80% (500 µm wide square cavity surrounded by 55 µm wide bonding rim).

Vacuum bonding resulted in slightly higher bond strength than air bonding [**Publication C**]. Tests were also performed to study whether small areas can be properly bonded by bonding handle wafers with cavities and small support pillars into the cap wafer and then removing the handle wafer. SEM investigation showed that 100 µm wide pillars were still standing on the cap wafer after handle wafer removal (Figure 34). This means that the support pillar is properly bonded to the cap wafer. Even support pillars with 20 x 20 μm^2 area were found to be well bonded.

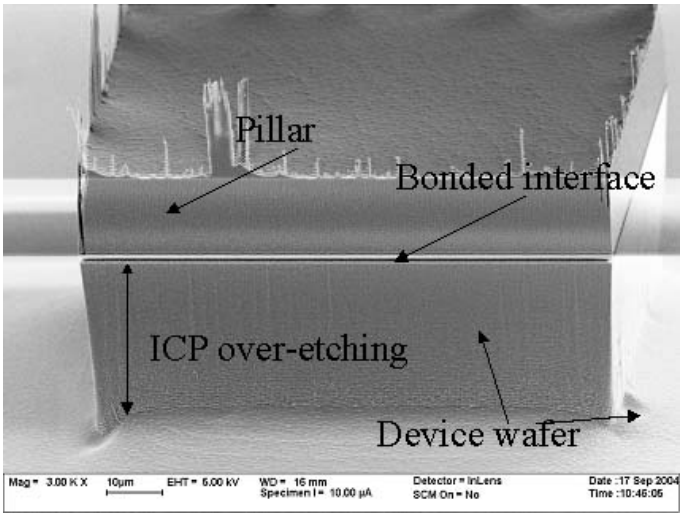

Figure 34. SEM image of 100 µm x 100 µm pillar bonded to the device wafer. The handle wafer is removed with ICP etching.

In cavity SOI wafers, the location of the oxide varies depending on the final application. The oxidation can be done on the cap wafer, the handle wafer before patterning, and the handle wafer after patterning. The first process is straightforward, as the cap wafer is unpatterned and the oxide surface is flat and smooth after thermal oxidation. In the second process care should be taken to avoid roughening of the oxide during cavity fabrication by having a protective layer on top of it, e.g. photoresist. However, in some applications it is desirable to have oxide as well on the bottom of the cavity. The thermal oxidation rate is different in convex and concave corners than on flat surfaces. The oxide profile was measured in the area next to the cavity after cavity fabrication and thermal oxidation with a Veeco Dektak surface profilometer. On these wafers small oxide bumps were detected (width 1–5 µm, height 5–15 nm) next to the cavity (Figure 35). However, these bumps did not cause voids large enough to be detected with SAM or SEM. [**Publication C**]

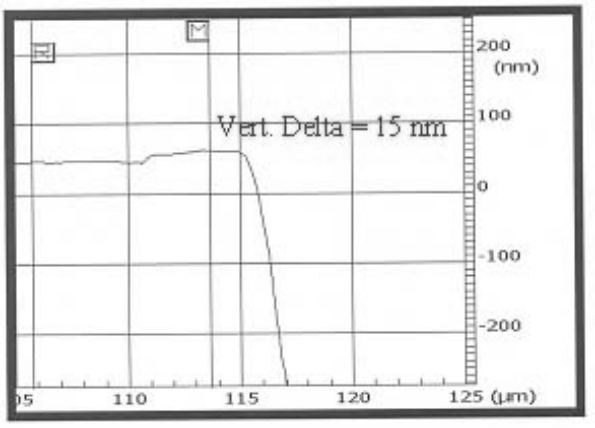

Figure 35. Dektak surface profilometer image of oxide shape next to the cavity.

The next step in cavity SOI fabrication is mechanical thinning. The thinning procedure consists of two grinding and one polishing step. The forces present in the grinding and polishing processes press the film in unsupported areas (areas above the cavities) downwards, causing variation in the SOI film thickness [**Publication C**].

After thinning, the device structure can be defined and released using lithography and ICP etching. Figure 36 shows a MEMS delay line fabricated on a cavity SOI wafer.

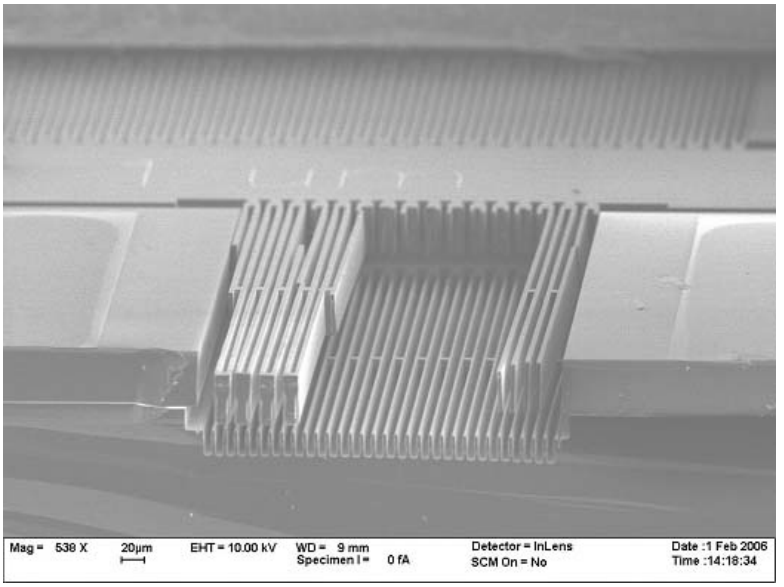

Figure 36. SEM image of a delay line fabricated on cavity SOI wafer. (Picture courtesy of James Dekker, VTT.)

4.1.6 Multi-layer SOI

Some applications may require substrates with more buried layers than just an insulating oxide layer. For example, in some cases it is advantageous to have a buried conductive layer inside the oxide. A boron-implanted polysilicon layer is one such option. In the process (presented in Figure 37) the cap wafer and the handle wafer are thermally oxidized. The silicon layer is then deposited on the handle wafer using LPCVD. The silicon is deposited in the amorphous state, because polishing of amorphous silicon to the surface roughness required for direct bonding is much easier than polishing of polycrystalline silicon. The amorphous silicon is then ion implanted with boron and polished with a short CMP step (removal ~50 nm). It was decided to carry out ion implantation before CMP, as boron implantation was found to roughen the polished surface from ~1 Å RMS to about ~2.5 Å RMS. The wafers were bonded and annealed at 1100°C for 2 hours.

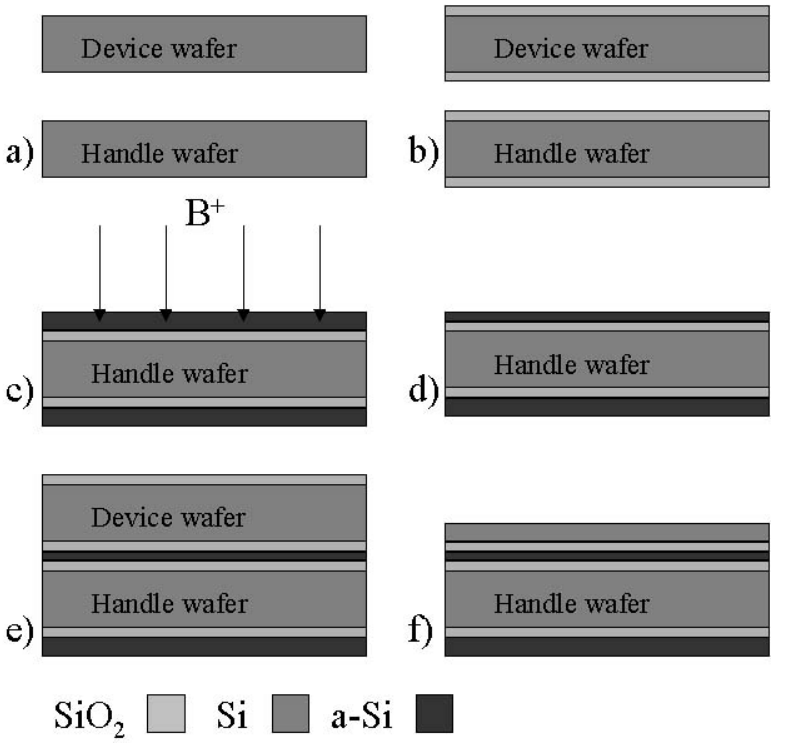

Figure 37. a) Start wafers are standard silicon wafers b) The wafers are thermally oxidized c) The amorphous silicon layer is deposited on the handle wafer with LPCVD and the silicon layer is boron-implanted d) The prime side a-Si is polished with CMP e) The handle wafer is bonded to the device wafer and high-temperature annealing (1100°C) converts a-Si to polycrystalline Si f) The device wafer is thinned to the desired SOI thickness.

Despite the silicon turning from the amorphous state to the polycrystalline state during high temperature annealing, no voids were detected at the bonded interface (Figure 38). The bond strength was also excellent, as can be seen from the SEM image in Figure 39, which shows a polysilicon beam after buried oxide etching of 10 minutes in 50% HF. The etch rate of ~1.5 µm/minute at the bonded interface equals strong bonding (**Publication D**).

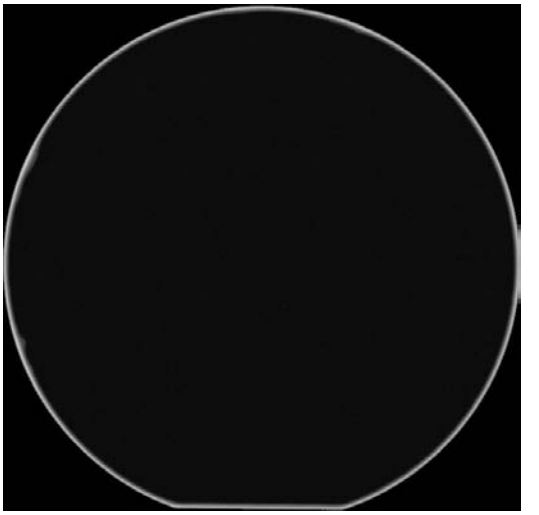

Figure 38. SAM image of a bonded Si-ox-aSi-ox-Si stack.

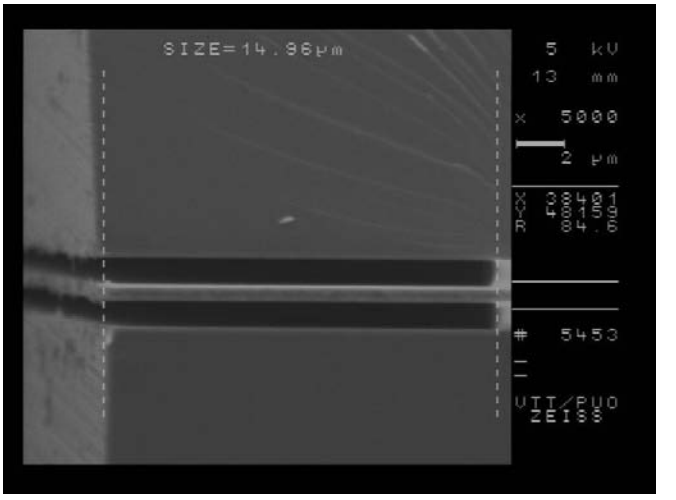

Figure 39. SEM image of a polysilicon beam after buried oxide etching (10 min, 50% HF). The etch rate of both oxides is equal and ~1.5 µm/min, which indicates strong bonding.

4.2 Heterogeneous integration

Heterogeneous integration means the joining of wafers of different materials. Various materials, such as GaAs, InP, Quartz, Glass, Sapphire, SiC, and GaN have been successfully bonded. In such bonding, the same requirements for smooth and clean surfaces apply, but there are further restrictions in the bonding process. In the bonding of dissimilar materials, there is usually a difference in the coefficients of thermal expansion (CTE), which causes stresses during bond annealing. Therefore, the annealing temperatures are usually limited to lower regions than in silicon-to-silicon bonding. Sometimes polishing of the material to be bonded is too difficult or expensive (e.g. SiC is difficult to polish) and an intermediate layer is needed. A good option is then to use a material with known properties and bonding behaviour. Therefore, most common intermediate layers used in direct bonding are polished CVD-SiO_2-layers.

An example of a difficult CTE mismatch is silicon-on-sapphire (SOS) wafers. When bonding silicon to sapphire, the annealing temperature should be kept below 150°C to avoid cracking of the silicon wafer. This causes problems, for example, when trying to make thin film SOS wafers. Low annealing temperature restricts the use of Smart Cut™ after the final bonding. For this purpose a temporary wafer bonding has been developed. In this method the device layer is first fabricated on a temporary handle wafer and then transferred to the final substrate. This method requires controlling of the bond strength during both bonding steps to keep the first bonded interface weaker than the second interface. If the difference between the bond strengths is large enough, the layer can be mechanically transferred from one handle wafer to another. The required steps for this method are shown in Figure 40. The methods for controlling the bond strength are explained in more detail in Chapter 5 and **Publication E**.

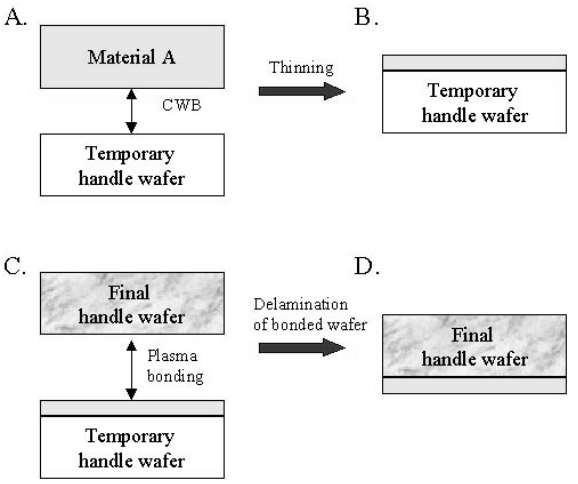

Figure 40. Principle of temporary wafer bonding for high CTE-mismatched materials integration a) Bonding of desired thin film material to temporary handle wafer b) Thinning of the material with ion-cut or mechanical thinning and polishing to make the surface smooth enough for direct bonding c) Low-temperature bonding of the layer to the final handle wafer d) Delamination at the interface between the thin film and temporary handle wafer.

4.2.1 Compliant substrates

Nowadays heteroepitaxy is a common method for fabricating substrates for electronic and optoelectronic purposes. If the layers have the same lattice constant as the substrate, or if the thickness of the layers is kept below their critical thickness, no defects are formed during growth. If the critical thickness is exceeded, the epitaxial layers relax plastically by forming dislocations at the interface. Lattice and thermal mismatches are the main causes of defect formation [53]. These dislocations cause deterioration of the optical and electrical properties of the structure, therefore the amount of dislocations should be minimized. However, this has proved difficult with standard epitaxy. This problem can be avoided by using a compliant substrate. This kind of substrate should accommodate the misfit by deforming elastically or plastically in a zone localized near its top surface, right below the heteroepitaxial layer [54]. The idea of elastic relief was first introduced by Lo [55]. According to his hypothesis, the template as a whole can shrink or expand by slipping along the weak interface.

Several authors have rejected the hypothesis; a more reasonable one is plastic relief of the epitaxial film [56]. In plastic relief the film relaxes by slipping on its crystallographic slip planes, where the slip direction is oblique to the film plane. It may also be that relaxation occurs due to climbing of dislocations instead of slip. However, the final answer regarding the theory behind compliant substrates is still under debate.

There are various methods for fabricating compliant substrates and some of them require wafer bonding. To have an efficient compliant substrate, some criteria should be fulfilled: the layer on which the epitaxy is performed should be as thin as possible, the layer should remain flat and planar and if it is supported, the layer should be free to glide and supporting media should be soft [57].

The first compliant substrates were free-standing thin films, actually GaAs membranes supported at several points (Figure 41a) [58]. However, warping of the film due to stress induced by the deposited epilayer is a serious problem and the method is no longer in use. Another reported freestanding film structure has an InGaAs membrane standing on a central pedestal [59]. However, this structure is fragile and the surfaces are not planar.

Compliant layers when implementing the SOI technique have also been reported (Figure 41b) [60]. In this method the oxide layer is supposed to behave as a viscous layer and a frictionless interface. During epitaxial growth the viscous layer flows, allowing the misfit strain to decrease [61]. As an example of such a compliant substrate, Hansen et al. have reported $In_{0.40}Ga_{0.60}As$ growth on a 10 nm GaAs template on borosilicate glass on a GaAs mechanical host [62]. The viscous intermediate material can also be something else than glass oxide, for example indium.

The most popular option for compliant substrate fabrication has been the use of a twist-bonded layer (Figure 41c). In this method a thin layer of material is transferred to a mechanical host of the same material, but introducing a large twist angle between them. This method was first presented by Ejeckam et al. [63]. The layer is thinned down using either Smart Cut™ [43] or an etch-stop layer and etch-back [63, 54]. The twist-bonded substrate is considered to have a weak boundary due to a network of screw dislocations, which can accommodate the slip resulting from growth of a mismatched layer [53].

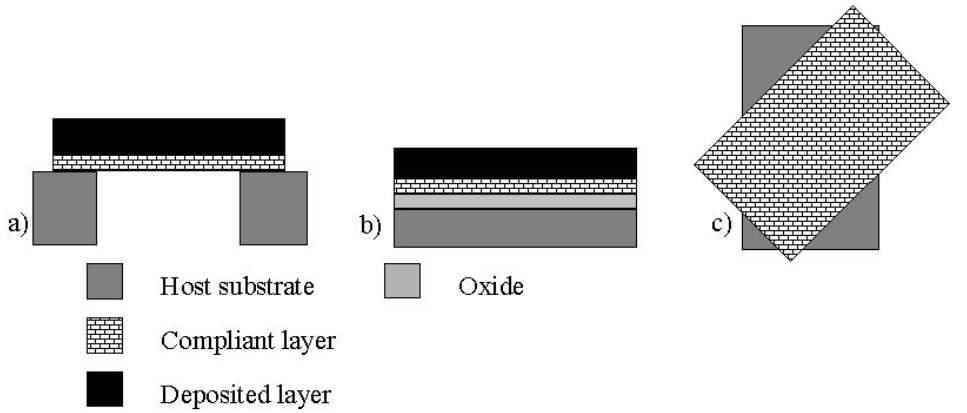

Figure 41. Different compliant substrates a) Free-standing thin film, e.g. GaAs membrane b) Compliant layer on viscous glass c) Twist-bonded layer.

With these different types of compliant substrates, the quality of heteroepitaxially grown layers has increased significantly. Compared with layers grown on ordinary substrates, the density of threatening dislocations has decreased significantly, the relaxation is less or comparable, and the layer thickness is no longer limited to the critical thickness but to a much higher thickness value [57]. While the use of heteroepitaxially grown layers on electrical and optoelectrical applications is increasing, the development of compliant substrates will remain a hot topic in substrate development research.

4.3 Wafer scale packaging

Packaging of MEMS devices is required for various reasons. The sensors are usually delicate components, the operation of which may be sensitive to particles or chemical contaminants. They may also require a specific operation atmosphere (vacuum, inert gas, certain pressure) to function as planned. The encapsulation process should be also cost effective, because nowadays packaging costs can contribute up to 90% of the total device costs. To reduce these costs, the packaging should be done at wafer level, enabling encapsulation of multiple devices on a single run. This can significantly reduce the packaging cost per chip.

Wafer-scale packaging is not a new approach in the MEMS industry. The most common methods are anodic bonding and glass frit bonding. These methods, however, have limitations such as high temperature (400–600°C) and a large bonding area. These processes also involve metals that are not compatible with ICs sometimes required with the MEMS device. Agilent uses gold seal bonding to encapsulate their devices [24] and Ziptronics uses covalent bonding for wafer-scale encapsulation [42].

Publication B examines methods for direct bonding of a silicon wafer to another silicon wafer containing MEMS devices at low temperature. To achieve strong bonding at low temperatures, plasma activation of wafer surfaces is used before contacting the wafers. The advantages of the plasma-activation based process over glass frit and anodic bonding are a lower process temperature, high throughput, IC compatibility and the possibility to have a small bonding rim. The problem with this method is that the areas to be bonded have to be very smooth and flat, which is usually not the case with processed wafers. Therefore, the device wafer usually needs planarization and/or polishing before direct bonding can take place.

There are three principal steps in the encapsulation of MEMS devices with direct bonding: Planarization and polishing (including surface protection during further processing), bonding itself, and fabrication of electrical contacts into the package.

4.3.1 Planarization and polishing

To make the handle wafer bondable, it needs to be planar and smooth in the areas to be bonded. For this purpose three different approaches were tested: a) covering of the whole handle wafer with thick CVD-oxide, followed by global planarization and smoothening (Figure 42); b) planarization, polishing and protection of the areas to be bonded before actual device fabrication (Figure 43); c) covering of the whole handle wafer with CVD oxide, removal of the oxide from the top of the device and polishing of the elevated oxide areas (Figure 44).

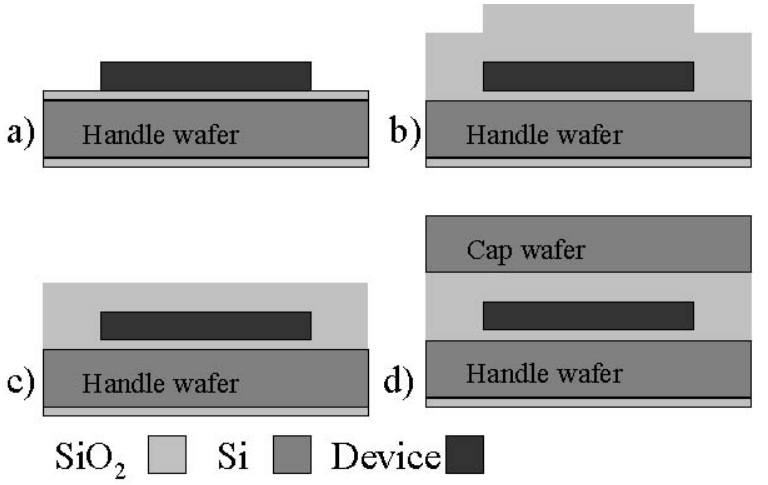

Figure 42. a) Device fabrication on oxidized wafer b) Covering of the device with CVD oxide c) Planarization and polishing d) Bonding of cap wafer.

The first proposed method can be done with conventional oxide polishing processes, but it requires a large amount of extra oxide polishing before the step, caused by the buried device, is planarized. Typically the required removal is about twice the height of the hill. By using polishing pads with fixed abrasives, the main part of the removal takes place at the elevated areas and the 800 nm high surface step can be planarized by removing less than 1000 nm of oxide [**Publication B**].

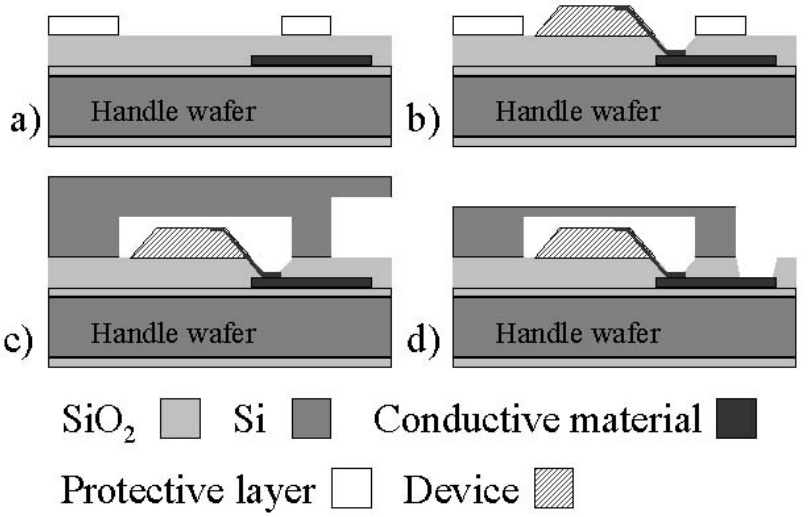

Figure 43. a) Fabrication of conductive path on thermally oxidized Si, CVD oxide deposition, planarization and polishing and deposition and patterning of protective layer b) Device fabrication and contact fabrication from device to conductive path c) Removal of protective layer and aligned bonding to patterned cap wafer d) Thinning of cap wafer for contact opening.

In the second proposed method, the surface of the oxide layer is polished before device fabrication. The areas to be bonded can be polished with a conventional oxide polishing step. The difficult part in this method is to protect the oxide surface during device fabrication so that no roughening of the oxide takes place. The protective layer should also be selectively removable from the top of the oxide. Molybdenum is a good protective layer, for example during release etching with HF, and it can be selectively removed from the oxide surface with mild SC-1 cleaning (NH_3:H_2O_2:H_2O solution). If buffered HF is used for release etching, then also standard photoresists can be used for surface protection. The resist can be removed with various solvents and developers without roughening the oxide surface. With complex devices this method is difficult or impossible to use, because it is hard to find a protective material that could withstand all the various process steps and still be easily removable from the oxide surface afterwards.

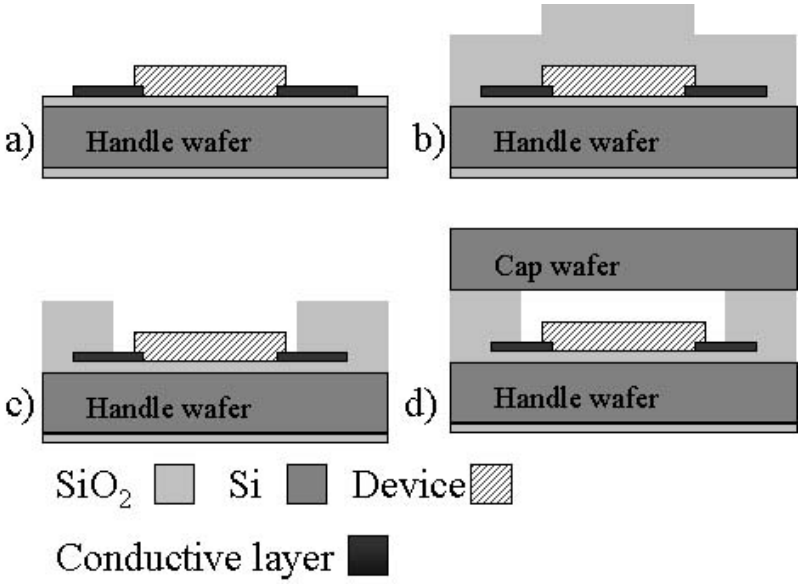

Figure 44. a) Device and conductive path fabrication b) Covering of the device with CVD oxide c) Oxide etching from top of the device and polishing of elevated oxide areas d) Bonding to cap wafer.

The third option is to fabricate the device first, cover it with CVD oxide, remove it from the top of the device, and then polish the areas to be bonded. With typical polishing processes the problem is rounding of the corners of the oxide "walls", which especially with a narrow bonding rim areas drastically reduce the area to be bonded (Figure 45b&c). By again implementing the fixed abrasive polishing process, the elevated oxide areas can be polished without detectable edge rounding (Figure 45d).

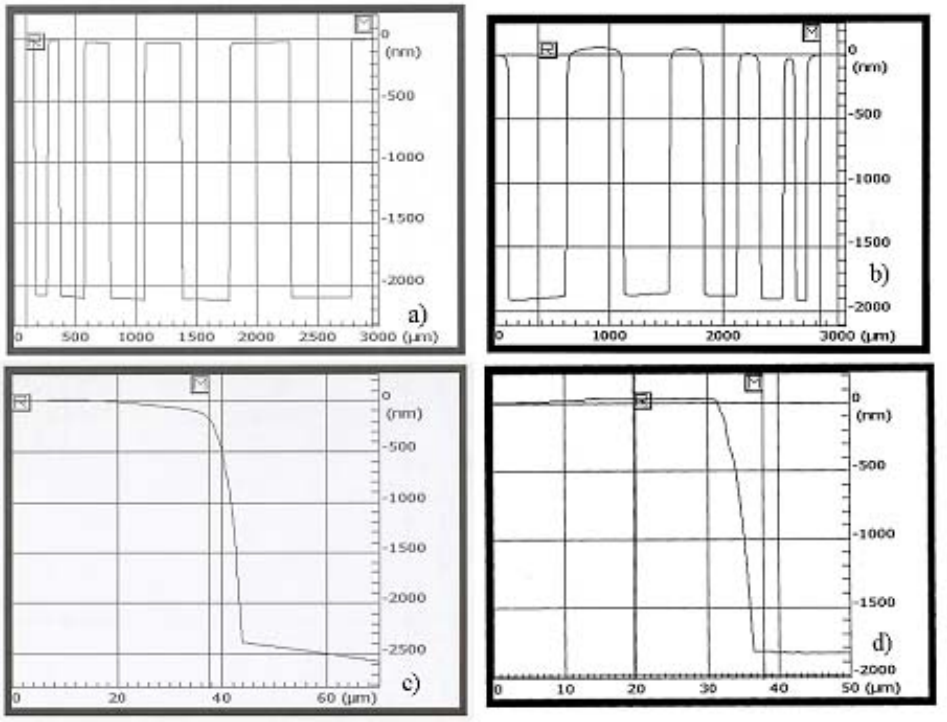

Figure 45. Surface profiles of elevated oxide areas a) After patterning b) After conventional oxide polishing process c) Oxide pillar profile after conventional oxide CMP d) Oxide pillar profile after fixed abrasive polishing process.

The encapsulation process needs to be decided upon already when designing the MEMS and its fabrication process.

4.3.2 Direct bonding of MEMS wafer

Direct bonding of wafers containing MEMS devices must in most cases be carried out at low temperature. The temperature of 1100°C needed for the high-temperature bonding process is too high for possible metallizations and other temperature sensitive parts, and also causes outgassing (and void formation) from the CVD oxides. Therefore, plasma activation should be used for both wafer surfaces to achieve strong bonding already at 200°C. In cases where the cap wafer is patterned, aligned bonding should be used.

The main thing to remember in direct bonding of wafers containing MEMS is the same as with any other direct bonding processes: the areas to be bonded must be smooth and clean. Therefore, it is important to highlight again the need for good CMP processes and the importance of having particle-free processes.

4.3.3 Fabrication of electrical contacts

In **Publication B** two different methods for fabrication of electrical contacts are presented. The first possibility is to use a patterned cap wafer which contains wells for contact opening. The wells are aligned during bonding above the contact pads, and during cap wafer thinning the wells are opened and a path to the contact pads is created (Figure 43). The encapsulated device can then be contacted to the next level, for example by wire bonding (Figure 46).

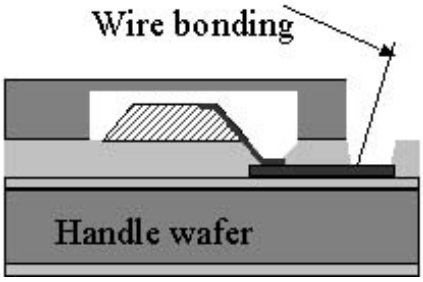

Figure 46. Contact fabrication with wire bonding for encapsulated device, continuation of the process presented in Figure 43.

The second approach is to use a dicing saw for the contact opening. The bonded cap wafer is first thinned down to <100 µm thickness. Next the v-shaped dicing blade is used to cut through the remaining handle wafer, slightly penetrating the contact pads. After this, a layer of conductive material, e.g. molybdenum, is deposited onto the v-groove and patterned (Figure 47). Then, for example, solder bumps can be grown on top of the cap wafer to make the final contacts to the next level.

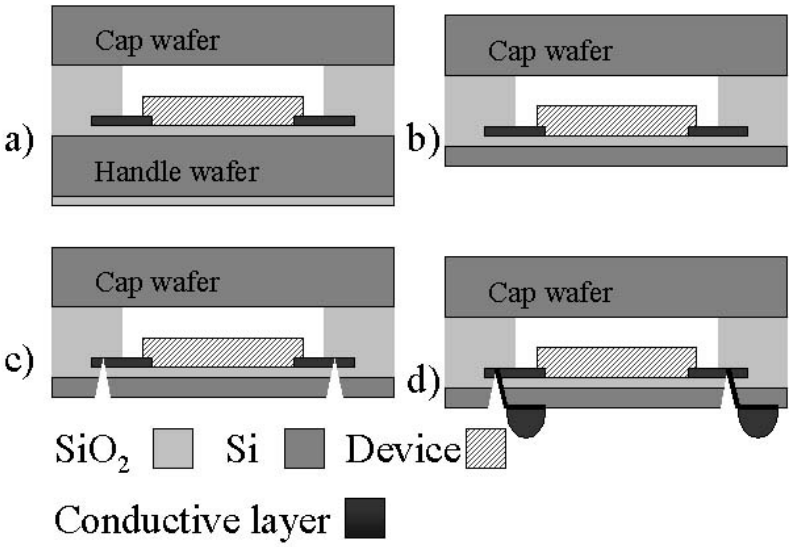

Figure 47. Contact fabrication with an encapsulated device, continuation of the process presented in Figure 44. a) Encapsulated device b) Thinning of the handle wafer c) V-groove sawing through the handle wafer and contact pads d) Conductive material deposition into the groove, patterning and solder bumping.

5. Temporary wafer bonding

Temporary wafer bonding means bonding of wafers to a temporary substrate so that they can easily be released afterwards. The principle of the method is presented in Figure 48 and explained in more detail in **Publication E**. The main principle of the method is that the crack propagates on the weakest interface. Therefore, if the bonding between the temporary holder wafer and the thin film is weaker than between the thin film and the final handle wafer, the film can be transferred to the final substrate. In practice, the difference should be significant (> 500 mJ/m^2) to avoid "jumping" of the crack from one interface to another.

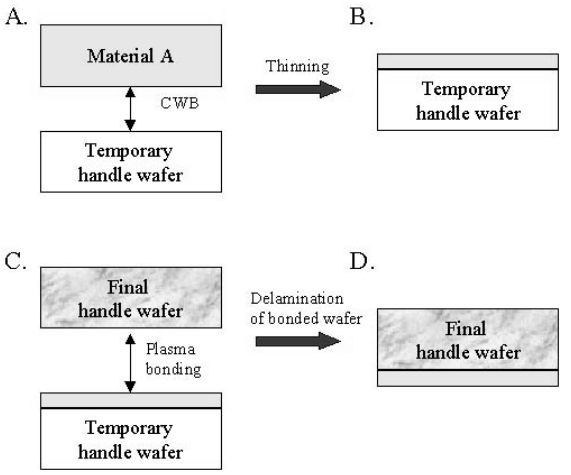

Figure 48. Principle of temporary wafer bonding a) Bonding of the desired thin film material to the temporary handle wafer b) Thinning of the material with ion-cut or mechanical thinning, and polishing to make the surface smooth enough for direct bonding c) Low-temperature bonding of the layer to the final handle wafer d) Delamination at the interface between the thin film and the temporary handle wafer.

The use of a temporary handle wafer is advantageous in many cases, such as wafer thinning and heterogeneous integration. For example, the quality of ion-cut silicon-on-glass (SOG) layers can be improved by removing ion implantation induced crystalline damage from the silicon film with high temperature annealing (at >1000°C). However, the glass substrate cannot withstand temperatures over 600°C and annealing before bonding is out of the question

because of the blistering effect. Therefore, the annealing should be done while the thin film is on a temporary handle (Si) wafer.

Temporary wafer bonding is also a usable method in fabrication of silicon-on-sapphire (SOS) wafers. Coefficients of thermal expansion (CTE) vary between silicon and sapphire so that the bonded silicon-sapphire wafer pair starts to break at temperatures over 150°C. However, the ion-cut requires annealing temperatures of ~200°C even if boron implantation and mechanical delamination are used [46]. The SOS wafer can be fabricated by first bonding the implanted silicon wafer to the oxidized silicon wafer without plasma activation, then doing a thermal ion-cut at 500°C. The transferred Si-layer is then polished to reduce the surface roughness from a split roughness of ~3 nm RMS to ~1 Å RMS. On a sapphire wafer, the PECVD oxide layer should be deposited to avoid void formation during bonding. PECVD oxide should also be polished to enable direct bonding. After ion-cut annealing, the bond strength of the temporary bonding is <1000 mJ/m^2. By using plasma activation on both surfaces and long annealing at 120°C, bonding between the sapphire and silicon layer could be made much stronger than the temporary bonding. After mechanical delamination, the surface roughness of the transferred layer was ~1 Å RMS, which is close to the surface roughness of the donor wafer at the start of the process. A thin film SOS wafer is shown in Figure 49.

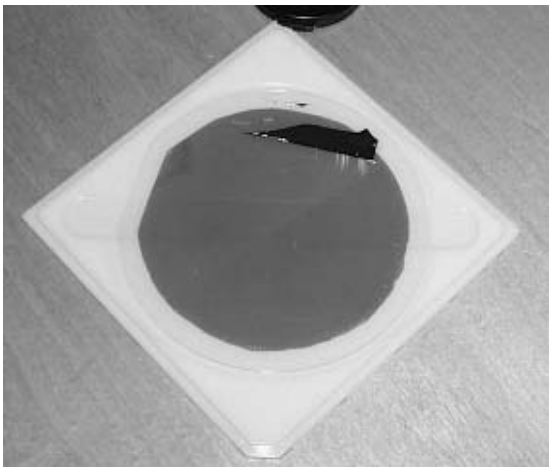

Figure 49. Picture of thin Si layer on a sapphire wafer.

The third application would be the fabrication of cavity SOI wafers (Figure 50). As mentioned in chapter 4.5.1, mechanical thinning induces thickness variation in diaphragms above cavities. Therefore, it would be advantageous (especially with thin diaphragm thicknesses) to do the thinning while the SOI layer is on the temporary substrate. Once the SOI layer is thinned to desired thickness, it is bonded to the patterned wafer and the temporary handle is removed by debonding.

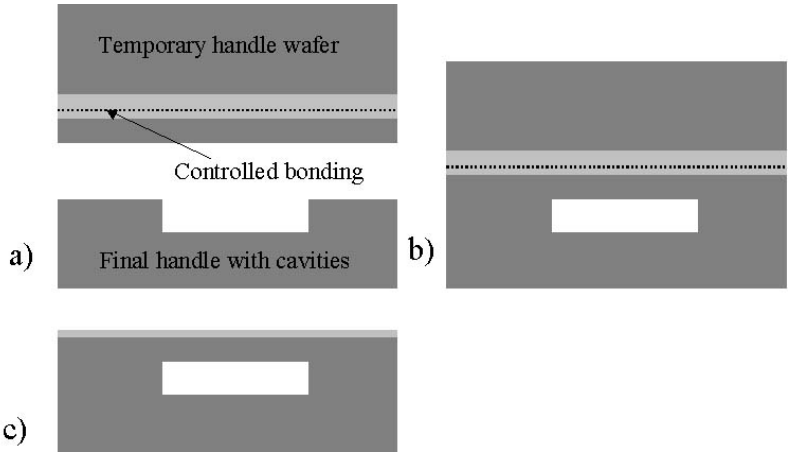

Figure 50. Temporary wafer bonding for cavity SOI fabrication a) Fabrication of SOI wafer with weak bonded interface b) Bonding of temporary SOI wafer to cavity wafer c) Mechanical delamination for removal of the temporary handle.

With this method it is also possible to carry out double side processing on the SOI layer. In this case one side of the SOI layer is processed while it is bonded to the temporary substrate. After bonding and debonding, another side of the SOI layer can also be processed. It is also possible to stack many processed SOI layers on the same handle wafer. [**Publication E**, 64]

5.1 Temporary wafer bonding using impurity outgassing of CVD oxides

Impurity outgassing of CVD oxides can be used for temporary wafer bonding. As mentioned in the chapter on bonding of CVD oxides, trapped impurities start to outgas when the bond annealing temperature exceeds the film deposition

temperature. Use of this behaviour in temporary wafer bonding was tested by bonding a PECVD oxide layer to a silicon wafer using plasma activation and annealing at 200°C. After this bonding procedure, the bond is strong. Then the cap silicon wafer was thinned down to a thickness of 20 µm by grinding and polishing. After polishing, the surface roughness of the SOI layer was low enough to enable good bonding. This SOI wafer was then bonded to a thermally oxidized wafer with plasma activation and the wafer stack was annealed at 500°C. At this temperature, the first made bonded interface weakens due to impurity outgassing (Figure 8b) while the second interface gets stronger. After annealing, a razor blade was inserted between the wafers and the crack propagated on the weaker PECVD oxide / silicon interface. After complete separation the 20 µm SOI layer was successfully transferred to another substrate. The new SOI wafer had some residual PECVD oxide on the surface due to crack propagation partly inside the CVD oxide layer. After short a HF dip the oxide residues were removed and the silicon surface was found to be smooth (~1Å RMS).

5.2 Temporary wafer bonding using surface roughening

The requirements for spontaneous direct bonding to take place are smooth and clean surfaces. The surface roughness limit is ~1 nm RMS and usually the silicon and oxide surfaces have a surface roughness of 1–2 Å RMS. **Publication E** describes how increasing the surface roughness within the limits of spontaneous bonding affects the bond strength. Similar results have been published by Moriceau et al. [64]

The optimal target would be to have a controlled surface energy (of 700–1200 mJ/m^2) for a temporarily bonded wafer pair after annealing at temperatures ranging from 200°C to 1100°C. This would enable thermal ion-cut at low temperatures and removal of the ion-implantation induced crystalline damage with high temperature annealing before moving the thin film to the final substrate. If the bond strength is below 500 mJ/m^2 at the thermal ion-cut temperature, instead of a thermal cut blistering and debonding will occur.

The experiments focused mainly on roughening of thermally grown oxide with plasma etching. After several tests, the best process for roughening the oxide

surface was found to be 30s CHF_3 plasma etching, which resulted in a surface roughness of ~8 Å RMS (Figure 51).

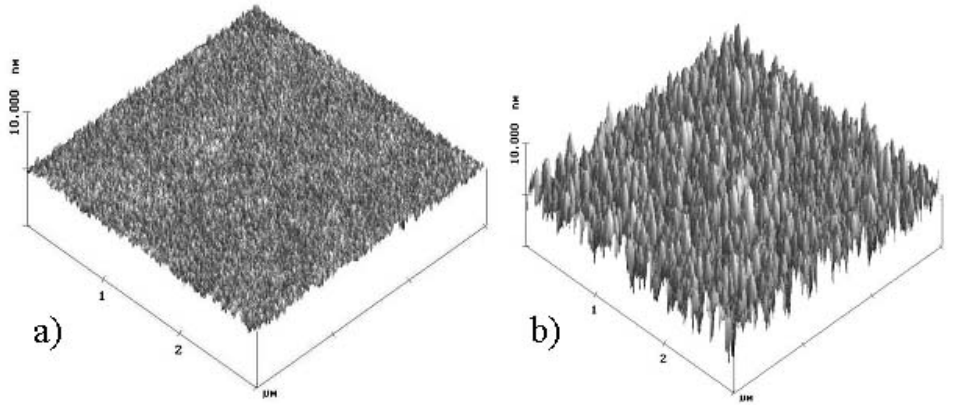

Figure 51. AFM images of a) as grown thermal oxide (RMS ~2 Å) and b) roughened thermal oxide (RMS ~8 Å).

Figure 52 presents measured surface energies for roughened and bonded SiO_2 wafers after annealing at different temperatures. Roughening of surfaces has a clear influence on the bonding energy and the bond strength remains at a level still debondable after annealing at 1100°C. However, with roughened surfaces the bond strength at temperatures < 500°C is not sufficient for thermal ion-cut.

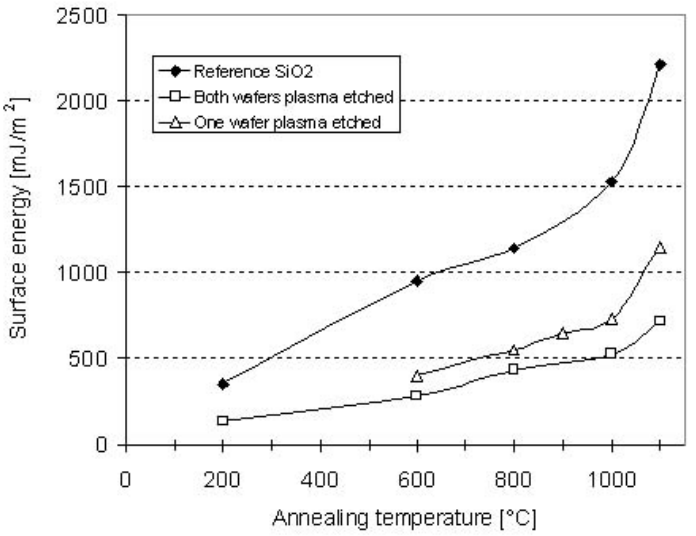

Figure 52. Bond strength as a function of annealing temperature for oxide-oxide wafer pairs with and without surface roughening. Annealing time was 2 h.

To improve bond strength at low annealing temperatures, plasma activation was combined with surface roughening. The plasma activation of the roughened surface seemed to remove the influence of the roughening somewhat, and the bond strength at high temperatures was similar or higher to that in reference samples (Figure 53). By plasma-activating one wafer and roughening the other, the desired results were obtained enabling ion-cut at 400°C (bond strength ~500 mJ/m^2) and debonding after high temperature annealing (~1200 mJ/m^2).

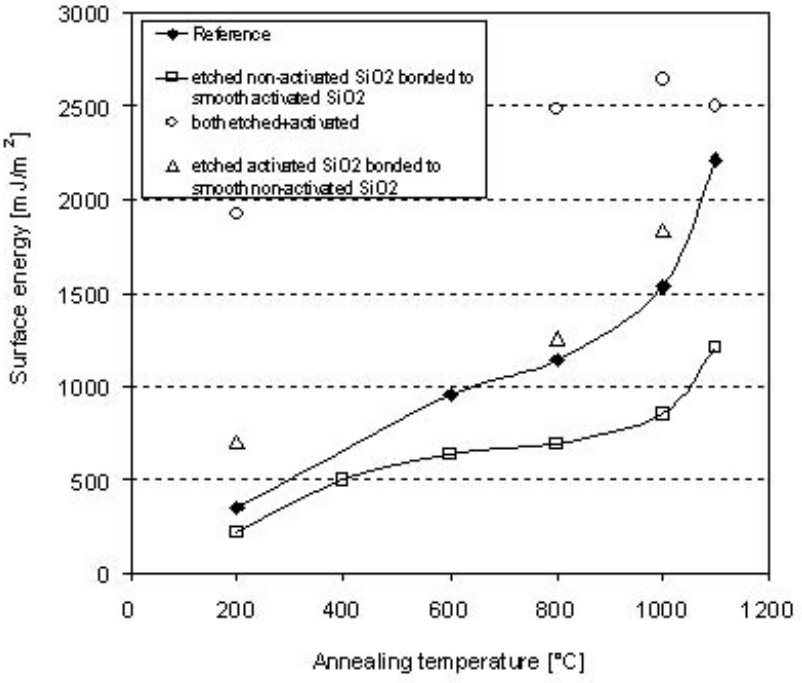

Figure 53. Measured bond strengths for oxide-oxide wafer pairs as a function of annealing temperature after different roughening and plasma activation procedures. Annealing time was 2 h.

6. Summary

The purpose of this work was to study silicon direct bonding processes and evaluate the influence of different pre-bonding treatments on the bond quality. The main focus was on studying the effect of plasma activation before bonding on the bond strength. The influence of other pre-bonding treatments such as chemical-mechanical polishing (CMP), lithographical surface patterning and surface roughening was studied while developing bonding processes for various applications. These applications included heterogeneous integration for fabrication of silicon-on-glass (SOG) and silicon-on-sapphire (SOS) substrates, bonding of patterned wafers for fabrication of SOI substrates with buried cavities, and bonding of wafers with MEMS devices for wafer scale packaging.

The plasma-activation based bonding process reduces the required annealing temperature to achieve strong silicon to thermal oxide bonding from 1100°C to <200°C. Plasma is assumed to create a porous layer on the oxide surface, which helps the water diffuse out from the bonded interface at low temperature. The plasma activation effect can be lost by excess SC-1 cleaning after activation.

The plasma activation-based bonding process has been found to be a suitable method for MEMS encapsulation at wafer level. Covering the wafer with LPCVD oxide and using it as an intermediate bonding layer was found to be a viable method for encapsulation. Suitable CMP processes were found for LPCVD oxide planarization and polishing. By using a protective layer above areas to be bonded during further processing, surface roughening could be avoided. Two methods were developed for fabrication of electrical contacts in the package. Contact pad opening by grinding or sawing enables electrical contact to the package without losing the hermeticity of the package.

Patterning, bonding and mechanical thinning is a viable method for fabricating SOI wafers with buried cavities. Such new substrates enable fabrication of MEMS components difficult or impossible to fabricate on conventional Si or SOI wafers.

Bond strength is usually measured with the crack opening method or a chevron test. The former requires a place for blade insertion, and is therefore unsuitable for thinned or diced samples. It also has problems measuring high bond strengths

or fragile samples due to sample breakage during measurement. The latter method is accurate but requires pre-patterning before bonding and is therefore time-consuming. The HF etching test was found to be a suitable method for measuring bond strength from ready-made SOI, small samples or small bonded areas. In the method the buried oxide is etched in HF and the etched distance is measured. In direct bonding of hydrophilic silicon, the bond strength was found to be logarithmically dependent on the bond strength. The etched distance can be measured by cross-sectional SEM or IR microscopy.

The mechanical exfoliation of hydrogen implantation and bonded Si is a suitable method for fabrication of thin film silicon-on-insulator and silicon-on-glass substrates. In mechanical exfoliation the crack propagates on the weakest interface, therefore it is necessary to achieve a high bond strength at low temperature by using plasma activation. With this method the mechanical transfer of hydrogen-implanted Si is possible after annealing at 200°C. The strength of the implanted layer is dependent not only on the hydrogen dose, but also on crystalline orientation and boron doping. High boron doping (implantation dose of 3e15 cm^{-2}) combined with hydrogen implantation was found to decrease the required annealing temperature for mechanical exfoliation of about 80°C compared to a sample with hydrogen implantation only.

Controlling of the bond strength is possible with different surface preparations. By slightly increasing the surface roughness of wafers to be bonded, the bond strength can be limited to a level that is still mechanically debondable after high temperature annealing (1100°C). For example, the crystalline damage due to hydrogen implantation in ion-cut Si layers could be removed by high temperature annealing on temporary substrate before transferring the Si film onto a temperature-sensitive final substrate.

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Effects of Plasma Activation on Hydrophilic Bonding of Si and SiO_2

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Effects of Plasma Activation on Hydrophilic Bonding of Si and SiO_2

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Low-temperature bonding of Si wafers has been studied utilizing reactive ion etching-mode plasma activation. The hydrophilic Si and thermally oxidized Si wafers were exposed to N_2, Ar, or O_2 plasma prior to bonding in air or vacuum. After plasma treatment the wafers were cleaned in RCA-1 solution and/or deionized water. Strong bonding was achieved at 200°C with all the investigated plasma gases, if proper bonding and cleaning procedures were used. Extended RCA-1 cleaning deteriorated the bond strength, but a short cleaning improved bonding. We found that the activation of the thermal oxide has a larger influence on the bond strength than the activation of the native oxide surface in Si/oxide wafer pairs. We suggest that the plasma treatment induces a highly disordered surface structure, which enhances the diffusion of the water from the bonded interface. As a result of the plasma exposure the number of the surface OH groups is greatly increased enabling strong bonding at a low temperature.
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Direct bonding of hydrophilic silicon wafers can be applied to the fabrication of silicon-on-insulator (SOI) structures and advanced microelectromechanical and optical devices. Wafer bonding usually requires high-temperature annealing above 1000°C to achieve strong bonding between the wafers. When bonding preprocessed wafers it is essential to restrict the annealing temperature in order to avoid undesirable changes and reactions in the substrate structures. In the case of materials with different thermal expansion coefficients excessive stresses may arise in the bonded wafer pair. Therefore, it is mandatory to find a low-temperature bonding process that results in strong bonding at temperatures below 400°C.

It has been reported that strong hydrophilic bonding with Si can be achieved at a low annealing temperature (<400°C) by exposing the wafers to a low pressure plasma prior to the bonding.[1-3] Alternatively, surfaces can also be activated with ion bombardment in vacuum.[4] The plasma of various gases, including O_2 and Ar, have been found to yield similar results.[1,3] Infrared spectroscopic measurements have confirmed that the bond strengthening in hydrophilic bonding of Si is due to the formation of covalent siloxane bonds (Si-O-Si) at the bonded interface.[3,5] This reaction which involves dissociation of silanol groups at the interface can take place even at room temperature. The resulting bond strength is limited by the number of silanol groups available for the bonding reaction. Further bonding only occurs at higher temperatures via plastic flow and distortion of the silica tetrahedra. Ion bombardment by plasma exposure or by incident ion beam is known to create structural defects on a Si surface.[6] The particles and ions impinging on a Si surface also have a charging effect.[6] It has been proposed that the disordered surface structure is responsible for the increased reactivity of the surface.[1] Farrens *et al.* have suggested that the increased oxidation rate (Si-O-Si bond formation) at the bonded interface is due to the plasma induced surface charge.[2] Amirfeiz *et al.* found no evidence to substantiate this hypothesis.[3] They suggested that plasma treatment creates a porous surface structure which enhances the diffusivity of water molecules from the bonded interface. In summary, a number of experiments with varying, sometimes conflicting, results have been published on plasma-activated Si wafer bonding. This suggests that the effects of plasma activation are not fully clarified yet.

We have studied the influence of various plasma and bonding parameters on the hydrophilic bonding of Si and SiO_2 using alternative surface treatment procedures prior to bonding. The bonded interface strength was measured with the crack-opening method,[1] and the voids at the bonded interface were studied with scanning acoustic microscopy (SAM).

Experimental

In the experiments, ⟨100⟩ oriented p-type Czochralski grown silicon wafers with a diameter of 100 mm were used. The resistivity of the wafers was 1-10 Ω cm. A thermal wet oxide layer with a thickness of 500 nm was grown at 1050°C on part of the wafers to be used for hydrophilic Si to SiO_2 bonding (oxide/Si bonds) and SiO_2 to SiO_2 bonding (oxide/oxide bonds). Prior to bonding, the wafers were activated in a reactive ion etcher (RIE, Electrotech) using argon, oxygen, or nitrogen plasma. During the plasma exposure the chamber pressure was 50-150 mTorr with the gas flow set at 30 sccm. The rf power was varied between 50 and 150 W. With these parameters the bias voltage at the substrate electrode varied between 125 and 280 V. The duration of the plasma exposure was varied between 10 s and 10 min. After the plasma treatment the wafers were cleaned in an RCA-1 (NH_3:H_2O_2:H_2O, 70°C) solution and/or deionized water (DIW). To study the influence of the cleaning step on the bond strength, different cleaning times were used. After cleaning, the wafers were dried in a spin dryer. The wafers were subsequently bonded in a commercially available wafer bonder (Electronic Visions EV801). The bonding was carried out either in air or in vacuum usually at room temperature or in some cases at 150°C. The bonded wafer pairs were annealed for 2 h at 100°C. After this first annealing step the wafers were cut into rectangular slices using a dicing saw. The diced samples were annealed for 2-100 h at 100-500°C. The surface energies of the diced samples were measured in air using the crack-opening method.[1] The bonded wafer pairs were inspected for interfacial voids using IR transmission imaging and scanning acoustic microscopy (Sonix UHR2000). The surface roughness of the plasma-activated surface was measured with a Digital Instrument D3100 atomic force microscope (AFM) using silicon tips in the tapping mode.

Results and Discussion

The surface energy of SiO_2/Si bonds as a function of annealing temperature is shown in Fig. 1 for different surface activation treatments. For reference, the surface energy of the nonactivated oxide/Si bonds is depicted in Fig. 1b. For nonactivated oxide/oxide bonds we have measured approximately the same surface energy. The wafers were exposed to oxygen, argon, or nitrogen plasma and subsequently cleaned with RCA-1 and/or DI water before bonding in air. Strong bonding is observed for all plasma species investigated after annealing up to 300°C, if a proper cleaning procedure is used. For example, a short RCA-1 cleaning step for 45 s results in strong bonding whereas extended RCA-1 cleaning deteriorates the bond

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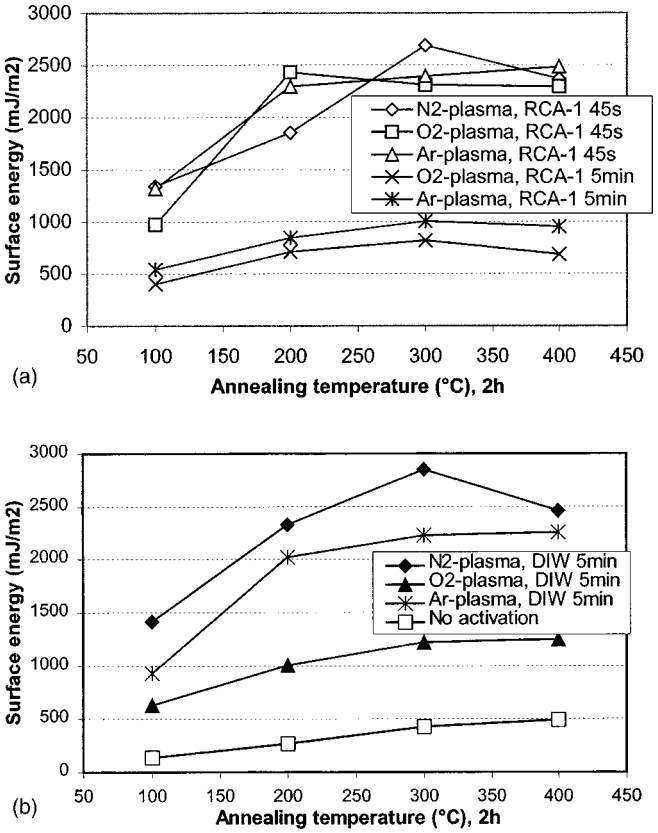

Figure 1. (a) The surface energy of oxide/Si bonds for different plasma gases and for different RCA-1 cleaning times. The bias voltage at the substrate electrode was ~200 V, and the plasma exposure time was 30 s. The wafers were bonded in air. The bond annealing time was 2 h. (b) The surface energy of oxide/Si bonds for different plasma gases. The subsequent cleaning was performed in DI water. The surface energy of the nonactivated oxide/Si wafer pair is shown as a reference. The bias voltage at the substrate electrode was ~200 V, and the plasma exposure time was 30 s. The wafers were bonded in air. The bond annealing time was 2 h.

strength. Our results also show that for wafers exposed to an oxygen plasma DIW rinse is not effective in bringing about strong bonding.

Bonding experiments using plasma activation with a varying bias voltage and exposure time were also carried out. A short plasma exposure up to 30 s was found to be more efficient than a treatment lasting several minutes. The AFM measurements show that an extended plasma exposure increases the surface roughness. A surface roughness of 2 Å was measured for a Si wafer activated with Ar plasma for 10 min, as compared to a roughness of 1 Å for an untreated sample. Plasma activation at a 200 V bias voltage lasting less than a minute was not found to have any effect on the surface roughness. Figure 2 shows the measured surface energy as a function of the bias voltage for a wafer pair exposed to an oxygen plasma for a constant time of 30 s. The bias voltage was controlled by adjusting the plasma pressure and power. When measured after a heat-treatment at 200°C the bond strength increases with an increasing bias voltage if the wafers are cleaned with an RCA-1 solution after the plasma exposure. When the cleaning is carried out in DIW, the influence of the ion energy is less pronounced. Our results suggest that the activation extends to a depth controlled by the average ion energy in the RIE process. Increasing the bias voltage results in ions penetrating deeper into the wafer.[6] Figure 3 shows simulated profiles of O_2, N_2, and Ar implanted at 200 eV into SiO_2.[7] The projected range of 200 eV O_2^+, N_2^+, and Ar^+ ions varies between 1 and 2 nm. This shallow surface layer is very reactive and readily adsorbs water from the cleaning solution. Measurements us-

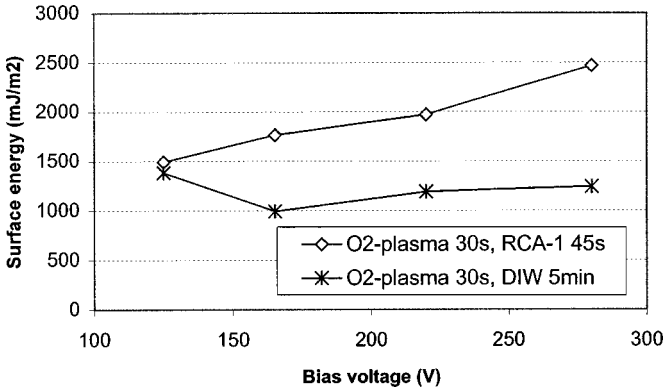

Figure 2. The influence of the bias voltage on the bond strength of oxide/Si bonds. The bonding was performed in air after which the bonded wafer pairs were annealed at 200°C for 2 h.

ing optical ellipsometry show that RCA-1 cleaning for 5 min after plasma exposure removes a 5 nm layer from the surface of the activated oxide. Therefore, we conclude that in the RCA-1 bath the damaged layer induced by plasma is consumed and eventually the activation is lost, as we have observed for extended cleaning times. This etchback process is less effective when the bias voltage and penetration depth of the ions increase.

While a surface energy of >2000 mJ/m^2 was obtained for oxide/Si bonds, the surface energy of oxide/oxide bonds remained below 1500 mJ/m^2 with all the activation treatments (Fig. 4). The observation is consistent with earlier results on low temperature bonding of hydrophilic Si.[8] The silanol groups (Si-OH) of opposing surfaces can react and polymerize even at room temperature provided that they are in close proximity.[1] Therefore, the interface water trapped between the hydrophilic wafers has to be removed before the polymerization of the Si-OH groups can take place. If one of the wafers is covered with a thin native oxide layer, the water can diffuse to the oxide/Si interface and oxidize silicon, even at a low temperature. When both wafers are covered with a thick oxide layer, the diffusion of water to the oxide/Si interface is hampered at low temperatures.

A mass spectroscopic analysis of the wafer pairs bonded without plasma activation has proved that the interface water can oxidize Si generating molecular hydrogen at the bonded interface.[9] Hydrogen gas was also found to be the main constituent inside the cavities (voids) after annealing at <700°C. We carried out experiments where two unoxidized hydrophilic Si wafers were bonded (Si/Si

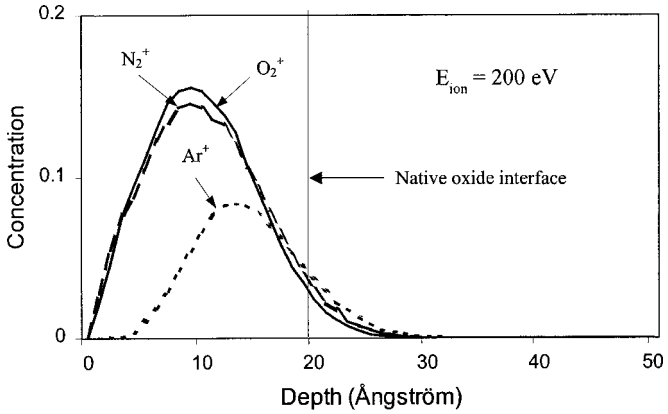

Figure 3. The distribution profiles of 200 eV O_2^+, N_2^+, and Ar^+ in Si O_2 simulated using the SRIM2000 code.[7] The approximate thickness of the native oxide is given as a guideline.

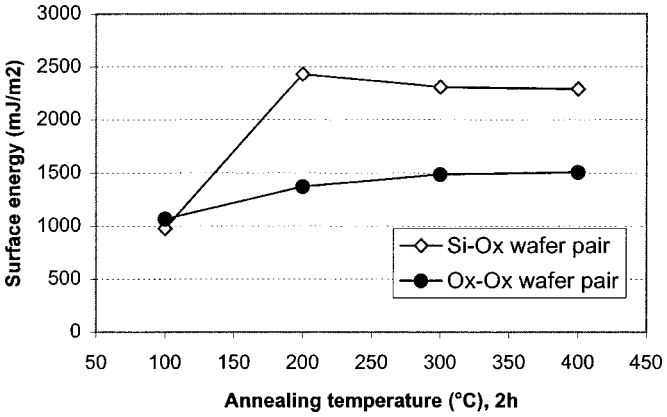

Figure 4. Comparison of Si/oxide and oxide/oxide bonds. The wafers were activated with oxygen plasma (30 s) followed with RCA-1 cleaning (45 s). The wafers were bonded in air. The bond annealing time was 2 h.

bonds) using different plasma activation treatments. A large number of presumably hydrogen-induced voids was observed by scanning acoustic microscopy (SAM) after annealing at 100-400°C (Fig. 5a). No hydrogen-induced voids were found in hydrophilic silicon-to-oxide and oxide-to-oxide wafer pairs (Fig. 5b). The result is in agreement with the reported behavior of the voids in wafer pairs bonded without plasma activation.[1] This suggests that the plasma-enhanced bonding process involves a similar oxidation reaction as the conventional hydrophilic Si wafer bonding.

The molecular water resulting from the polymerization of Si-OH groups may either out diffuse along the bonded interface or react with Si according to $2H_2O + Si \rightarrow SiO_2 + 2H_2$.[1] The difference in bond strength at 200°C between oxide/Si and oxide/oxide bonds and the behavior of the voids suggest that most of the interface water is consumed by oxidation reaction if at least one of the oxide layers is sufficiently thin.

Figure 6 presents the measured surface energy for oxide/Si wafer pairs bonded with the O_2 plasma activation but in different atmospheres. A reduced surface energy of 1000 mJ/m^2 was measured for the samples which had been bonded in vacuum or at 150°C in air in contrast to the values of $>$2000 mJ/m^2 obtained for the wafer pairs bonded in air at room temperature. The molecular water is known to desorb from a Si wafer surface at above 110°C.[1] It is then reasonable to assume that most of the water has desorbed from the surface held at 150°C or in vacuum. The observed difference in the surface energies corroborates the important role of water molecules in the early phase of hydrophilic bonding.

In comparison, no dependence of the bond strength on the bonding atmosphere was observed in the samples activated with nitrogen or argon gases. Both vacuum and air bonding resulted in strong bonding at 200°C, if argon or nitrogen RIE was used. Hence, the adsorption of the OH groups appears to produce a more stable surface coverage in this case. We simulated the surface sputtering process using the SRIM2000 Monte Carlo code.[7] For 200 eV Ar ions incident on a SiO_2 surface the average sputtering rates for Si and O are 0.041 and 0.227 atoms/ion, respectively. For real surfaces the sputtering yield changes during the ion bombardment due to variations in surface roughness and changes in the stoichiometry. The large relative difference in the atomic sputtering rates nevertheless suggests that the silica surface under Ar bombardment becomes enriched in Si. The hydroxyl groups link to the enriched silicon atoms and constitute a stable hydrated surface. For oxygen plasma exposure the surface remains saturated with oxygen and cannot bind to OH before a light etching step in RCA-1.

We also studied the influence of the plasma activation if only one of the two wafers is activated. The surface energy results for Si/oxide wafer pairs in Fig. 7 show that the activation of the thermal oxide has a larger effect on the bond strength than the activation of

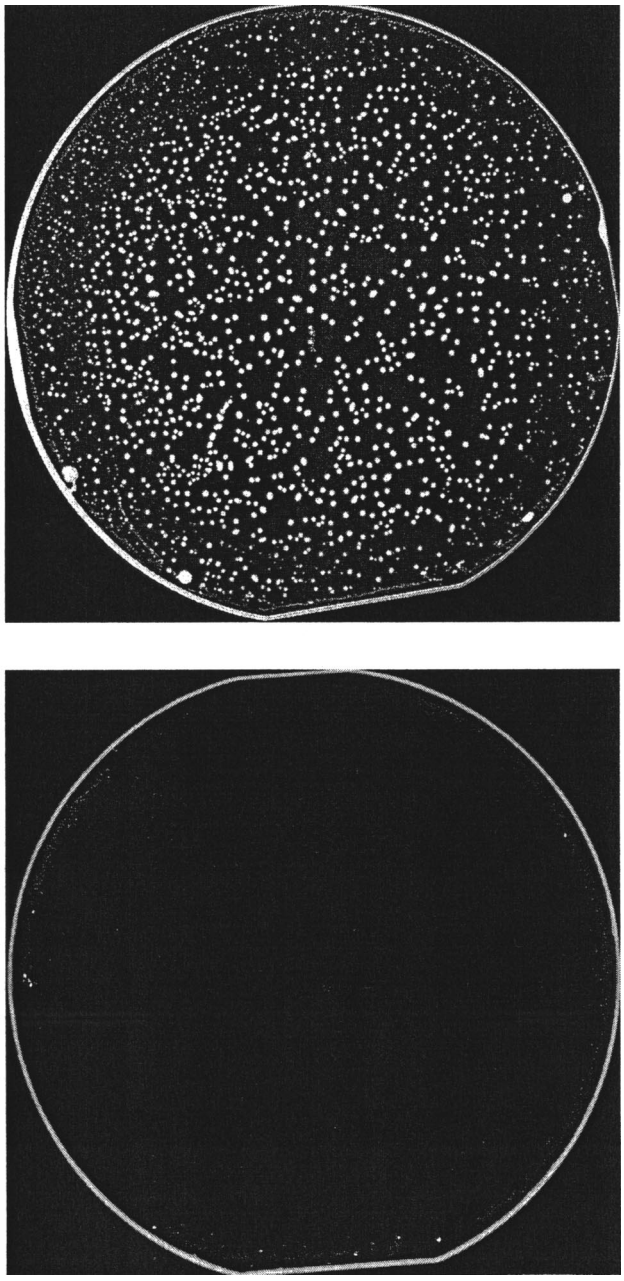

Figure 5. (a) A SAM image of a hydrophilic Si/Si wafer pair. The wafer pair was activated with argon plasma followed with DI water rinse. The bonding was carried out in air with the bond annealing at 200°C for 2 h. (b) A SAM image of Si/oxide wafer pair. The wafer pair was activated with argon plasma followed with DI water rinse. The bonding was carried out in air and the bond annealing at 200°C for 2 h.

the native oxide surface. The same result was obtained both for argon and oxygen plasma. The result can be explained by the varying degree of hydrophilicity of the surfaces. The surface of native oxide can accommodate a higher density of silanol groups compared to the thermal oxide. The density of OH groups on the thermal oxide surface is 0.06/nm^2 whereas the fully hydrated silica surface contains about 4.6 OH groups per nanometer squared.[1] Hence, the reduced density of the bonding sites available on the thermal oxide surface becomes the strength-limiting factor in bonding. The number of bonding sites is increased during the plasma treatment rendering the surface more reactive. The relative amount of this enhancement is more pronounced in the case of the thermal oxide. Figure 7 also shows that after annealing at 200°C, where the majority of Si-OH

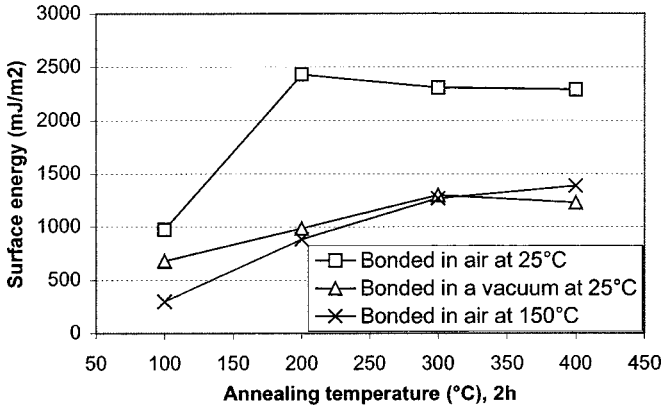

Figure 6. Surface energy as a function of annealing temperature for Si/oxide wafer pairs bonded in different atmospheres. The wafers were bonded after activation in oxygen plasma followed with RCA-1 cleaning.

groups should have reacted to form Si-O-Si bonds, the contributions of the two bonded wafers add almost linearly to the final bond strength.

We also measured the surface energy for argon-plasma-activated and DI water cleaned samples after annealing at 50-300°C for 67 h. The bonding was performed in air. The surface energy of 1200 mJ/m^2 was measured after 50°C, and the surface energy increased linearly as a function of temperature up to 200°C after which the saturated value of 2500 mJ/m^2 was reached. In hydrophilic bonding of Si without plasma treatment the surface energy of >1000 mJ/m^2 is obtained only at 150°C after the interface water has been removed.[1] Our result suggests that the interface water is removed at <50°C if the wafers are exposed to plasma before bonding. We believe that the diffusitivity of the water at the bonded interface is increased due to a highly disordered surface structure induced by plasma activation. After the water has been removed the OH groups can react and form siloxane bridges across the bonded interface. It is well documented that in hydrophilic Si wafer pairs the polymerization of surface Si-OH groups according to Si-OH + Si-OH → Si-O-Si + H_2O increases the bond strength.[1,5] To obtain strong bonding at a low annealing temperature, there should exist a high number of available bonding sites (Si-OH groups) on a wafer surface.[1] We suggest that plasma induces a surface structure, which can accommodate a much higher number of OH groups than the equilibrium density of 4.6/nm^2 reported for silica.[1,10] This equilibrium value corresponds to a surface energy of ~1600 mJ/m^2[1] if we assume that each silanol pair is converted to one siloxane bond. In contrast, the measured surface energy of 2500 mJ/m^2 would require 7.2 siloxane bonds per nanometer squared suggesting a high initial surface coverage by OH ions. Iler has calculated that the surface of fully hydrated silica holds about 7.85 hydroxyl groups per square nanometer. [11] This value is very close to the OH coverage required for surface energies measured in this experiment.

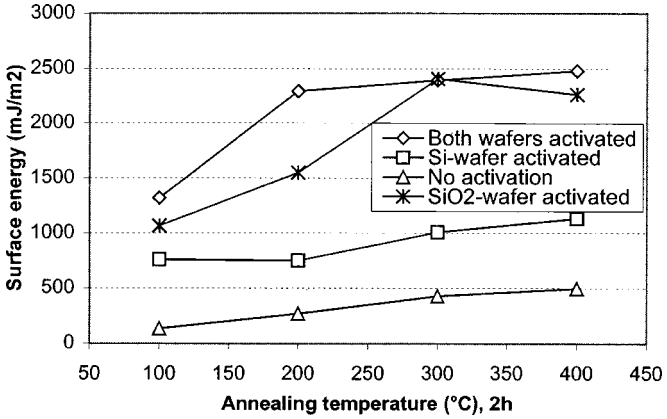

Figure 7. Surface energy of bonded Si/oxide wafer pairs activated by plasma exposure of the Si wafer or the oxide wafer or by exposure of both wafers. The nonactivated wafer pair is given as reference. The activation treatment was a 30 s argon plasma exposure followed with a 5 min DI water cleaning.

Conclusions

Our experiment demonstrates that strong hydrophilic Si-to-thermal-oxide bonds can be obtained at temperatures below 200°C by exposing the wafers to RIE-mode plasma prior to bonding. Both inert and reactive plasma gases result in strong bonding suggesting that the surface activation of hydrophilic Si wafers results from physical modification of the surface layer. This activation is lost under extended treatment in an RCA-1 solution suggesting that the modified surface layer is slowly consumed by chemical etching. Argon or nitrogen plasma activation yields stronger bonds than oxygen plasma, if the bonding is carried out in vacuum. This can be explained by a more stable surface configuration for OH groups on the oxide surface enriched in Si. Because plasma-assisted wafer bonding yields a high surface energy at <100°C, we suggest that the plasma activation creates a surface structure which enhances the escape velocity of water from the bonded interface. The damaged surface layer presumably accommodates a high concentration of OH groups resulting in high bond strength.

Acknowledgments

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PUBLICATION B

Wafer Scale Packaging of MEMS by Using Plasma-Activated Wafer Bonding

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Wafer Scale Packaging of MEMS by Using Plasma-Activated Wafer Bonding

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Plasma-assisted direct bonding has been investigated for wafer scale encapsulation of microelectromechanical systems (MEMS). Direct bonding requires smooth and flat wafer surfaces, which is seldom the case after fabrication of MEMS devices. Therefore, we have used polished chemical vapor deposited oxide as an intermediate bonding layer. The oxide layer is polished prior to bonding the MEMS wafer to cap silicon wafer. The bonding is carried out with plasma-assisted direct wafer bonding at a low temperature (<300°C). Two different methods to form electrical contacts to the encapsulated device are presented. In the first method trenches are etched on the surface of the cap wafer before the bonding. During the bonding the trenches are aligned to the contact pads of the device wafer. After bonding the cap wafer is thinned down with grinding until the path to the contact pads is opened. In the second method one or both of the wafers are thinned down to around 100 μm after bonding. The electrical path to contact pads is formed using V-groove sawing, metal sputtering, and lithography. To test the viability of the developed methods for MEMS encapsulation, we have sealed polysilicon resonator structures at a wafer level.
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The wafer scale packaging process is needed for several reasons in microelectromechanical (MEMS) applications. The packaging cost for MEMS may contribute up to 90% of the total device costs. Wafer scale packaging reduces these costs significantly and may also result in system miniaturization. Moreover, microsystems often contain delicate surface structures which have to be protected from the outside world. Sensor surfaces can be sensitive to particles and chemical contaminants. MEMS devices may also need vacuum or controlled atmosphere for their operation. Typical packaging and assembly tools (such as dicing, solder flux, pick, and place) are not usually compatible with delicate mechanical structures. One way to seal the devices at a wafer level is to bond another wafer to the MEMS wafer. The encapsulation of the devices can take place right after the micromechanical structures are released inside the clean room. The encapsulated (0-level packaged) MEMS wafer can be handled more or less like a normal integrated circuit (IC) wafer.

Various methods for 0-level wafer scale packaging of devices have been reported. Glass frit sealing and anodic bonding are probably the most common methods in 0-level packaging. Both of these methods, however, require relatively high temperatures (400–600°C) and also the required bonding rim around the active device blows up chip size dramatically. This is particularly pronounced in the cases where the chip size is small. Glass frit sealing and anodic bonding involve harmful metals (Pb, Na) that hinder their use in many applications requiring complementary metal-oxide semiconductor (CMOS) compatibility. Agilent uses gold seal bonding to encapsulate their film bulk acoustic resonator (FBAR) devices.[1] Covalent bonding of wafers has also been reported as a wafer scale packaging method.[2]

We have studied the wafer scale packaging of MEMS devices by using a plasma-activation-based, low-temperature direct bonding process.[3] In this method a silicon wafer and an oxidized silicon wafer are exposed to short plasma treatment. Then the wafer surfaces are brought into contact and annealed at 100–300°C. Plasma-assisted bonding has the benefits of low process temperature, inherent cleanliness, high throughput, and also the bonding areas can be small. The main drawback of the method is that in order to achieve good bonding the surfaces have to be very flat and smooth (surface microroughness less than 0.5 nm.). Therefore, we have studied different planarization processes as well as ways to protect the surfaces during subsequent process steps. We also investigated two different methods for forming electrical contacts into the package. To test the feasibility of the developed methods for MEMS packaging, we have encapsulated simple polysilicon resonators.

Experimental

In our experiments 100-mm p-type silicon wafers were used. In the first experiments different conductive paths and pads were fabricated to thermally oxidized device wafers. The conductive layer was made by deposition of molybdenum (sputtering) or in situ boron-doped polysilicon (low-pressure chemical vapor deposition, LPCVD) and subsequent patterning of the conductive layer with standard lithography. The conductive layer was then covered with thick (2-μm) LPCVD-oxide (low-temperature oxide, LTO). The surface steps caused by buried conductive paths were planarized with chemical-mechanical polishing (CMP, Strasbaugh 6DS-SP). For this step special fixed abrasive pads were used. In these pads the abrasive material is fixed into the pad and pH-adjusted water is used to increase the removal rate. A second CMP step was used to smoothen the oxide surface to a level required for fusion bonding. For this conventional oxide final polishing pads and slurry were used.

On some capping wafers we fabricated deep trenches for contact opening. In these cases both sides of the cap wafers were patterned with standard lithography by using Süss mask aligner MA6. Backside alignment marks were needed for aligned bonding. Deep silicon etching was done in a Surface Technology System (STS) inductively coupled plasma chamber (ICP) by using an oxide mask.

The wafers were plasma activated in an STS ICP chamber with 30 s argon plasma treatment. Then the wafer pairs were bonded in Süss MA/BA6 bond aligner. Bonded wafer pairs were heat-treated at 200°C for 2 h to strengthen the bonding. Bond strength was measured from some wafers by using a crack opening method.[4] The thinning of the wafer stack was done with a Strasbaugh 7AF grinding tool. Grinding was also used for contact opening when cap wafers with deeply etched trenches were used. LTO was removed from contact pad surfaces with short hydrofluoric acid (HF) dip. After this the resistance of the buried conductive layer was measured. The above-described process flow is depicted in Fig. 1.

Another way to make the electrical contacts was to saw V-grooves to either one of the wafers. For sawing we used a Loadpoint dicing saw. In these cases molybdenum was sputtered to the sawed grooves to establish electrical contacts with the contact pads. For sputtering we used a Von Ardenne sputter system. This second contact opening process is shown in Fig. 2.

To analyze the surface profile we used Veeco Dektak V200 surface profilometer. Surface roughnesses were measured with a Digital Instruments D3100 atomic force microscope (AFM). The bonding quality and bond alignment accuracy were measured with Sonix

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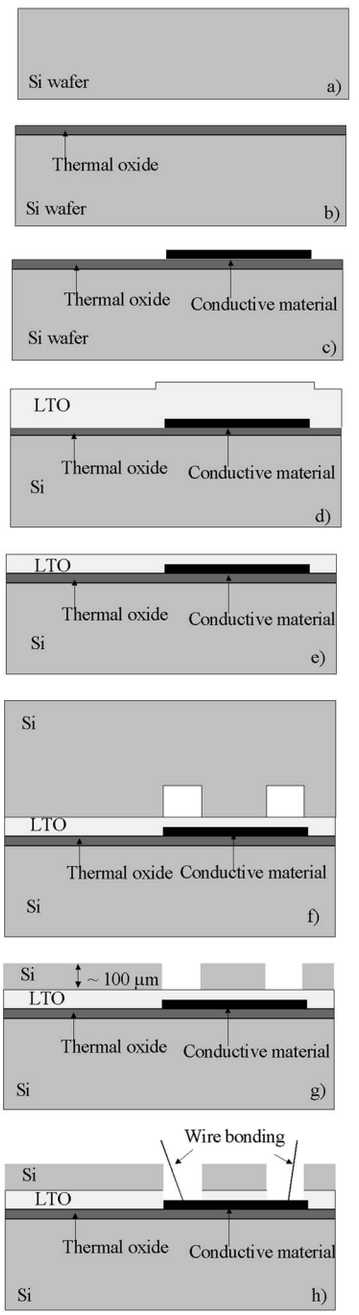

Figure 1. Process flow for buried conductive pads and wires when grinding is used for contact opening: (a) start device silicon wafer, (b) thermal oxidation of the device wafer, (c) deposition and patterning of conductive material (doped polysilicon or molybdenum) on device wafer surface, (d) covering of conductive material with thick LPCVD-oxide layer, (e) oxide surface planarization and smoothening with CMP, (f) aligned bonding of patterned cap wafer to the device wafer, (g) cap wafer thinning and contact hole opening with grinding, and (h) etching of oxide from contact holes and probing or wire bonding.

UHR2000 scanning acoustic microscope (SAM). Scanning electron microscopy (SEM) was used for closer examination of packages from cross-sectional samples.

To test all these process steps in one process flow we fabricated a simple polysilicon resonator and encapsulated it.

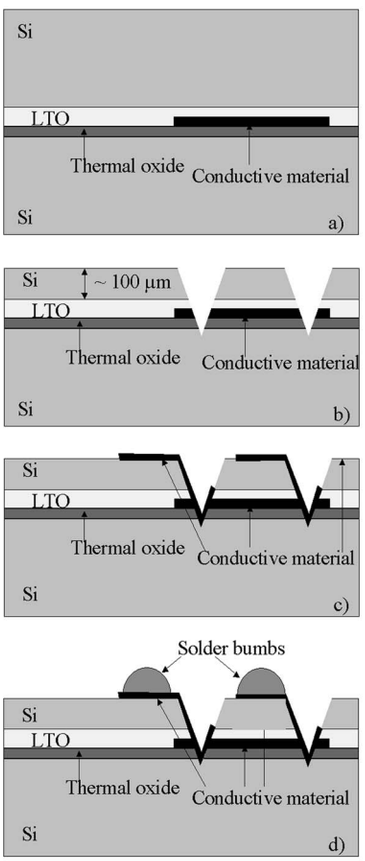

Figure 2. Contact opening by sawing: (a) the device wafer is bonded to the cap wafer, (b) grinding down one of the wafers and sawing of V-grooves, (c) deposition and patterning of molybdenum layer, and (d) growth of solder bumbs.

Results and Discussion

Bonding of LPCVD-oxide differs from bonding of thermal oxide. LPCVD-oxide has to be polished and usually outgassing will take place if bond annealing exceeds oxide growth temperature. The outgassing can be avoided by either using high-temperature annealing prior to bonding or by using a low-temperature bonding process. High-temperature annealing is not usually an acceptable process step because of temperature-sensitive materials or devices on the wafer. Therefore, we have used plasma-activation-based, low-temperature bonding in our process.[3] Figure 3 shows the measured

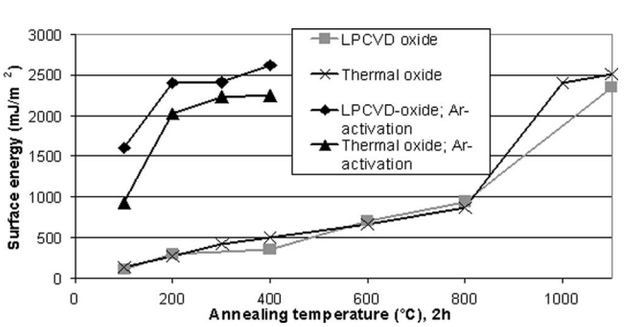

Figure 3. Measured surface energies for thermal oxide to Si and for LPCVD-oxide to Si wafer pairs bonded with and without plasma activation. Bond annealing time was 2 h.

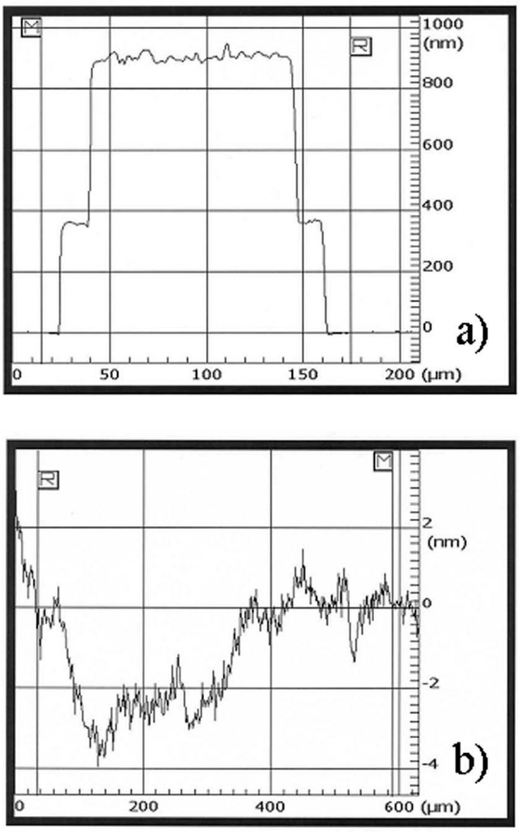

Figure 4. Measured surface profile of the resonator wafer (a) before and (b) after the planarization.

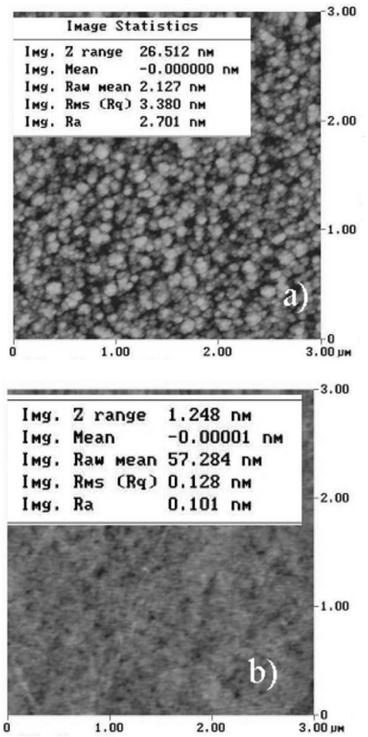

Figure 5. AFM image of resonator wafer (a) before and (b) after CMP steps.

surface energies for low-temperature and high-temperature-bonded LPCVD-oxide and for thermal oxide.

The first tests had patterned conductive layers on top of thermal oxide on the device wafer. When the conductive layers were covered with LPCVD-oxide (LTO), the buried material caused surface steps to the oxide. These steps had to be removed with planarization. Figure 4 shows the profile of the oxide layer on top of buried structure (a) before and (b) after CMP. Before CMP the surface step height was 800–1000 nm. After CMP the step could not be observed with surface profilometry. The total removal needed to planarize 800-nm-thick oxide hills was less than 1000 nm, indicating good planarization capability of our CMP process. Typically oxide planarization processes need removal of oxide layer at least twice the hill height.[5,6] After the first CMP step the surface roughness [root-mean-square (rms)] was reduced from as-grown value of 3.38 nm (Fig. 5a) to 0.273 nm. During the second CMP step, the surface roughness (rms) reduced to 0.128 nm (Fig. 5b).

After the planarization the device wafers were bonded to the cap wafers with trenches using a plasma-assisted bonding process. The bonding was spontaneous and no voids could be observed after annealing of the wafer pairs at 100–300°C (Fig. 6). In Fig. 6 the dark areas represent buried conductive material and white areas trenches on the cap wafer.

We also tested the possibility of removing first the surface steps by lithography and buffered hydrofluoric acid (BHF) etching and then carrying out the polishing process. The problem with this process is usually rounding of the corners of oxide walls or pillars (Fig. 7a and b) during the polishing process. By adjusting the polishing force and slurry flow the rounding effect decreased but could still be noticed (Fig. 7c). However, we managed to develop a CMP process so that even small pillars ($\sim$50 µm) could be polished without significant edge rounding effect (Fig. 7d) by using fixed abrasive pads. The surface roughness on top of the pillars was reduced from about 3 nm to below 0.3 nm. Figure 8 shows the bonding result of a 200-µm-wide LPCVD-oxide wall pattern bonded to a blank silicon wafer. The polished oxide rim area around the cavities is well bonded and void-free.

We used two different approaches for making the electrical contact to the contact pads between the wafers. The first one was to have deep etched wells on the cap wafer, which were aligned to pad positions during bonding (Fig. 6). When the cap wafer was ground down an access to the contact pad was formed. The electrical probing proved that the electricity flowed well through the buried conductive layer from pad to pad. With large pads and small final cap wafer thickness the final connection can be made with wire bonding, for example. The process is shown in Fig. 1.

Another studied approach for contact formation was to use sawing for contact opening. We used a dicing blade for cutting a

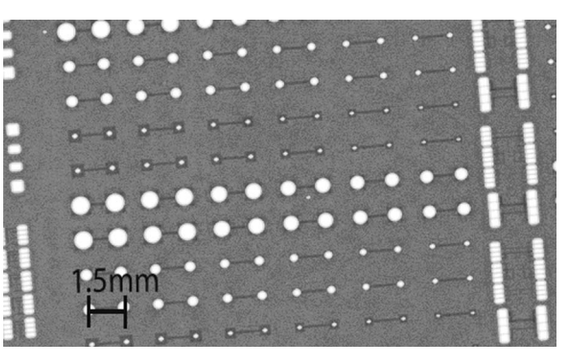

Figure 6. SAM image of wafer with buried conductive structures bonded to a patterned cap wafer. Conductive material is seen in the image as dark areas and cavities are seen as white areas.

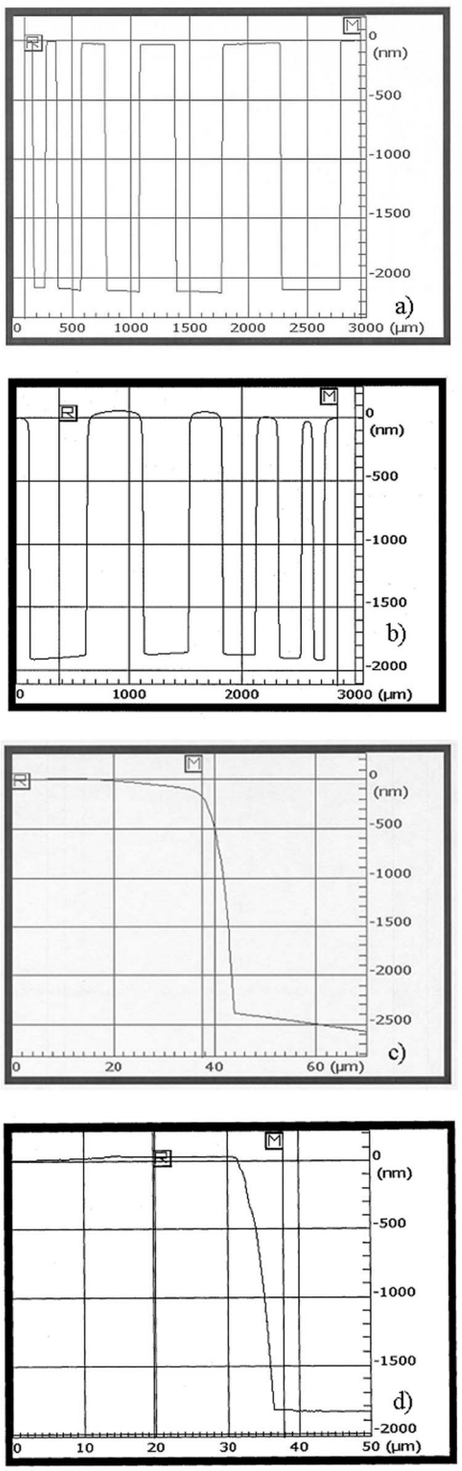

Figure 7. Surface profiles of LPCVD-oxide pillars (a) before CMP, (b) after normal oxide polishing process, (c) after modified oxide polishing (low-force, high-slurry flow), and (d) after the special CMP process.

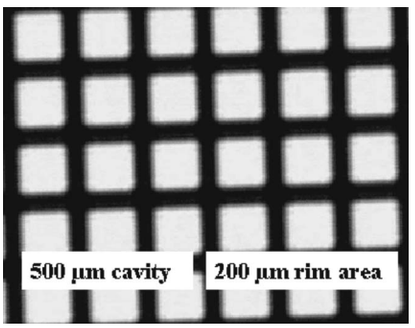

Figure 8. A SAM image of patterned and polished LPCVD oxide bonded to blank silicon wafer.

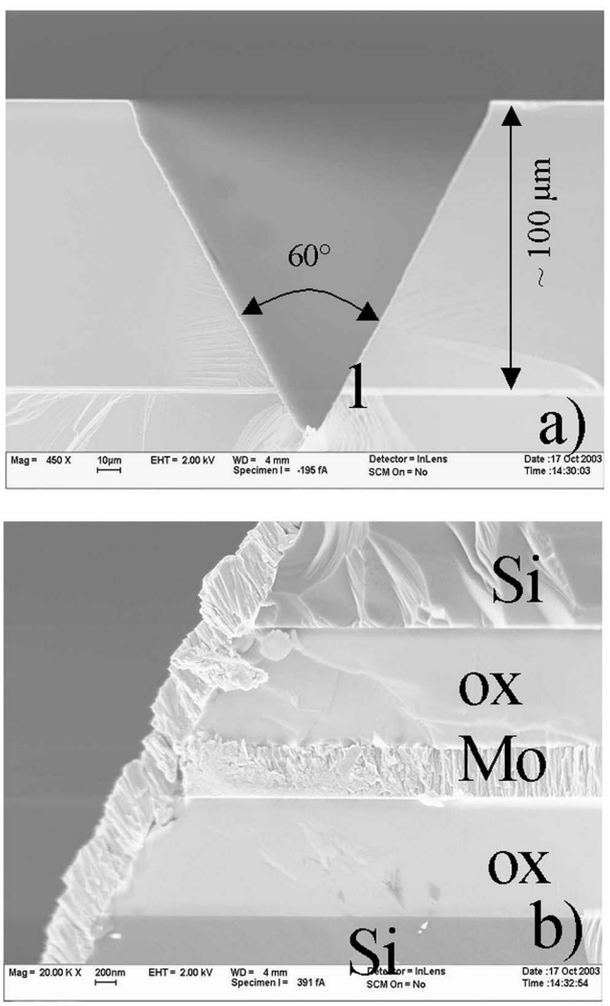

Figure 9. (a) SEM image of a V-groove sawed to the cap wafer. The groove goes about 20 μm into the device wafer. (b) Close-up from point 1 in Fig. 8a. Molybdenum in the V-groove is in contact with molybdenum between the oxide layers.

V-groove through the cap wafer and contact pads (Fig. 9a). The V-groove can also be made from the device wafer side. After sawing a molybdenum layer was sputtered onto the V-grooved surface. The molybdenum made an electrical contact with the buried conductor

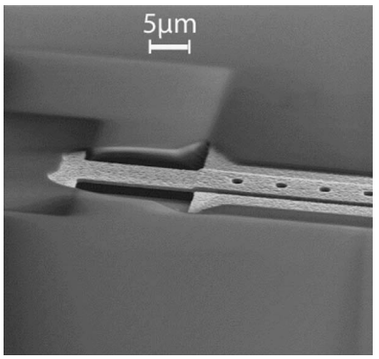

Figure 10. SEM image of released polysilicon resonator.

material, enabling a buried lateral electrical path to be formed (Fig. 9b). Then the molybdenum was patterned so that the only path between the two pads was a line going inside the bonded wafer stack. We found out that the molybdenum can be patterned even inside the groove with standard lithography, if a thick resist mask is used and if the groove is kept relatively shallow (<150 μm). Therefore, it is recommended that the wafer where the grooves are to be placed is thinned before sawing. Afterward the molybdenum is patterned to desired shapes, e.g., solder bumbs can be fabricated on it and used to connect the protected component to the next level package. This process is depicted in Fig. 2. The problem with groove-sawing a contact opening is that first the components and the contact pads have to be placed in the wafer so that sawing of one groove cuts through several pads but does not harm devices or cut-off the connector lines. Both silicon wafers should be high-resistivity wafers to avoid short cutting via Si. Good things with this process are that the cap wafer do not have to be deep-etched on contact pad areas (less lithography and etching, more bonded area) and contacts can be made to either the handle or the cap wafer. Sawing is a cost-effective process compared to, e.g., dry etching, if the pads can be placed in rows.

When probing the electrical properties of these two types of connections, both had resistivity of the same order of magnitude. However, with the sawing process there was sometimes a problem with oxidation of buried molybdenum, which increased the contact resistance between buried Mo and Mo in V-groove significantly. This problem was removed by using short HF-dip and sputtering etching before sputtering Mo to the V-groove. Further investigations are on their way to measure the exact values of resistivity and to test the repeatability of our processes.

One problem with our wafer scale packaging process is that the surfaces to be bonded have to remain really smooth, even though it is sometimes necessary to do several processing steps after the final

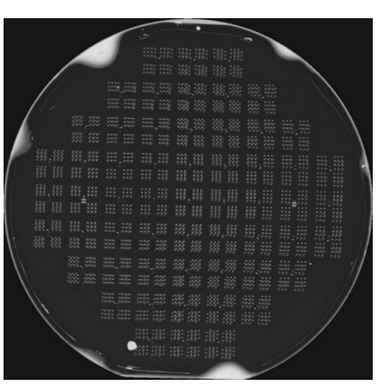

Figure 11. An SAM image of encapsulated resonators.

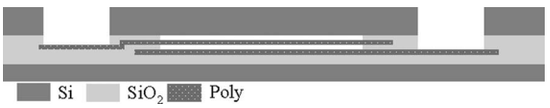

Figure 12. Schematic image of the encapsulated resonator.

polishing steps. Therefore, we tested different materials as protective layers for areas to be bonded. The best result was obtained by using sputtered molybdenum as a protective layer. This layer was resistant to HF during oxide patterning and was later on easily removed with mild SC-1 cleaning (H_2O_2:NH_3:H_2O). The surface roughness of the protected areas remained the same as before processing. If buffered hydrofluoric acid (BHF) is used for oxide etching, a good protective layer is standard photoresist.

Both protective layers were tested on resonator packaging. A simple polysilicon resonator was covered with LPCVD-oxide. After oxide planarization and smoothening the areas to be bonded were protected with molybdenum or photoresist, depending on if HF or BHF was used for release etching. The critical step after release etching is drying. If normal drying is used the resonator structures break or stick due to surface tension of the liquids. Therefore we used supercritical carbon dioxide drying. An SEM image of a released resonator is presented in Fig. 10. After the release etching the protective layer was removed and the device wafer and the cap wafer were plasma activated and bonded together. An SAM image of a bonded wafer pair is presented in Fig. 11. The bonding result was good, although wafer pairs had some voids due to particles. The cap wafer was subsequently thinned down to open the contacts to resonator pads. A schematic image of the final package is shown in Fig. 12. The resonator properties were not optimized, because the goal was just to test the packaging concept with an actual device structure.

Conclusions

In our experiments we have shown that plasma-assisted direct bonding is a usable method for wafer scale MEMS packaging, if care is taken in surface preparation and protection. Covering of the device with LPCVD oxide and using it as an intermediate bonding layer was found to be a viable method for encapsulation. By using a special CMP polishing process, surface steps can be removed and surface roughness reduces to a level required for fusion bonding. If device fabrication steps are needed after CMP, the roughening of the surface has to be prevented with a protective layer.

We have also tested two different methods to fabricate electrical contacts to the package. Both methods, opening of pre-etched trenches on the cap wafer by grinding as well as a V-groove sawing method, facilitated an electrical path from the encapsulated device to the outside world.

Acknowledgments

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PUBLICATION C

Silicon-on-Insulator Wafers with Buried Cavities

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Silicon-on-Insulator Wafers with Buried Cavities

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Direct bonding and mechanical thinning of pre-etched silicon wafers have been studied for the fabrication of silicon-on-insulator (SOI) wafers with buried cavities. The thin Si diaphragm over the cavity is deflected downward during the grinding and polishing, as the thinning is carried out without supporting the diaphragm. The deflection causes thickness variation for the Si diaphragm that can also be observed as a hill on the wafer surface after thinning. The results show that the thickness variation of the Si diaphragm increases with increasing cavity size and with decreasing SOI layer thickness. After grinding the measured hill height was about 1.5 μm for a 20-μm-thick Si diaphragm over a 1 × 1 mm cavity. The hill height was reduced to less than 0.5 μm when a small supporting column was placed under the diaphragm. With polishing the hill height was further reduced to <0.1 μm. It appears that mechanical thinning of the bonded wafers with pre-etched cavities is a viable method for various applications.
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In silicon microelectromechanical system (MEMS) technology the prominent techniques currently in use are bulk and surface micromachining. Silicon-on-insulator (SOI) MEMS is a complementary micromachining technology which has several advantages over bulk and surface micromechanics. Nevertheless, it also has some limitations, such as the gap between the released mechanical structure and the substrate cannot be freely adjusted but is limited to the thickness of the buried thermal oxide used as a sacrificial layer. The need for protection of the metal layers during hydrofluoric acid (HF) release etching of the sacrificial oxide may also cause process complications. Bonded substrates with pre-etched cavities would provide freedom to the design of MEMS structures and solve some of the restrictions to the use of SOI for microsystems. It might also be useful in fabrication of 3D structures containing several wafer-bonded layers. After bonding the device/cap wafer can be thinned down mechanically and/or chemically to the desired device layer thickness, resulting a Si diaphragm over the cavity.[1-3] Subsequently, these diaphragms can be released with dry etching, avoiding the problems due to HF etching. In pre-etched SOI wafers the cavity dimensions are well-defined because they are lithographically patterned prior to the bonding. Moreover, the parasitic capacitance between the device layer and the substrate can be decreased far below what is achievable with a buried oxide layer in conventional SOI wafers if deep cavities and small bonding areas are prepared on a wafer. Also, the pressure inside the cavity can be adjusted by using suitable bonding ambient. Overall, pre-etched SOI wafers would be a suitable platform for vertically and horizontally moving structures in various applications, such as capacitive inertial sensors, pressure sensors, microphones, and microfludic devices. Bonding of patterned wafers enables double-side processing of the SOI layer and in principal, a wafer with pre-etched cavities would be transparent to complementary metal oxide semiconductor (CMOS) processes.

We have studied direct bonding and mechanical thinning of patterned Si wafers for the fabrication of thick-film SOI wafers with pre-etched cavities. The viability of grinding and chemical mechanical polishing (CMP) for silicon diaphragm fabrication has been investigated. The main objective of the work is to gain design rules for the buried cavities and mechanical thinning.

Experimental

A typical process flow for pre-etched SOI wafers is depicted in Fig. 1. The process is basically similar to a standard thick-film SOI wafer manufacturing process that is based on direct wafer bonding and mechanical thinning of the device layer. The difference is the fabrication of cavities on the handle wafer or the device wafer or even both prior to the bonding. In addition to the processing tools found in a typical wafer-manufacturing factory, some lithography equipment is needed. At the beginning of the process the cavities are prepared on a handle wafer using standard wet or dry etching techniques. Next, the etched handle wafer is bonded to another wafer, and subsequently the Si diaphragms are thinned with surface grinding and polishing (CMP).

In this work, ⟨100⟩-oriented 100-mm, p-type Si wafers were used for prepatterned SOI fabrication. The handle wafers were thermally oxidized either before or after the cavity etching. Wells with various sizes and shapes were formed on the handle wafers using standard lithography and wet and/or dry etching. The wells were etched to thermal oxide and/or to silicon. Thermal oxide was etched in buffered hydrofluoric acid (BHF) at room temperature. Wet etching of silicon was carried out in tetramethylammonium hydroxide (TMAH) at 80°C, and inductively coupled plasma (ICP) etching was used for the dry etching of silicon. Oxide and/or photoresist masking layers were used during the etching of silicon cavities. In some cases the cavity wafers were reoxidized in order to form oxide layer on the bottom and walls of the cavity (cavity oxidation). This reoxidation step was carried out after the oxide mask layer was removed with HF.

After cavity fabrication and buried oxide formation the handle wafers were bonded to the cap wafers with direct bonding. The bonding (wafer contacting) was carried out in vacuum (pressure $<10^{-2}$ mbar) or in air with commercially available wafer bonder (EVG801). Subsequently, the wafer pairs were annealed at 1100°C to increase the bonding strength. After bonding the cap wafer was thinned down by grinding and CMP. The grinding was conducted on a Strasbaugh model 7AF wafer backgrinder using a diamond cup coarse and fine wheels. The used fine grinding wheels were no. 2000 mesh (ca. diamond size 3–6 μm) or finer resin bonded diamond wheels. The grinding process was not optimized for cavity wafers, but a process that yielded a smooth surface and a thin subsurface damage layer was applied. This kind of processes is typically used in SOI wafer manufacturing, because short polishing process and a good wafer uniformity can be obtained. The polishing was carried out with a commercial CMP tool (Strasbaugh 6DS-SP) using standard polishing pads and slurries for silicon.

The bonding quality was evaluated with scanning acoustic microscopy (SAM), cross-sectional scanning electron microscopy (SEM) samples, and HF etching (50% HF, 10 min) of the buried oxide.[4] Prior to the bonding some of the cavity wafers were studied with atomic force microscopy (AFM) to see how the cavity preparation influences the surface roughness. In addition, the profiles of the cavity edges were investigated with SEM and surface profilom-

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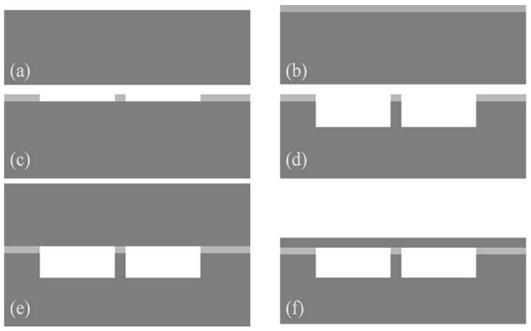

Figure 1. A typical process flow for SOI substrates with pre-etched cavities starts with a silicon handle wafer (a), which is thermally oxidized (b). The next step is patterning and etching of oxide (c) and silicon (d). After cavity formation the handle wafer is bonded to the cap wafer (e). Subsequent process steps are grinding and polishing down to a required Si diaphragm thickness (f).

etry (Veeco Dektak V-200). After thinning of the bonded wafer pairs the deflection and thickness of the Si diaphragms were measured with surface profilometry and SEM, respectively.

Results

In Fig. 2 SAM images of patterned bonded wafer pairs with square cavities are shown. Prior to the bonding the cavities were formed on thermally oxidized handle wafers using BHF etching. The width of cavity and pitch were varied on different wafers to change the overall bonded fraction. For wafers with large bonded areas the bonding occurred as expected. However, SAM measurements taken after air bonding and annealing at 1100°C showed voids at the bonded interface when the bonding area was small as compared to the total wafer surface area. For example, when the cavity width was 500 μm and the pitch 555 μm (bonded rim area 55 μm), corresponding to a cavity fraction of over 80%, wafer bonding in air resulted in a large void while wafers bonded in vacuum showed no voids. Voids with same size and shape were found from all similarly prepared air bonded samples, only location of the void varied. We assume that this is due to the pressure increase in the cavity during the high-temperature annealing. If the bonding area is sufficiently small, the pressure in shallow (in this case 2 μm) cavities may lead to the formation of voids. The wafer pairs with smaller cavity fractions, that is larger bonding area, had no voids irrespective of the bonding ambient.

The bond strength of patterned bonded wafers was measured by using the HF etching method.[4] In this test the buried oxide of the SOI wafer is etched with 50% HF for 10 min and the etched distance of the buried oxide is measured from the bonded interface with cross-sectional SEM. The etch rate has a relation with the bond strength: a faster etch rate means a weaker bond, as has been found for the bonded unpatterned wafer pairs.[4] After annealing of the patterned bonded wafer pairs at 1100°C the etched distance of buried oxide was 15–18 μm in vacuum-bonded samples, whereas an etched distance of 25–30 μm was measured for air-bonded samples. The result suggests that bonding in vacuum yields somewhat higher bond strength than air bonding.

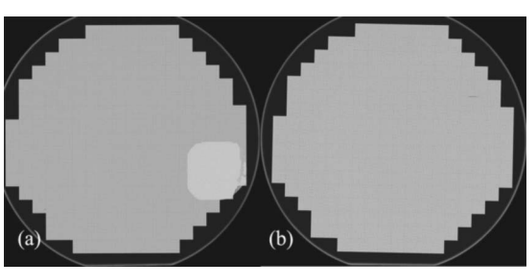

Figure 2. SAM images of prepatterned, bonded wafer pairs with 0.5 × 0.5 mm cavities. The width of the bonding rim area around the cavities is 55 μm. The bonding was carried out in either air (a) or in vacuum (b).

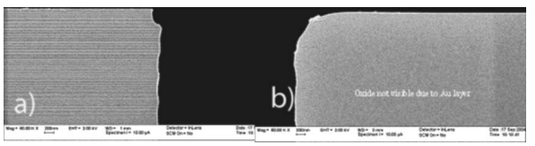

Figure 3. Cross-sectional SEM images of edges of the plasma etched Si cavities before (a) and after (b) thermal oxidation. The oxide layer (thickness 500 nm) is not visible in Fig. 3b, because a thin gold layer was evaporated on the sample for better image quality.

In some cases it would be desirable to cover the walls and bottom of the cavities with oxide layer. This can be accomplished by thermal oxidation, which is carried out after cavity formation. However, thermal oxidation of etched wafers may cause poor bonding because of pattern-dependent oxidation rate. Figure 3 presents SEM images of edges of the cavities before and after thermal oxidation. It is well documented that convex and concave corners on Si cause oxide thinning.[5] This stress-dependent oxidation causes rounding of the etched cavity corner (Fig. 3b). Surface profilometry revealed that the oxide surface is also slightly elevated near the edge of the cavity (Fig. 4). The height and width of this elevated area (bump) are typically 5–20 nm and a few micrometers, respectively. According to Tong and Gösele,[3] the gap closing can occur at the bonded interface if the condition $h < 3.5(R\gamma/E')^{1/2}$ is fulfilled, where h is height of the bump, R is the lateral extension of the gap, γ is surface energy at room temperature (0.1 J/m^2 for oxide–silicon bonding), and $E' = E/(1 - \nu^2)$, where E and ν are Young's modulus and the Poisson ratio, respectively. Based on this equation, the gap closing should not occur with typical bump dimensions. However, we could not detect any unbonded area with SAM measurements. This might be due to insufficient resolution of SAM. In order to study the bonding quality of oxidized cavity wafers, we thinned down the bonded handle wafers with oxidized cavities using backgrinding and anisotropic plasma etching. The thinning was continued until the etched cavities were reached. Figure 5 shows an SEM image of a etched column located inside the cavity after removing the handle wafer. Because the column survived the grinding and etching processes, it appears that at least the center area of the column is bonded to the handle wafer regardless of stress effects at the cavity edge. Anyway, the stress effects in oxidation have to be taken into account when one is performing thermal oxidation for cavity structures prior to the bonding.

To study the relation between the lateral dimension of the cavity, SOI layer thickness, and thickness variation of the Si diaphragms over the cavities, we ground and polished bonded wafers with pre-etched cavities of various size. After thinning the total thickness variation, convexity or concavity of Si diaphragms were measured. Figure 6 presents the measured total thickness variation of Si diaphragms as a function of average SOI-layer thickness for the various cavity sizes. The values were obtained from rectangular cavities. The length of the cavities was 10 mm and the width varied from 250 to 750 μm. It appears that the thickness variation of the Si diaphragm over the cavity increases with increasing lateral dimension of the cavity and with decreasing SOI layer thickness. The thickness of the Si diaphragm is largest at the center of the cavity and decreases toward the edge of the cavity. The result is similar to the data, which have been published by Prochaska et al.[1] With surface profilometry this thickness variation can also be observed as a hill on the Si film over the cavity (Fig. 7). The magnitude of hill height

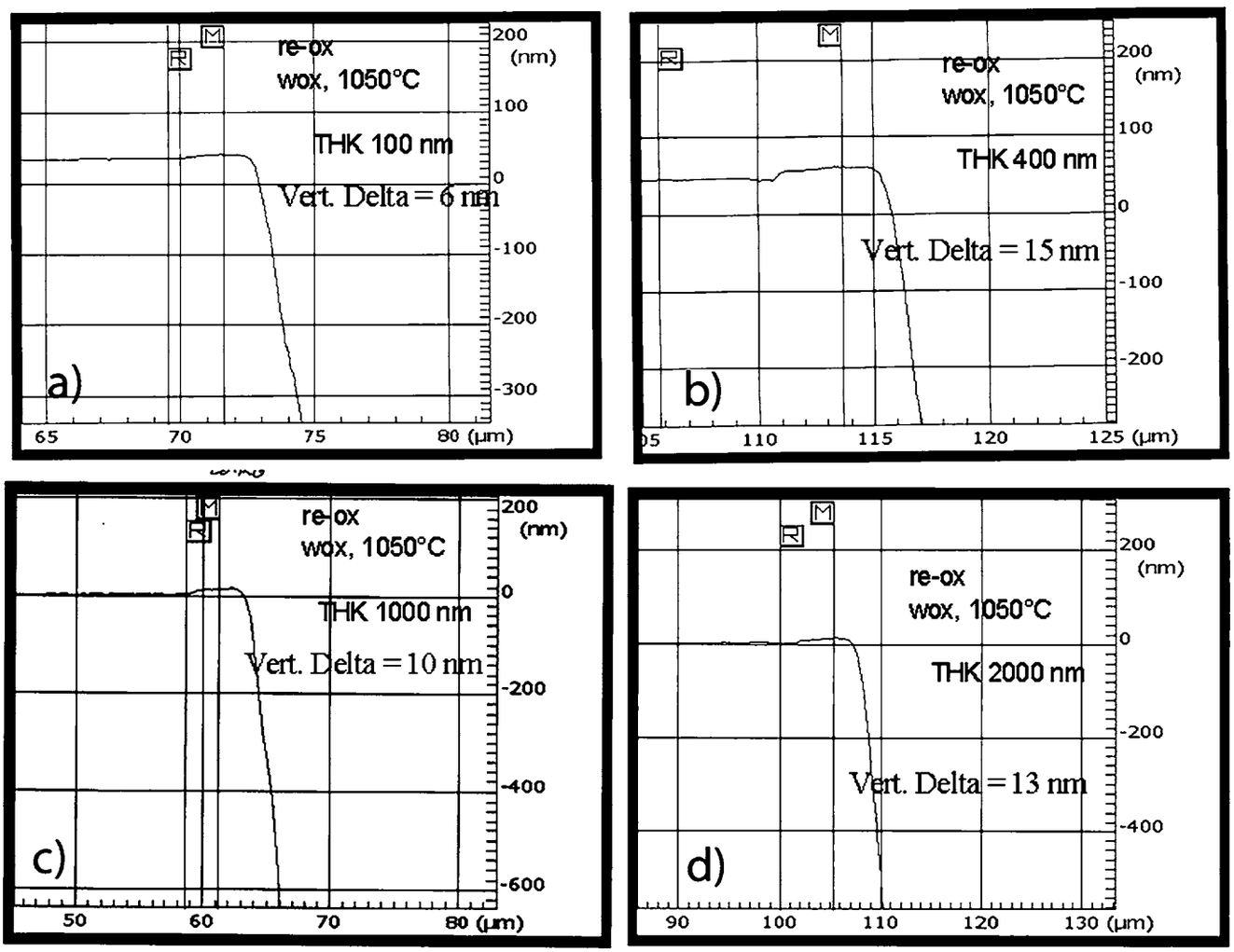

Figure 4. Surface profilometry on the edges of TMAH-etched Si cavities which were thermally wet oxidized at 1050°C after cavity formation. The thicknesses of the oxide layer are (a) 100, (b) 400, (c) 1000, and (d) 2000 nm.

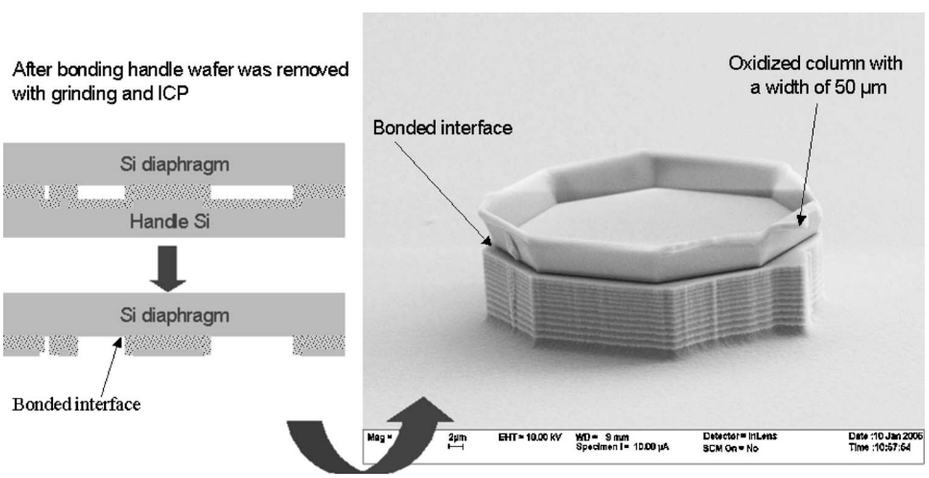

Figure 5. SEM image of an oxidized bonded column inside the cavity after removing the handle wafer with grinding and plasma etching. The width of the column is 50 μm.

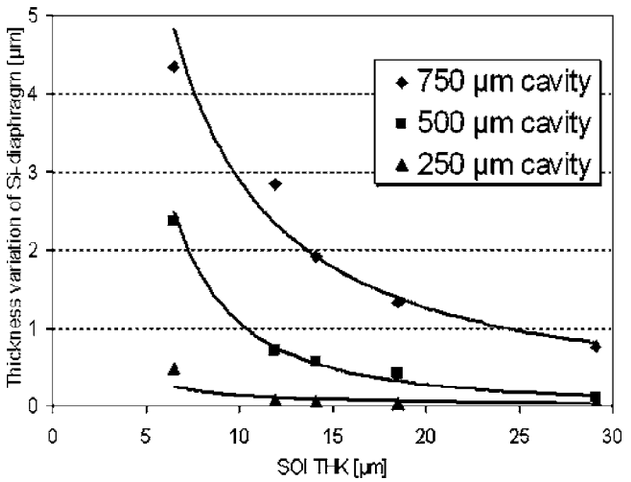

Figure 6. Measured thickness variation (TTV) for thinned (grinding + CMP) Si diaphragms as a function of average SOI-layer thickness for various cavity sizes. The cavities were etched on SiO_2/Si with BHF and ICP plasma etching. The length of the cavities are 10 mm, and the cavity depth is 50 µm. The widths for the cavities are 250, 500, and 750 µm. The wafer pairs were bonded in vacuum.

depends on the thickness of the diaphragm and its location on the wafer. Larger hill height was observed for the cavities at the wafer edges than at the wafer center. Concave bending was measured for a 6-µm SOI film over a cavity with a width of 500 µm. This is caused by the pressure difference between the inside and outside of the cavity that deflects the diaphragm downward.

It appears that the grinding and polishing forces bend the Si diaphragm downward during the thinning process, leading to nonuniform Si membrane thickness. The bending occurs due to increasing flexibility of Si film toward the center of film (cavity) and because of lack of support under the film. The thickness variation and integrity of the Si diaphragm can be improved by using support structures under the silicon diaphragm. Figure 8 depicts the influence of support structures on the surface profile of the Si diaphragm after grinding. All profiles were convex, because the vacuum inside the cavities was not able to deflect the membranes with the used cavity dimensions. For an unsupported cavity the hill height was

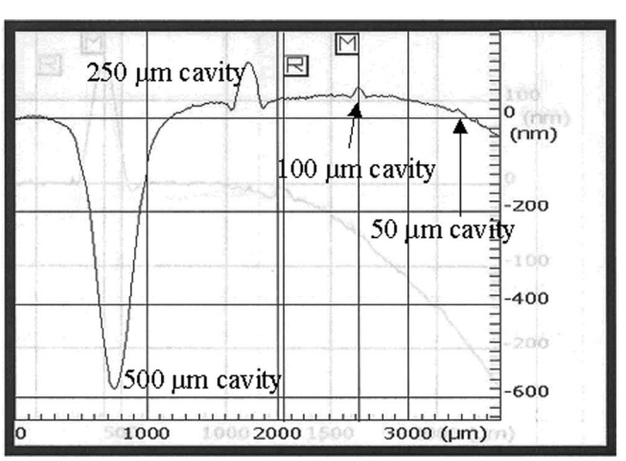

Figure 7. Surface profilometry on thinned (grinding + CMP) Si diaphragms over similar rectangular cavities as in Fig. 6. Scanning direction is perpendicular to the long side of the cavity. The thickness of the SOI layer is about 6 µm. The measured deflections are −600, 80, and 30 nm for 500, 250, and 100 µm diaphragms, respectively. The wafer pairs were bonded in vacuum.

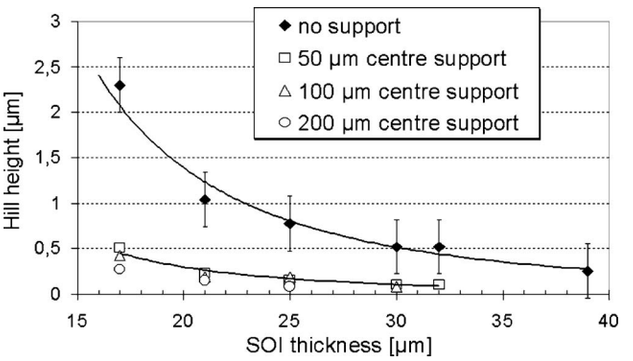

Figure 8. Measured hill heights for the Si diaphragms over 1 × 1 mm cavities with and without support columns. The depths of cavities were around 5 µm. No CMP was carried out, but the values were measured after grinding. The support square columns were located at the center of the cavity. The sizes for the columns were 50, 100, and 200 µm. The wafer pairs were bonded in vacuum.

about 1.5 µm after grinding with a SOI layer thickness of 20 µm. Figure 8 indicates that if a center support column is placed under the silicon diaphragm the hill height is about four times lower than the values observed for unsupported diaphragms. As the wafers were polished the measured hill heights were less than 0.1 µm for SOI thicknesses over 20 µm. Figure 9 presents 3D surface profiles of 2 × 2 mm cavities with a simple column support and four column supports inside the cavity. The measurements were carried out after grinding the diaphragms to a thickness of 23 µm. The measured hill height was about 1.9 µm for the diaphragm with four 50-µm column supports and about 0.6 µm for the diaphragm with a 800-µm

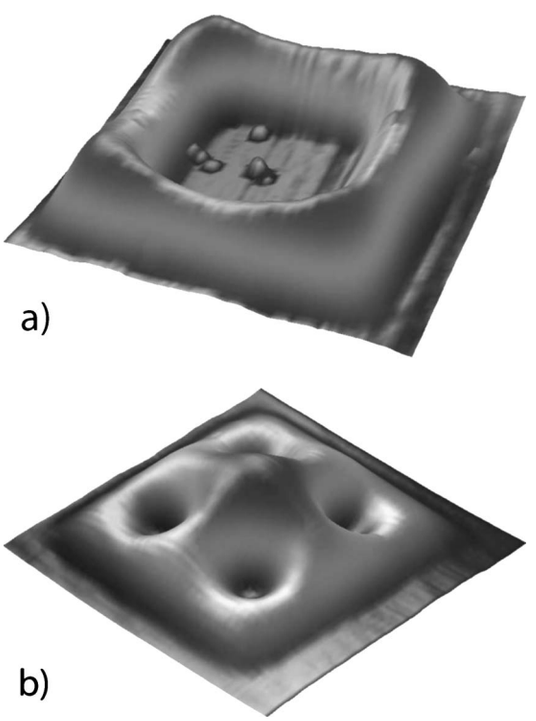

Figure 9. Measured 3D surface profiles of ground Si film over a 2 × 2 mm cavity with a 800-µm center column (a) and with four 50-µm columns under the diaphragm (b). The thickness of the SOI layer is 23 µm. The measured maximum hill heights are 0.6 and 1.9 µm for (a) and (b), respectively.

center column support. This suggests that the hill height and the thickness variation of the silicon diaphragms are largely determined by the dimensions of the unsupported film area.

Conclusions

Mechanical thinning of pre-etched and bonded silicon wafers is a viable method for fabrication of SOI substrates with buried cavities. SOI with pre-etched cavities may solve some of the problems inherent to conventional SOI MEMS technology. The grinding and CMP induce forces on the Si diaphragms over the etched cavities during the thinning of the bonded wafer pairs with cavities. This leads to thickness variation and hill formation on the surface of a Si diaphragm. The hill height was found to decrease during the polishing process. The integrity of the diaphragm can be significantly improved with various support structures. The results suggest that grinding and polishing can be utilized in buried cavity fabrication for various MEMS applications.

Acknowledgments

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PUBLICATION D

Characterization of Bonded Interface by HF Etching Method

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CHARACTERIZATION OF BONDED INTERFACE BY HF ETCHING METHOD

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ABSTRACT

Directly bonded interfaces have been studied using a HF etching method. Bonded wafer pairs were dipped into 50% hydrofluoric acid (HF) solution for 10 minutes and subsequently the etched distance was measured from cross-sectional samples by scanning electron microscopy (SEM). Studied wafer pairs were silicon/oxide, oxide/oxide, silicon/glass, oxide/glass and silicon/quartz wafer pairs. In silicon/oxide and oxide/oxide bonds a relationship was found between the surface energy measured with the crack opening method and the etched distance. In silicon/glass and oxide/glass bonding we found the etch rate of the bonded interface to decrease with increasing bond annealing temperature.

INTRODUCTION

SOI (silicon-on-insulator) wafers have replaced the conventional silicon wafers in many electrical and sensor applications. SOI wafers are available with different buried oxide (BOX) and SOI-layer thicknesses. The strength of the bonded interface is usually measured with the crack opening method [1]. However, the use of the crack opening method is rather difficult in cases when one or both of the bonded materials are fragile such as glass or thin wafers, since in these cases the blade insertion usually leads to wafer breakage instead of crack formation. Another limitation is that the blade needs to have a place for insertion, e.g. opening between two rounded wafers. Therefore, the surface energy is measurable only from the areas near the wafer edges. The crack opening method has also problems in measuring strong bonded interfaces [2]. In the sensor applications, where structures are released by etching of buried oxide layer, it is important to have a well-defined etch rate and good knowledge about formed oxide wall profile. The objective of this work was to find a new method for bond strength determination especially suitable for fragile substrates.

EXPERIMENTAL

In the experiments we used <100> oriented 100 mm p-type Czochralski grown silicon wafers, 100 mm Corning 1737F glass wafers and 100 mm fused quartz wafers. Thermal wet oxide was grown on some of the silicon wafers. Some of the wafers were activated in a reactive ion etcher (Electrotech RIE) using argon or oxygen plasma. After

plasma activation the wafers were cleaned in 70°C SC-1 (NH_3:H_2O_2:H_2O) solution and/or in deionized water. Wafers were bonded in a commercially available wafer bonder (Electronic Visions EV801). The bonded wafer pairs were annealed for 2 hours at 100°C. After this wafers were cut into 1 cm thick stripes with a dicing saw. The stripes were annealed at various temperatures to achieve bonds with different bond strengths. For comparison, some of the stripes were used to measure the surface energy with the crack opening method [1]. The samples were dipped in a 50% HF solution for 10 minutes. Subsequently, the samples were cleaned in deionized water and dried. The etched distance was measured from the cross-sectional samples by using scanning electron microscopy (SEM).

RESULTS

A logarithmic relation between the surface energy and the etched distance was found for silicon/oxide and oxide/oxide bonds (Fig. 1). For strongest bonds, the etched distance was ~15 μm and the etched oxide profile was almost straight (Fig. 2), showing that the etch rate was nearly uniform across the oxide. For weak bonds, the oxide profile shows that etch rate is higher at the bonded interface than on the other parts of the buried oxide (Fig. 3).

We also performed the HF etch experiments for plasma-activated silicon/oxide bonds. The etch rate versus measured surface energy curve shown in Figure 4 differs significantly from the one obtained for silicon to oxide bonds formed without plasma activation. The etched distance in a plasma activated sample annealed at 200°C was from 80 μm to 100 μm depending on the activation procedure and the measured surface energy was ~2400 mJ/m^2. Etched distance in silicon/oxide wafer pair bonded without plasma activation having similar bond strength was about ~15 μm. Higher etch rate in the plasma activated samples may be due to porous or damaged layer formed into the oxide surface during plasma activation. The layer affected by the plasma ions is found to be about 5nm thick and it is quickly consumed during SC-1 cleaning [3].

In thermal oxide to glass bonding we measured the length of the notch (Fig. 5) formed during etching. The length decreased with increasing annealing temperature (Fig.6). Due to the fragility of the glass wafer, the applicability of the crack opening method was limited to weak bonds. The measured surface energy for oxygen plasma activated oxide to glass bonding annealed at 200°C for 2 hours was ~680 mJ/m^2.

We investigated the suitability of HF etching method also in silicon to quartz bonding. To avoid debonding due to the mismatch in thermal expansion coefficients [4], we used oxygen plasma followed with SC-1 cleaning to achieve strong bonding at the annealing temperature of 200°C. The crack opening method was again not applicable for bond strength measurement, because of the fragility of the quartz wafer. The etched distance was ~126 μm (Fig.7), which is close to the etched distances measured for similarly prepared silicon/oxide wafer pairs (~100μm). Since the etch rate for quartz glass and thermal oxide in HF are comparable, this result suggests strong bonding between quartz and silicon.

CONCLUSIONS

Etching in hydrofluoric acid is a promising method to measure the bond strength in cases where the crack opening method cannot be used. This method enables bond quality measurements from bonded fragile wafers, ready-made SOI and diced chips. The HF etching method can also be used to create bond strength maps over the wafer area. Limitations for the method are that at least one of the materials at the interface must be attackable by the HF and the etch rate is not only dependent on the surface energy, but also on the sacrificial material properties and possible interfacial voids.

We have shown a relation between the etch rate and the surface energy in conventional silicon to oxide and oxide to oxide bonding. By using plasma activation, high surface energies can be obtained for silicon/oxide bonds at annealing temperatures below 200°C. However, the etch rate of the buried oxide for the plasma activated wafer pairs is much higher than for non-activated silicon/oxide bonds having similar surface energy values. We believe that this difference in the etch rates is due to the porous or damaged layer at the plasma activated surface.

The method was also studied for silicon to glass, oxide to glass and silicon to quartz bonds. In silicon to glass and oxide to glass bonding, the HF formed a notch near the bonded interface. The length of the notch was found decrease with increasing annealing temperature.

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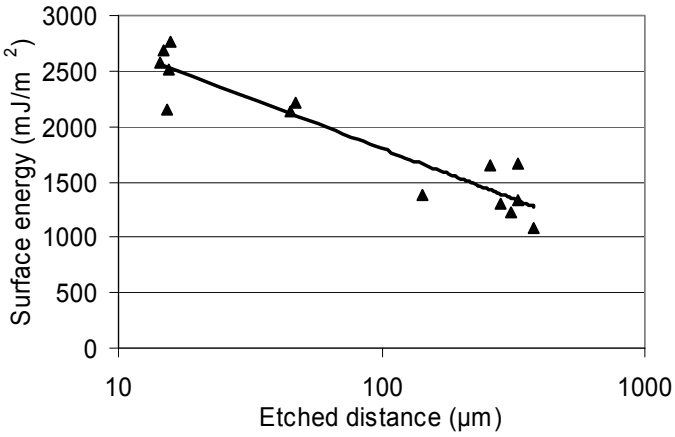

Figure 1. The measured surface energy as a function of the measured etched distance for the bonded SOI structures. The etching was carried out for 10 min in 50% HF at room temperature. No plasma activation was used.

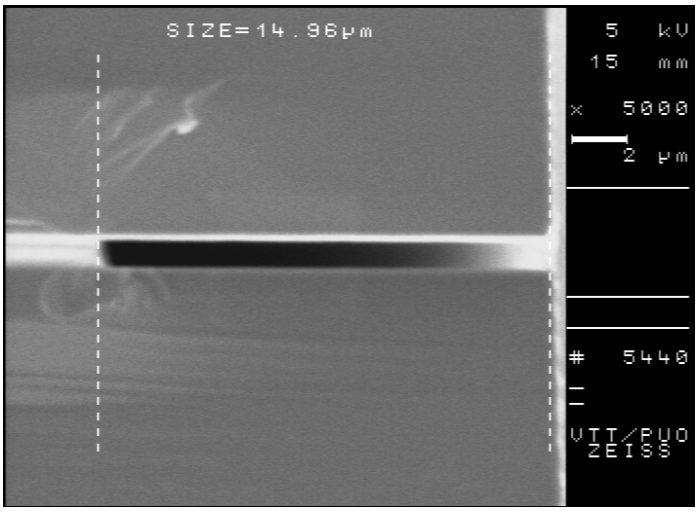

Figure 2. SEM image of bonded silicon to 1µm thermal oxide wafer pair. Annealing was done at 1100°C. The etched distance is ~15 µm. Surface energy was found to be ~2600mJ/m^2.

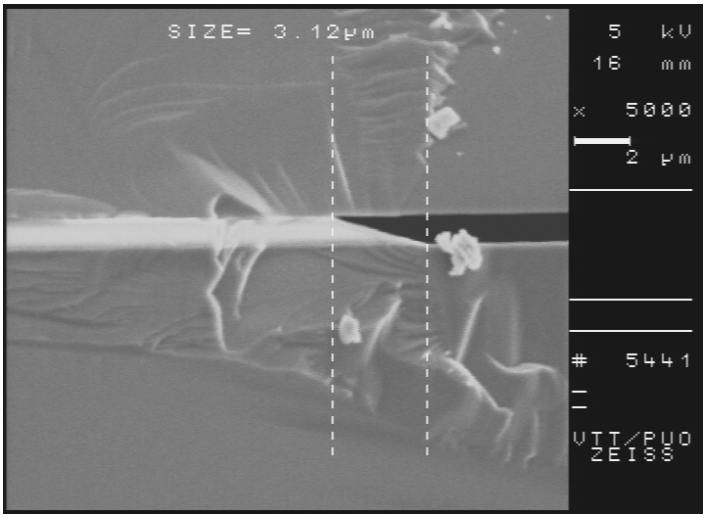

Figure 3. Profile of the etched oxide wall on 50nm oxide (top) to 1000nm oxide (bottom) bond annealed at 1150°C. Total etched distance was ~50µm and surface energy was ~2200mJ/m^2.

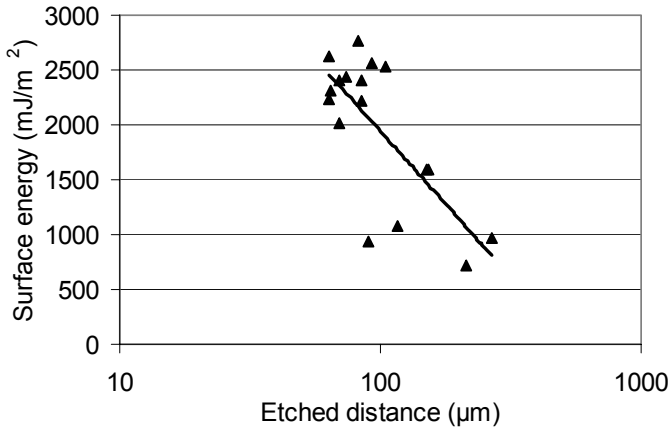

Figure 4. The measured surface energy as a function of the measured etched distance for plasma-activated and bonded SOI structures. The etching was done for 10 min in 50% HF.

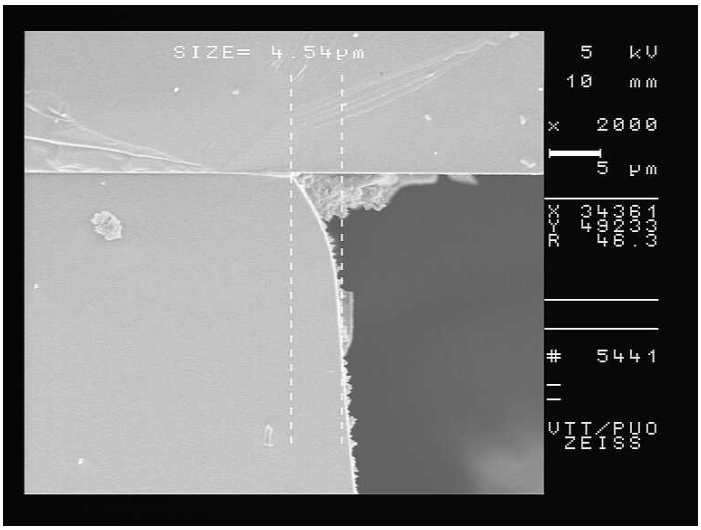

Figure 5. SEM image of the notch in the plasma activated 100nm thermal oxide (top) to glass (bottom) bond. The bond annealing temperature was 500°C. The notch was created by etching the sample for 10 min in 50% HF. The length of the notch is ~4.5 µm.

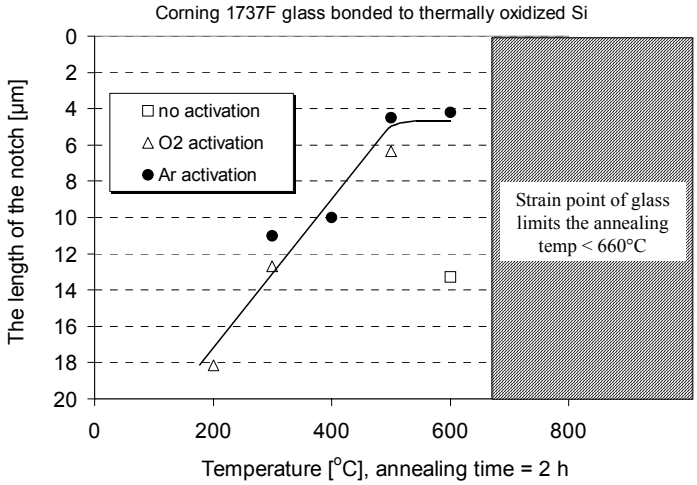

Figure 6. Measured length of the notch as a function of annealing temperature for 100nm thermal oxide to glass bonding with and without plasma activation.

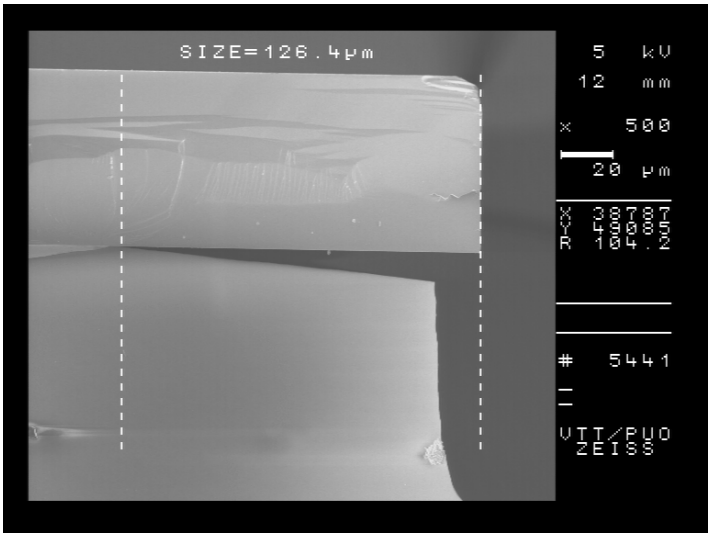

Figure 7. SEM image of bonded silicon (top) / quartz (bottom) wafer pair. Wafers were activated in oxygen plasma followed with SC-1 cleaning. Bond annealing was carried out at 200°C. The etched distance is ~125 µm.

PUBLICATION E

Mechanical Delamination for the Materials Integration

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MECHANICAL DELAMINATION FOR THE MATERIALS INTEGRATION

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ABSTRACT

Mechanical exfoliation process in hydrogen implanted and bonded Si and the mechanical delamination method have been studied. Thin Si layers have been transferred from the temporary holder wafers to sapphire wafers using controlled direct wafer bonding and mechanical debonding. Helium ion-channeling measurements show that the silicon film on sapphire is crystalline in nature. We have also investigated the effect of the surface roughness on the bond strenght in SiO_2 to SiO_2 direct bonding. Prior to the bonding the wafer surfaces were modified using CHF_3 plasma etching. With a combination of surface roughening and activation treatments the surface energy of the bonded interface can be tailored to 500-1200 mJ/m^2 at temperature range of 200-1100°C. We suggest that controlled wafer bonding in combination with the delamination techniques could enable the fabrication of multilayer substrates and 3D-devices.

INTRODUCTION

Wafer bonding and various layer transfer techniques such as the ion-cutting of Si are becoming important processes in the microelectronics and microsystems industry [1]. Layer transfer by hydrogen implantation and wafer bonding can be realized by mechanical or thermal means [2,3]. Mechanical splitting of the implanted and bonded wafer pair can be performed under 300°C, whereas the thermal exfoliation process typically requires annealing at > 300°C [4, 2]. Conventionally, wafer-bonding research has targeted to obtain strongest possible bonds by using high temperature annealing step or plasma exposure or other surface activation procedure [1]. However, temporary bonded wafer pairs with intermediate bond strength of 500-1500 mJ/m^2 would be desirable in some applications. For example, the crystalline damage due to the hydrogen implantation in ion-cut Si layers could be removed by high temperature annealing before transferring the Si film onto temperature sensitive substrates. The controlled wafer bonding would also permit the mechanical delamination and transfer of processed thin layers to another substrate. To fully utilize the potential of this method, a bonding process yielding intermediate surface energy even after high temperature processing should be found. The mechanical transfer process itself could be performed near or at room temperature without generating excessive stresses due to the difference in thermal expansion coefficient. Fully processed wafers can be thinned down to 20-150 μm using mechanical grinding and etching. However, controlled wafer bonding in combination with ion-cutting could result in wafer scale processed thin films in the thickness range of 0.1-1.5 μm. In principle the delamination of the temporary bonded and processed layers would enable fabrication of integrated materials and 3-dimensionally packed devices.

The objective of this work was to study the mechanical exfoliation process in hydrogen implanted Si and to survey the possibility of transferring thin layers of Si onto another substrate using the controlled wafer bonding and the mechanical delamination methods. In order to form a mechanically debondable substrate we modified the surface topography of the wafers prior to the bonding. The influence of surface roughness on the bonding behaviour was evaluated by measuring the bond strength and the voids at the bonded interface.

EXPERIMENTAL

In the experiments, <100> oriented p-type Czochralski grown silicon and r-cut <1120> oriented sapphire wafers with a diameter of 100 mm were used. The resistivity of the Si wafers was 1-10 ohm-cm. A thermal wet oxide layer with a thickness of 500 nm was grown at 1050°C on some of the Si wafers to be used for hydrophilic Si to SiO_2 bonding (oxide/Si bonds) and SiO_2 to SiO_2 bonding (oxide/oxide bonds). Plasma enhanced CVD-silicon oxide layer was deposited on sapphire wafers to suppress the formation of interfacial voids during the bonding. Prior to the bonding the deposited oxide layer was smoothened with chemical-mechanical polishing (CMP).

For the implantation induced exfoliation experiments, the donor Si wafers were implanted with H_2^+ at 100 keV to a dose of 4.5×10^{16} H_2 / cm^2. Some of the donor wafers were also implanted with B^+ at 175 keV with a dose of 3×10^{15} B/cm^2 either before or after the hydrogen implantation. No thermal annealing was used to activate the implanted boron. The implanted donor wafers were subsequently bonded to oxidized handle Si wafers using plasma enhanced bonding process resulting in a surface energy of >2000 mJ/m^2 at 200°C [5]. The implanted and bonded wafer pairs were annealed in two steps: first 2 hours at 100°C and then 2 hours at 180-400°C. After annealing the surface energy of the H-implanted layer was measured using the crack opening method in air [1].

In order to form a substrate, which could be debonded even after high temperature processing, we studied the influence of the surface roughness on the bond strength of oxide/oxide bonds. The thermal oxide surfaces were modified (roughened) before the bonding using CHF_3 plasma etching in parallel plate RIE-reactor (Electrotech). During etching the plasma power was 100-250 W, and the etching time varied from 5s to 1 min. After the roughening treatments the wafers were cleaned in a SC-1 (NH_3:H_2O_2:H_2O) solution and DI-water. A short oxygen plasma exposure and subsequent DI-water cleaning was used for the activation of the surfaces prior to the bonding. Bonding was performed in air, and subsequently the wafer pairs were annealed at 200-1100°C for 2 hours.

The surface energies of the bonded interface and the H-implanted layer were measured from sliced rectangular samples using the crack opening method [1]. Debonding and layer transfer experiments were carried out by inserting a thin blade between the bonded wafers for the initiation of the crack. The bonded wafer pairs were

inspected for interfacial voids using IR transmission imaging and scanning acoustic microscopy (Sonix UHR2000). The surface roughness of the samples was measured with a Digital Instrument D3100 atomic force microscope (AFM) using silicon tips in the tapping mode. The crystalline quality of the thin Si film on sapphire was evaluated by using 2 MeV ^{4}He ions with channeled Rutherford backscattering method. The scattering angle was 160° in the channeling measurements.

RESULTS AND DISCUSSION

Figure 1 shows the surface energy of the bonded interface and the H-implanted layer. The wafers were exposed to oxygen plasma prior to the bonding. The basic condition for the exfoliation process is that the bonded interface is stronger than the hydrogen implanted layer. The surface energy of 2500 mJ/m^2 can be obtained for the thermal oxide to hydrophilic Si bonds at 200-250°C if a proper plasma activation procedure prior to the bonding is used. When a certain critical temperature is exceeded the strength of the H-implanted layer drops below 2500 mJ/m^2 enabling mechanical layer transfer, whereas thermal exfoliation calls for somewhat higher temperatures. The temperature required for exfoliation depends on the crystal orientation, boron doping level and implanted hydrogen dose. Boron doping and implantation prior to the hydrogen implantation reduce the strength of the H-implanted layer. Similar lowering in exfoliation temperature is observed in B-implanted but not activated and B-doped epitaxially grown layers. If boron is implanted after hydrogen, higher temperatures are needed for the exfoliation (Fig. 1). In order to determine the effects of boron doping in exfoliation, elastic recoil detection analysis (ERDA) and ion channeling measurements are underway in our laboratory. Thickness of the mechanically transferred Si layer is predetermined by the damage zone induced by the implantation. As the wafers are delaminated the cleavage occurs through the damage zone yielding a very uniform and smooth Si layer on top of handle wafer. Total thickness variation of the mechanically transferred layer given by optical reflectometry is typically around 2 nm. AFM-measurements yield a surface roughness of around 3 nm for the transferred Si layer.

The key to the mechanical layer transfer is good control of the bond strength. If we fabricate a SOI-structure with intermediate bond strength of 500-1500 mJ/m^2, the SOI-layer could be transferred to another substrate using mechanically induced delamination. To test this idea of controlled wafer bonding and subsequent mechanical separation of wafers we bonded thermally oxidized Si to unoxidized Si wafers at 800°C resulting in a bond strength of about 1000 mJ/m^2. The wafer pairs were thinned to a SOI-layer thickness of 15 μm using grinding and polishing processes. The finished SOI-structures were bonded either to oxidized Si or sapphire wafer using low temperature oxygen plasma assisted bonding yielding a surface energy of >1500 mJ/m^2 [5]. Subsequently, the wafer pairs were separated using a thin blade for the crack initiation. Since the surface energy of the first bonded interface was lower than that of the second, thick SOI-layers were transferred from the temporary holder wafer to another substrate (Fig. 2a). We also prepared thin film SOI-structures using thermal ion-cutting process.

The exfoliation of the bonded wafer pairs was carried out at 500°C. After splitting the ion-cut SOI-wafers were polished and bonded to oxidized Si or sapphire wafers. Also in this case the bonding was carried out using the plasma-assisted process. The silicon-on-sapphire (SOS) wafer with a transferred thin Si-layer is presented in Fig. 2b. With normal thermal ion-cutting the fabrication of silicon-on-sapphire structures is difficult because of the large difference in thermal expansion coefficient [1]. However, in our experiments the bond between the debondable SOI-substrate and sapphire was formed at 120°C without generating excessive stresses. Figure 3 shows the $^4He^+$ ion-channeling spectrum of the thin film SOS-structure. For comparison a spectrum in random condition and a spectrum of a virgin sample are also presented. The ion-channeling results suggest that there is a very low amount of lattice damage in the Si layer. This damage due to the hydrogen implantation could be removed by annealing at high temperature. Figure 4 shows the AFM-image of the transferred SOS-layer. The measured surface roughness was around 0.1 nm indicating than no polishing is needed after separation of the wafers.

Our experiments show that both thin and thick Si films can be transferred onto another substrate using controlled wafer bonding and mechanical delamination. It appears that during the mechanical separation of wafers the crack propagates along the weakest interface without derailing to other interfaces provided that there is a sufficient difference in the interface strengths. To fully utilize the technique, it is necessary to find bonding processes for engineering or limiting the bond strength to prescribed level. The initial bonding between hydrophilic Si wafer surfaces is caused by hydrogen bonds [1]. Because of the short-range nature of hydrogen bonds, the bonding is sensitive to surface roughness. In order to control the bond strength we modified the surface topography of the thermally oxidized Si wafers using plasma etching. Figure 5 shows AFM images for untreated reference SiO_2 and plasma etched SiO_2. Plasma etching in RIE-mode induced texture with 30-100 nm wavelengths on the surface. The influence of the surface roughness on the bond strength in SiO_2 to SiO_2 bonding is illustrated in Fig. 6. The wafers were cleaned with SC-1 solution just before the bonding in air, and no plasma activation was used. After annealing at 1100°C a surface energy of 700 mJ/m^2 is measured for the samples etched in CHF_3 plasma prior to the bonding as compared to the strength of > 2000 mJ/m^2, which was obtained for the reference sample. The result is consistent with those reported by Roberts [6]. No macroscopic voids were detected for the plasma-etched samples. This kind of approach could be used to make debondable substrates with mechanically thinned SOI-layers. However, the strength of the bonded interface is too low for preparing ion-cut thin SOI-layers, since thermal exfoliation at 300-600°C requires surface energy of about 500 mJ/m^2 [2].

To further adjust the bonding energy we exposed the roughened surfaces to oxygen plasma before the bonding. The measured surface energies for the etched and plasma activated samples are depicted in Fig. 7. If plasma activation is used strong bonding is obtained at 200°C even though the SiO_2 surfaces were pre-roughened by dry-etching. This could be caused by the decrease in surface roughness due to the short oxygen plasma exposure. We tried to verify this with AFM, but were not able to obtain reliable roughness values probably because of plasma induced surface charging. High bond strength obtained for pre-roughened activated samples could also result from the increase in the initial bonding force leading to the enhanced formation of Si-O-Si covalent bonds. When smooth (non-etched) plasma activated SiO_2 is bonded to dry-

etched non-activated SiO_2 the surface energy is between 500 and 1200 mJ/m^2 in the temperature range of 200-1100°C. This surface energy range enables thermal ion-cutting as well as the debonding after high temperature annealing. Scanning acoustic microscopy measurements showed that there are no macroscopic voids in the samples (Fig. 8). We believe that plasma exposure increases the number of OH-groups resulting in increased surface energy at low temperatures. This is supported by the contact angle measurements, which were carried out after plasma exposure. Plasma-activated and DI-water cleaned SiO_2 surfaces showed a very hydrophilic behaviour, and the contact angle of DI-water dropplet on surface was so low (<5°) that it could not be measured. As the wafers are contacted the area over which the bonding really occurs is limited when the surfaces are rough. We believe that this limits the surface energy to 1500 mJ/m^2 even at high temperatures.

Based on the results, we suggest that with well-adjusted surface modification and activation treatments one could achieve useful debondable substrates. We used a thin solid wedge for the delamination of the wafers but more reliable delamination methods such as gas or fluid wedges may also be used [3]. In addition, the other surface of the bonded wafer pair could be clamped to a vacuum chuck for better cleaving action if one of the wafers is fragile.

CONCLUSIONS

When the bonded wafers are separated with mechanical splitting forces, the crack propagates through the weakest interface. Our result show that controlled wafer bonding and mechanical delamination method enable near room temperature fabrication of integrated substrates such as silicon-on-sapphire (SOS). Surface topography modification is an effective approach to control the bond strength in direct wafer bonding. We suggest than controlled direct wafer bonding can be used for the fabrication of debondable substrates for 3D-integrated devices.

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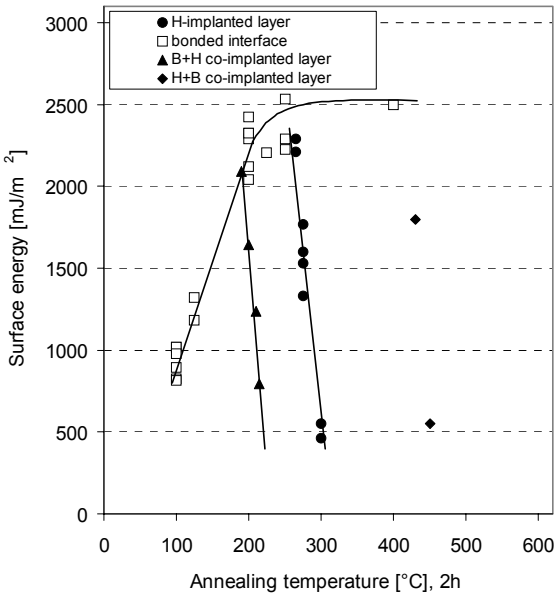

Fig. 1 Measured surface energies for the bonded interface, H-implanted layer and the boron and hydrogen co-implanted layer. Hydrogen was implanted with H_2^+ at 100 keV with a dose of 4.5 x 10^{16} cm^{-2}. Boron was implanted with B^+ at 175 keV with a dose of 3 x 10^{15} cm^{-2} either before (B+H) or after the hydrogen implantation (H+B). The annealing time was 2 hours.

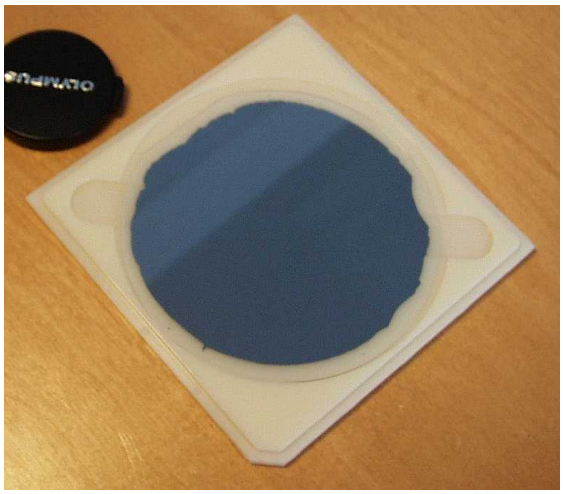

Fig. 2a Photograph of 100 mm thick film SOS-wafer fabricated by mechanically releasing the SOI-layer from temporary substrate to a sapphire wafer. Thickness of the Si film is 15 µm.

Fig. 2b Photograph of 100 mm thin film SOS-wafer fabricated by mechanically releasing the SOI-layer from temporary substrate to a sapphire wafer. Thickness of the Si film is 410 nm.

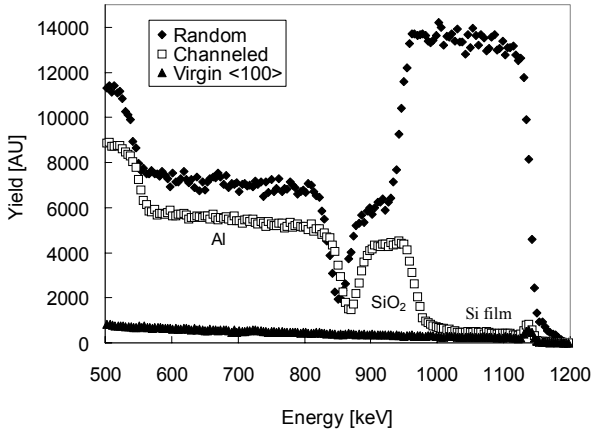

Fig.3 RBS-channeling spectrum of the transferred thin Si layer on top of sapphire substrate. The random and virgin spectra are shown as a reference. Silicon film and intermediate SiO_2 layer thicknesses given by scattering measurement are 410 and 130 nm respectively.

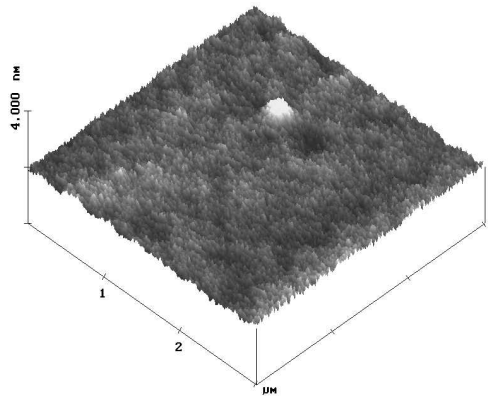

Fig. 4 AFM image of debonded and transferred thin Si layer on a sapphire wafer. The surface roughness is about 0.1 nm.

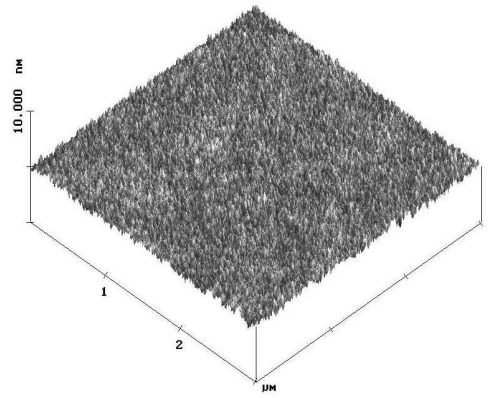

Fig. 5a AFM-image of as-grown thermal SiO_2 surface. The RMS- roughness is ~ 0.2 nm.

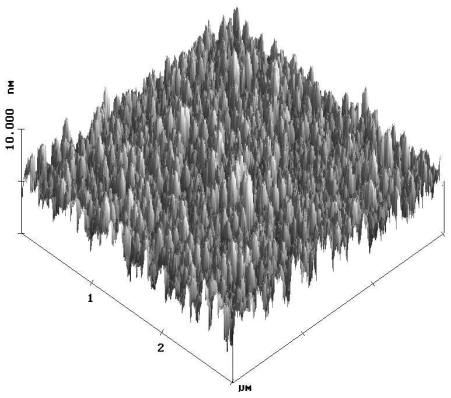

Fig. 5b AFM-image of SiO_2 surface etched in CHF_3 plasma for 30s. The RMS-roughness is 0.8 nm.

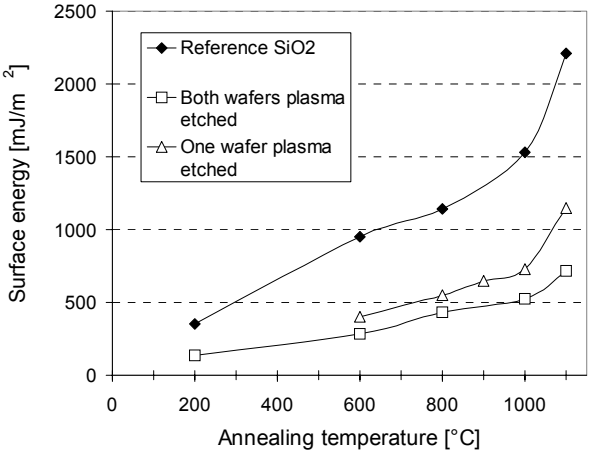

Fig. 6 Measured surface energies for SiO_2 to SiO_2 bonds. The surfaces were etched for 30s in CHF_3 plasma prior to the bonding. The untreated reference sample is shown for comparison. The bond annealing time was 2 hours.

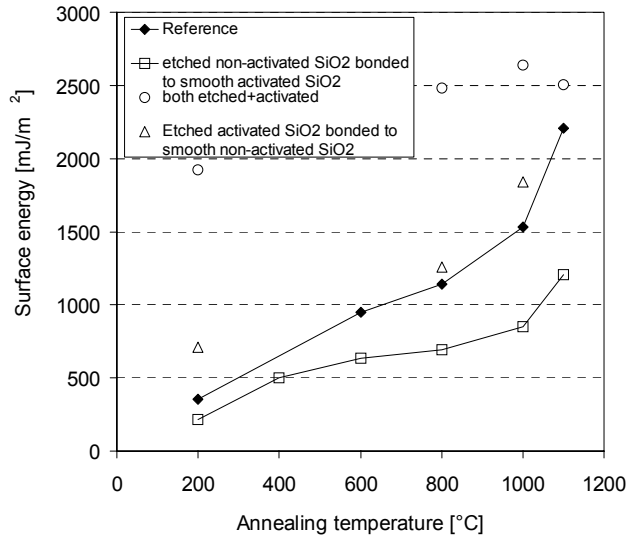

Fig. 7 Measured surface energies for the plasma etched and activated SiO_2 to SiO_2 bonds. The CHF_3 plasma was used for the surface etching. Short oxygen plasma exposure was used for the surface activation. The untreated reference sample is shown for comparison. The bond annealing time was 2 hours.

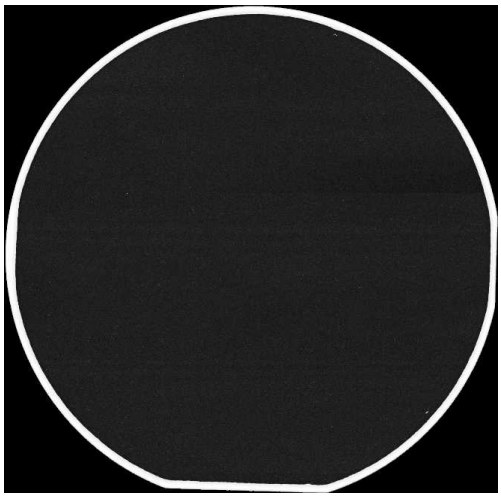

Fig. 8 Scanning acoustic misroscopy image of debondable SiO_2 to SiO_2 bond. The one wafer was modified in CHF_3 plasma before the bonding. The other wafer was exposed to oxygen plasma prior to the bonding. After bonding the wafer pair was annealed at 600°C.

PUBLICATION F

Transfer of Thin Si Layers by Cold and Thermal Ion Cutting

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Transfer of Thin Si Layers by Cold and Thermal Ion-Cutting

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ABSTRACT

We have used the crack opening method to study the mechanical exfoliation behaviour in hydrogen implanted and bonded Cz Si. We found out that the crystal orientation and boron doping influence the temperature required for mechanical layer transfer. The boron implantation at doses $>10^{13}$ cm^{-2} reduces the annealing temperature needed for mechanical exfoliation. The boron doped epilayers followed similar exfoliation behaviour as the boron-implanted samples. No lowering of the exfoliation temperature was observed for compensated and arsenic doped Si layers. The hydrogen implantation converted silicon wafer surface from p-type to n-type. The as-transferred Si layer was also found to be n-type after annealing at 200–450°C. The p-type conductivity was restored upon annealing at around 600°C. We believe that this conductivity conversion is due to the combined effect of ion-enhanced thermal donors and the presence of H-related shallow donors in the implanted layer. The p-type conductivity is restored at higher temperatures following the dissociation of the thermal donors and the out-diffusion of hydrogen. We also report that a good quality silicon on glass layer can be obtained by the bonding and ion-cutting processes.

Keywords: wafer bonding, exfoliation, silicon-on-glass

INTRODUCTION

Plasma assisted wafer bonding and layer transfer techniques can be utilized to integrate dissimilar materials at a wafer level enabling fabrication of multilayered wafers for optimal device performance. Hydrogen implantation induced exfoliation of Si has been shown to be an effective method to transfer a thin layer of Si to another wafer [1,2]. The splitting and transfer process of the hydrogen implanted and bonded Si is generally referred to as an ion-cutting process. The exfoliation of Si can be accomplished by thermal or mechanical means. Thermal exfoliation is normally carried out at a moderately high temperature of 300–600°C, whereas mechanically induced splitting of Si can be accomplished at <250°C. These low processing temperatures are particularly attractive for materials with a large difference in the thermal expansion coefficient or with a low softening point such as glass. Besides having a low process temperature, mechanical exfoliation has the advantage of producing a smooth split surface. In mechanical layer transfer or cold ion-cutting process, the implanted and bonded wafer pair is subjected to mechanical splitting forces which initiate the fracture across the bonded wafer. The delamination of a bonded wafer pair can be carried out with a gas, fluid or solid wedge [2,3,4]. Since the fracture propagates through the weakest region of a bonded wafer pair, it is necessary to achieve high bond strength at a low temperature. If the hydrogen implanted layer is weaker than the bonded interface the fracture propagates inside or near the damage zone created by the implantation. We have investigated the influence of crystal orientation and doping on the mechanical exfoliation of Si using the crack opening method [5] and Rutherford backscattering spectrometry (RBS). We also report that low-temperature plasma enhanced wafer bonding and ion-cutting processes can be used to integrate a thin single crystalline layer of Si on a glass wafer.

EXPERIMENTAL

In this work <100>, <111> and <110> oriented Czochralski (CZ) grown p-type 100 mm Si wafers with a resistivity of 1–35 Ω cm were used as donors for layer transfer. A boron or arsenic doped epitaxial (epi) Si layer was deposited on some of the <100> donor wafers. Two different boron concentrations of the epilayers 7.6 x 10^{18} cm^{-3} and 7.83 x 10^{19} cm^{-3} were studied. The arsenic concentration was 1.1–1.2 x 10^{19} cm^{-3}. To study the effect of the electrical activity of the epilayer, a compensated sample was prepared by doping the epilayer with the same

concentration level (10^{19} cm^{-3}) of boron and arsenic. The 100 mm handle wafers were <100> oriented Si, quartz glass or alkaline earth aluminosilicate (Corning 1737F) glass wafers. The thickness of the wafers was 500–600 μm. The Si handle wafers were thermally oxidized to a thickness of 500 nm of SiO_2 to make a silicon oxide to hydrophilic Si bond (oxide/Si bond). The glass handle wafers were bonded to unoxidized donor Si wafers. The donor wafers were implanted with H_2^+ at 100 keV to a dose of 4.0 x 10^{16} – 5.0 x 10^{16} H_2/cm^2. Prior to hydrogen implantation some of the <100> donor wafers were implanted with B^+ at 175 keV to a dose ranging from 10^{13} to 3 x 10^{15} B/cm^2. The boron implantation doses were adjusted so that the implanted boron concentration at the depth of exfoliation would approximately correspond to the boron doping concentration of the epilayers. No thermal annealing was used to activate the implanted boron. During the implantation the wafer temperature was maintained below 100°C. After the implantation the implanted donor wafers were bonded to the Si or glass handle wafers using the plasma enhanced low temperature bonding process [4]. The bonded Si wafer pairs were annealed in a box furnace under N_2 in two steps: first for 2 hours at 100°C and then 2 hours at 180–450°C. After annealing some of the wafer pairs were cut with a dicing saw to rectangular slices. The energy required for the delamination of the implanted layer was measured by the crack opening method [5]. A blade was inserted between the bonded wafers and a crack propagating though the implanted region was created when the H-implanted layer was sufficiently weak compared to the bonded interface. The blade was inserted along the [110] direction for <100> and <111> Si wafers and along [111] for <110> Si wafers. The surface energy of the implanted layer was calculated based on the crack length measurement [5]. The surface roughness of the split layer was measured with Digital Instruments D3100 atomic force microscope (AFM) using silicon tips in the tapping mode. The lattice damage induced by the implantation was investigated by using 2 MeV $^4He^+$ Rutherford backscattering in the channeling mode and transmission electron microscopy (TEM). The thickness of the exfoliated layer was measured by conventional backscattering in the random mode. The electrical properties of the samples were investigated with a four-point probe, a hot probe and Hall-effect measurements.

RESULTS AND DISCUSSION

The basic condition for the mechanical exfoliation process is that the bonded interface is stronger than the hydrogen implanted layer (Fig. 1). The maximum

bond strength of oxide/Si bonds is achieved at 200–250°C if a proper plasma activation procedure is used [4]. When the implanted hydrogen dose is > 4 x 10^{16} H_2/cm^{-2} and the annealing temperature of > 250°C is used, the bonded interface is stronger than the hydrogen implanted region enabling mechanical layer transfer. The strength of the H-implanted layer drops down linearly with the increasing annealing temperature when a certain critical temperature is exceeded. This temperature, which is required for mechanical exfoliation, reduces with the increasing hydrogen dose. We have been able to transfer low doped Si layers after annealing at 200°C when a implantation dose of 5 x 10^{16} H_2/cm^2 was used.

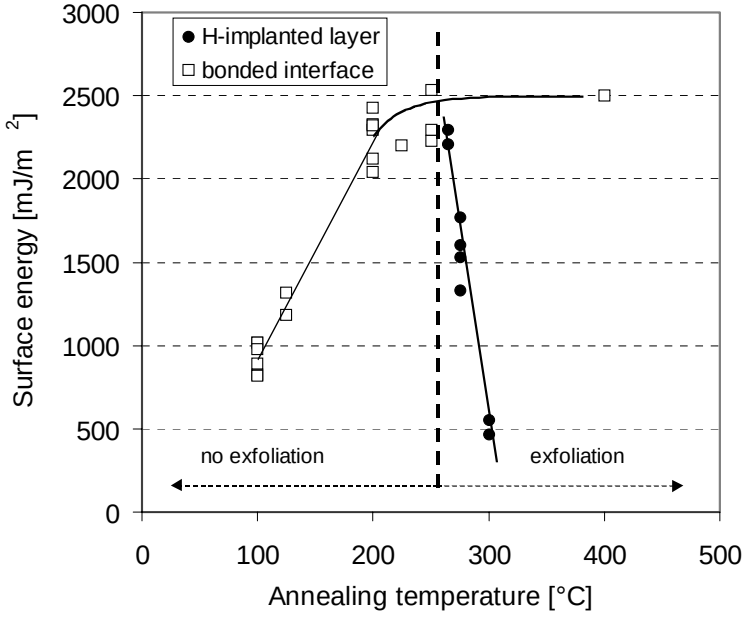

Fig. 1. Two-beam cross-sectional TEM-image (X30k) of the H-implanted and bonded <100> Si. The donor Si was implanted with H_2 at 100 keV with a dose of 5 x 10^{16} cm^{-2}. The implanted donor wafer was bonded to oxidized handle Si wafer using plasma assisted bonding process [4]. After implantation and bonding the sample was annealed at 250°C for 2 hours. The cut depth obtained by the RBS-measurement is marked on the figure.

Figure 2 shows cross-sectional TEM-image of the H-implanted and bonded <100> Si. The sample was annealed at 250°C after implantation and bonding. The damage zone caused by the hydrogen implantation can be observed as a

well-defined region having a thickness of ~200 nm. The Si areas outside the damage zone are essentially featureless. The RBS-measurement yielded a thickness of around 480 nm for the exfoliated layer. Comparison of TEM and RBS results suggests that the fracture takes place near the far end of the damage zone when the hydrogen dose of 10^{17} H^+/cm^2 is used.

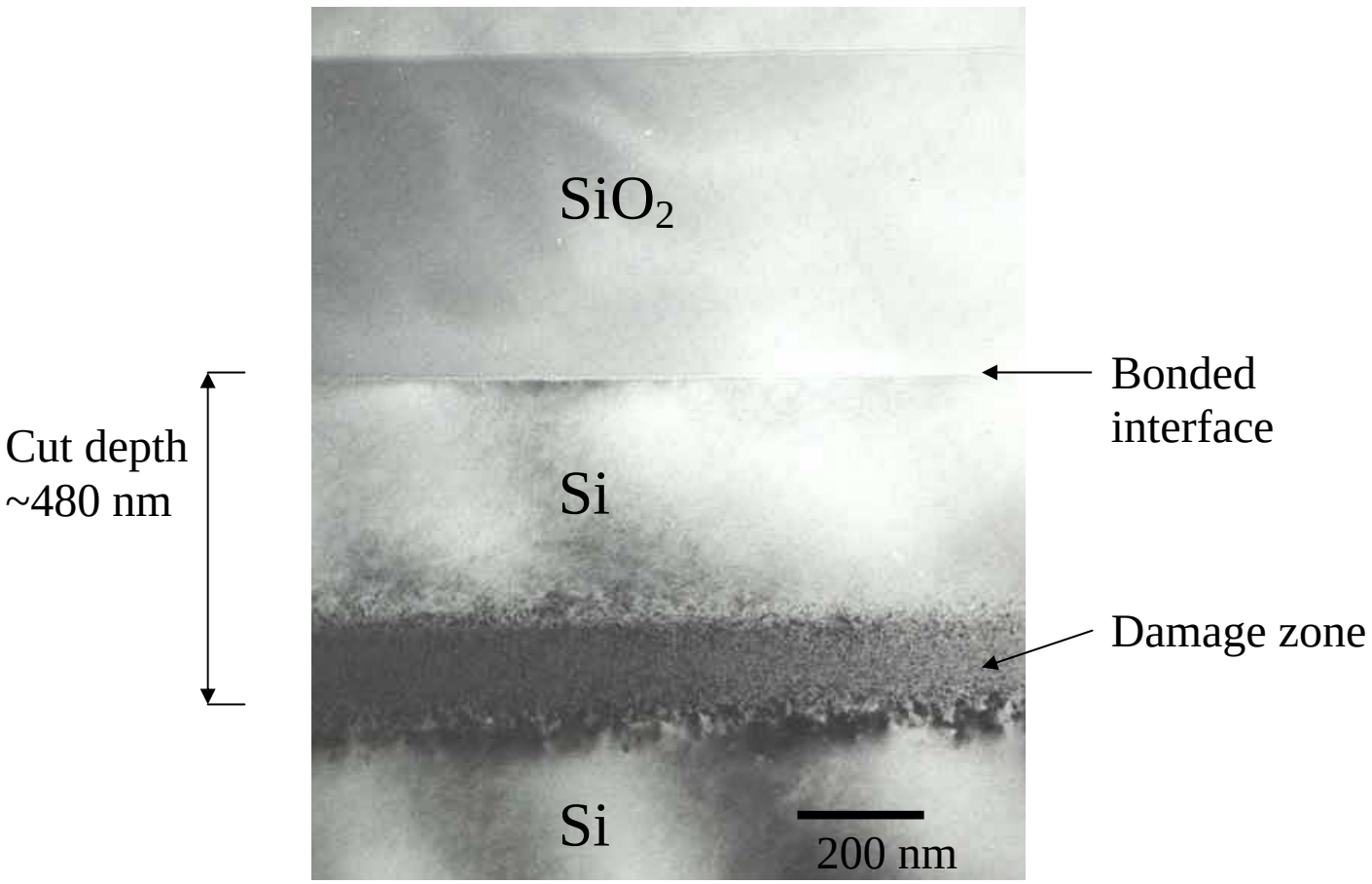

Fig. 2. Two-beam cross-sectional TEM-image (X30k) of the H-implanted and bonded <100> Si. The donor Si was implanted with H_2 at 100 keV with a dose of 5 x 10^{16} cm^{-2}. The implanted donor wafer was bonded to oxidized handle Si wafer using plasma assisted bonding process [4]. After implantation and bonding the sample was annealed at 250°C for 2 hours. The cut depth obtained by the RBS-measurement is marked on the figure.

The effect of boron doping and crystal orientation on the mechanical splitting of Si

The strength of the hydrogen implanted layer was found to decrease with increasing boron doping (Fig. 3) in agreement with the earlier results on surface blistering in H-implanted Si [6,7]. The samples implanted with boron prior to hydrogen implantation follow similar exfoliation behavior as the boron-doped epilayers. This indicates that the activation of the boron prior to H-implantation is not responsible for changes in the temperature required for mechanical splitting. The arsenic doped epilayers show no difference in the exfoliation behavior compared to undoped Si. If boron and arsenic are introduced simultaneously to obtain a heavily doped, compensated epilayer, the exfoliation strength is similar to that in the undoped Si. In B-implanted arsenic doped epilayers, the strength of the H-implanted layer is also similar to that obtained for undoped silicon. This spells out that the presence of the boron is not a sufficient condition for the lowering of the exfoliation temperature. It has been reported that crystal defects and shallow acceptors, such as boron, may trap hydrogen [8]. However, the damage due to boron implantation is not the primary reason for the reduced exfoliation strength, since our channeling RBS measurements showed that B+H co-implanted and B-doped H-implanted epilayers have less damage than the undoped samples implanted with hydrogen only. It has been reported that shallow acceptors in silicon are neutralized by monoatomic hydrogen [8]. This compensation effect involves silicon-hydrogen bonding. The boron neutralization and the associated Si-H bonding are suppressed by counterdoping with n-type impurities. Although this mechanism for hydrogen compensation of shallow p-type impurities provides mainly circumstantial similarities with our exfoliation experiments we propose that the same mechanism is responsible for the doping effects in the Si layer transfer. Measured by channeling RBS the lattice damage peak due to implantation appeared to move closer to the wafer surface if the peak concentration of boron is $> 10^{19}$ cm^{-3}. The depth of exfoliation was 478 nm for undoped Si and 460 nm for heavily boron doped samples. This shows that the exfoliation depth in Si is associated with the peak lattice damage generated by the implantation process.

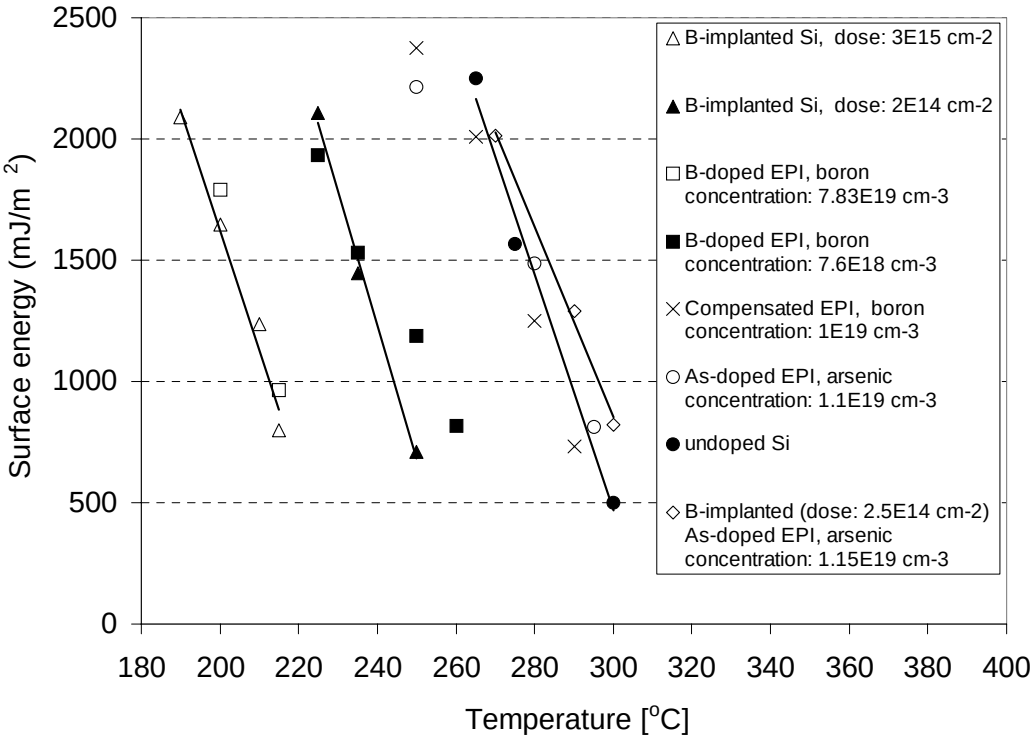

Fig. 3. The measured surface energy of the hydrogen implanted layer in <100> Si for the various doping schemes. The hydrogen implantation was done with H_2^+ at 100 keV with a dose of 4.5 x 10^{16} H_2/cm^{-2}. The annealing time was 2 hours. The boron implantation doses were adjusted so that the implanted boron concentration at the depth of exfoliation corresponds approximately to the boron doping concentration of the epilayers.

The strength of exfoliation was found to depend on the crystal orientation. The surface energies measured for the exfoliation process were 700, 1500 and 2300 mJ/m^2 for <100>, <111> and <110> oriented Si, respectively after annealing at 290°C. The thickness of the exfoliated layer was not affected by the crystal orientation being 478–488 nm for all samples. To understand the role of the implantation damage in producing the dependence on crystal orientation we studied separately the damage distributions in as-implanted samples. Using RBS channeling measurements we estimated that the normalized and corrected yield that can be attributed to scattering from displaced atoms is 5.5–7.5 % for all

three orientations. The result was obtained taking into account the differences in the intrinsic channeling yield along the different crystal axes and using appropriated normalization and correction methods [9]. Our result is similar to the data obtained by Zheng et al. [9] suggesting that the orientation has no significant effect on the disorder produced by the implantation.

Silicon on glass wafers formed by ion-cutting

Bonding of the donor Si wafer to a quartz glass (SOQ) or a Corning 1737F glass wafer (SOG) was carried out using plasma assisted bonding process without any intermediate layer between the wafers [4]. After plasma treatment the bonding occured spontaneously over the entire surface of the wafers under a slight applied pressure at the center of the wafers. No voids were detected at the bonded interface (Fig. 4). Since silicon and quartz glass have largely different thermal expansion coefficients we used $H_2^+ + B^+$ co-implantation to reduce the temperature needed for the exfoliation. The implantation doses were 3×10^{15} for B^+ and 4.5×10^{16} cm^{-2} for H_2^+. The Si/quartz wafer pairs were thermally split at 200°C because mechanical delamination process by the solid wedge was not found to be reproducible due to fragility of the glass wafers. However, it has been reported that more gentle peeling process can be obtained by a gas or liquid wedge [2,3]. Silicon on glass structure was formed using hydrogen implantation with a dose of 4.5×10^{16} H_2/cm^2. The splitting temperature was 400°C. The RBS channeling spectrum, <100> aligned, showed that the as-exfoliated Si layer on glass is crystalline in nature and the ion implantation damage is located near the surface of as-transferred Si layer. The AFM-measurement yielded an average surface roughness of 2.5–3.5 nm for the as-split surface of Si on glass layer (Fig. 5). As pointed out previously, the donor wafers used for SOG structures were B-doped CZ Si with a resistivity of 1–35 ohmcm. Using hot probe measurements, we found n-type conductivity in the implanted layer of the as-implanted wafers. The backside of the wafer remained p-type. The as-transferred Si layer and the as-split surface of the donor wafer were also found to be n-type after exfoliation at 400°C. The resistivity of the as-transferred SOG-layer was 0.1–0.3 ohmcm. At around 600°C the p-type conductivity of the exfoliated layer was restored. It is known that shallow donors are created in Si by hydrogenation. Some of these donors are associated with hydrogen enhanced thermal donors in CZ Si [10,11] and the others are caused by hydrogen and defect complexes [8]. We believe that the type of conversion

observed in our samples is due to the combined effect of ion-enhanced thermal donors and the precense of H-related shallow donors in the implanted layer.

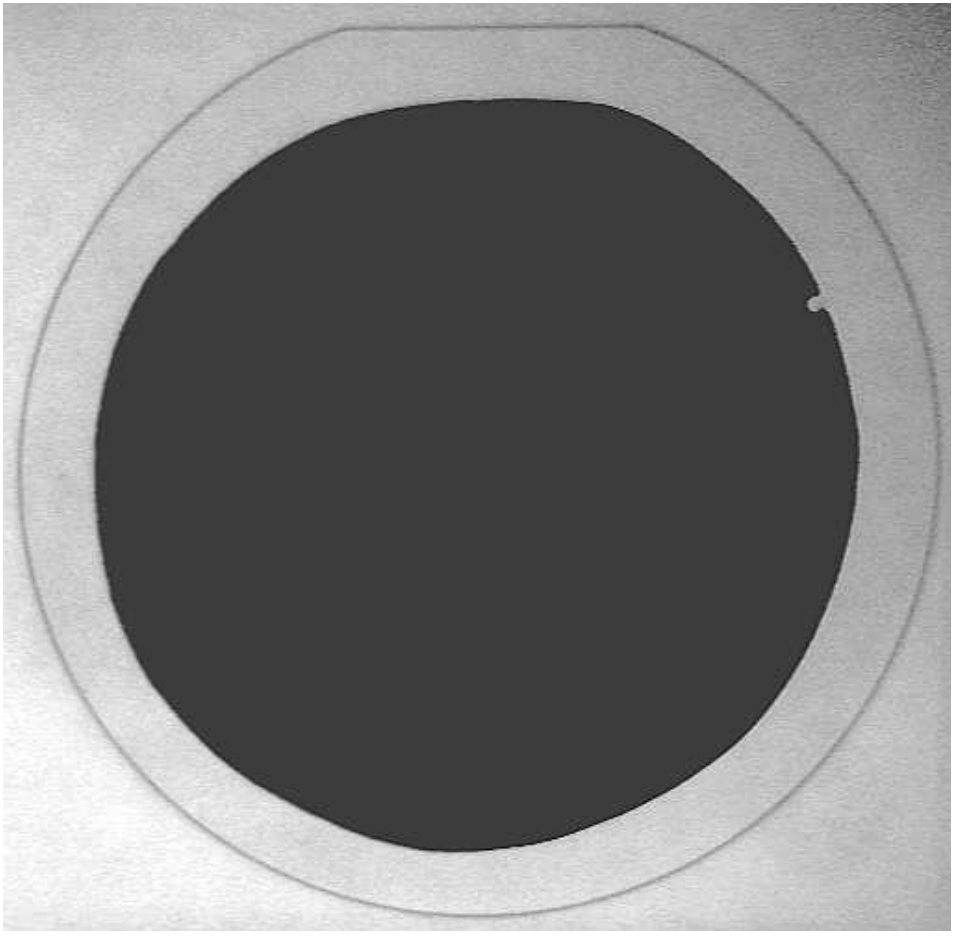

Fig. 4. The image of 100 mm silicon on quartz glass wafer. The wafer was exfoliated at 400°C. The dark area in the middle is the transferred Si layer with a thickness of about 480 nm. The outer white area is glass. No voids were detected at the bonded interface.

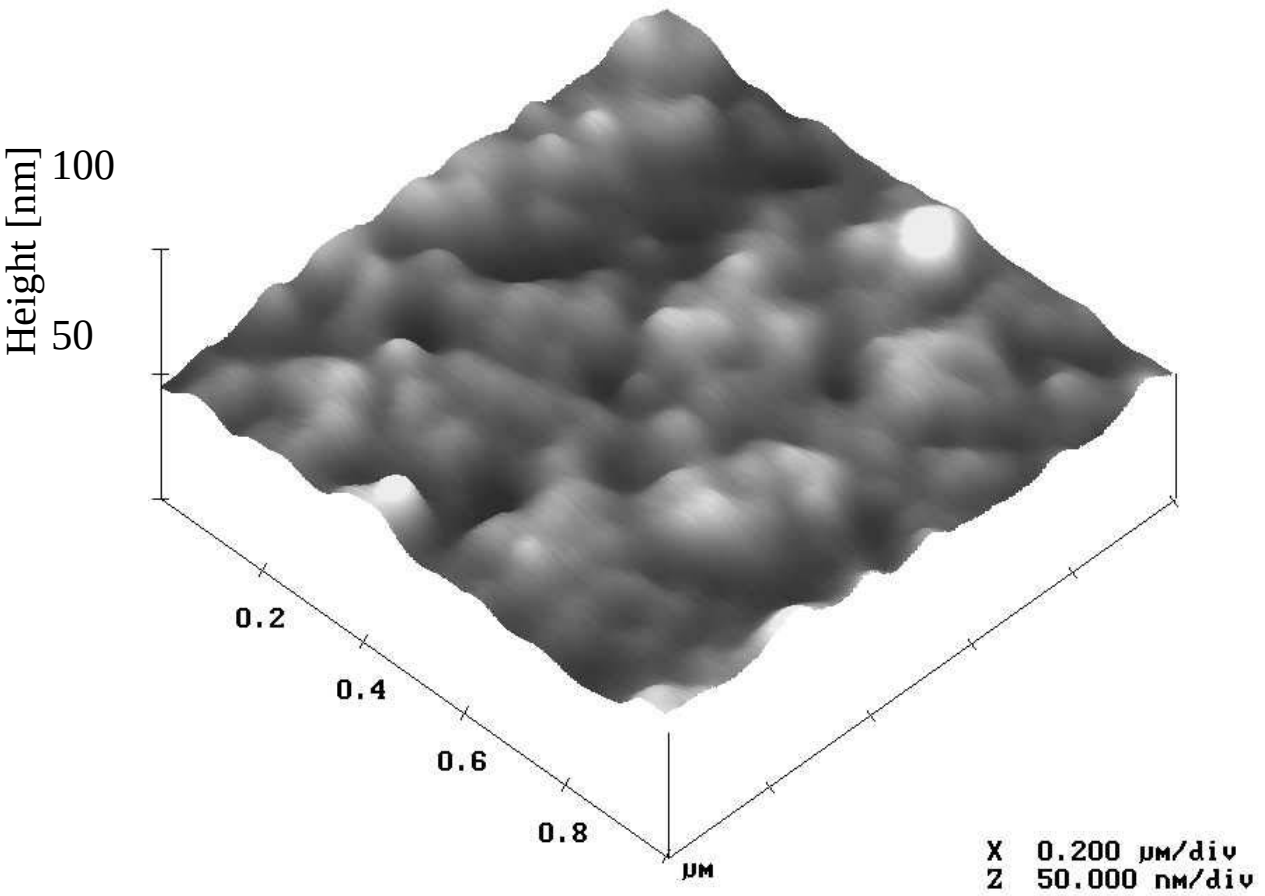

Fig. 5. AFM image of the as-split surface of silicon on glass layer. The average surface roughness (R_a) is 2.8 nm. The exfoliation was carried out at 400°C.

The p-type conductivity was restored at higher temperatures because of dissociation of the thermal donors and the out-diffusion of hydrogen. We direct attention to the fact that the restoration of the original conductivity type with reasonable carrier mobilities is a prerequisite for any useful application of these layers in electronics.

SUMMARY

We have found that, in silicon layer transfer process, the temperature required for exfoliation of silicon depends on the crystal orientation and boron doping. The cut depth is largely determined by the damage peak due to the implantation. The hydrogen implantation converted silicon wafer surface from p-type to n-type. The p-type conductivity was restored upon annealing at 600°C. Our results suggest that a good quality silicon on glass layer can be achieved by the ion-cutting process if the damaged surface region of the Si layer is removed.

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Title

Direct wafer bonding for MEMS and microelectronics

Abstract

Direct wafer bonding is a method for fabricating advanced substrates for microelectromechanical systems (MEMS) and integrated circuits (IC). The most typical example of such an advanced substrate is the silicon-on-insulator (SOI) wafer. SOI wafers offer many advantages over conventional silicon wafers. In IC technology, the switching speed of circuits fabricated on SOI is increased by 20-50% compared to circuits fabricated on a bulk Si wafer. The required operation voltage is lower in ICs on SOI than in ICs on a bulk silicon wafer, which decreases power consumption and chip heating. In the MEMS industry, the buried oxide layer works as a good sacrificial layer during release etching of diaphragms, beams etc. and offers an excellent etch stop layer for silicon etching. Direct wafer bonding can also be used in the fabrication of more complex structures than SOI. The wafers to be bonded can be of different materials, can contain patterns, and may have multiple layers or ready-made devices.

This thesis reports on studies of direct wafer bonding and its use in various applications. Different bonding processes used in microelectronics are briefly described. The main focus of this thesis is on the plasma activation-based low temperature bonding process, and on the control of bond strength by surface preparation.

A novel method for bond strength measurement is introduced. This method, based on buried oxide etching, is presented and compared with other methods used in evaluating bond quality.

This thesis also contains results on research of different applications requiring direct wafer bonding. Heterogeneous integration, pre-processed SOI fabrication, and wafer scale packaging are the main application topics.

Keywords

direct wafer bonding, MEMS, microelectronics, microelectromechanical systems, SOI, silicon-on-insulator, integrated circuits, bond strength measurement, heterogeneous integration, pre-processed SOI fabrication, wafer-scale packaging, plasma activation

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Tekijä(t)
Suni, Tommi

Nimeke

Puolijohdekiekkojen suoraliittäminen mikroelektroniikan ja mikromekaniikan sovellutuksissa

Tiivistelmä

Puolijohdekiekkojen suoraliittäminen on menetelmä valmistaa kehittyneitä alustoja mikroelektromekaanisille systeemeille (MEMS) ja integroiduille piireille. Yleisin tämänlainen kehittyneempi alusta on SOI-kiekko, jossa kantajakiekon ja varsinaisen komponenttipiikerroksen välissä on eristävä oksidikerros. Verrattuna tavallisiin piikiekkoihin SOI-kiekot tarjoavat useita parannuksia. Integroitujen piirien tapauksessa kytkentänopeus on SOI:lla 20–50 % nopeampi, käyttöjännite matalampi ja energian kulutus pienempi. MEMS-teknologiassa haudattu oksidi toimii uhrautuvana kerroksena kalvojen ja palkkien vapautusetsauksessa ja myös pysäytys-kerroksena piin syövyttämisessä. Suoraliittämistä voidaan käyttää myös monimutkaisempien rakenteiden kuin SOI-kiekkojen valmistamiseen. Liitettävät kiekot voivat olla eri materiaaleista, kuvioituja tai sisältää valmiita komponentteja.

Tässä väitöskirjassa keskitytään pääasiassa korkean ja matalan lämpötilan suoraliittämiseen sekä liitoslujuuden kontrollointiin pintoja karhentamalla. Kirjassa esitellään lyhyesti myös muut kiekkoliitostekniikat.

Väitöskirjassa raportoidaan myös uusi menetelmä mitata liitoslujuus kahden kiekon välillä. Menetelmä perustuu haudatun oksidin märkäsyövyttämiseen ja sitä verrataan myös muihin raportoituihin liitoslujuuden mittausmenetelmiin.

Tämä väitöskirja sisältää myös tuloksia suoraliittämisen käyttämisestä muutamiin erilaisiin sovellutuksiin, kuten kiekkotason paketointiin, heterogeeniseen integrointiin ja esiprosessoitujen SOI-kiekkojen valmistukseen.

Avainsanat

direct wafer bonding, MEMS, microelectronics, microelectromechanical systems, SOI, silicon-on-insulator, integrated circuits, bond strength measurement, heterogeneous integration, pre-processed SOI fabrication, wafer-scale packaging, plasma activation

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VTT PUBLICATIONS 609 Direct wafer bonding for MEMS and microelectronics Tommi Suni

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