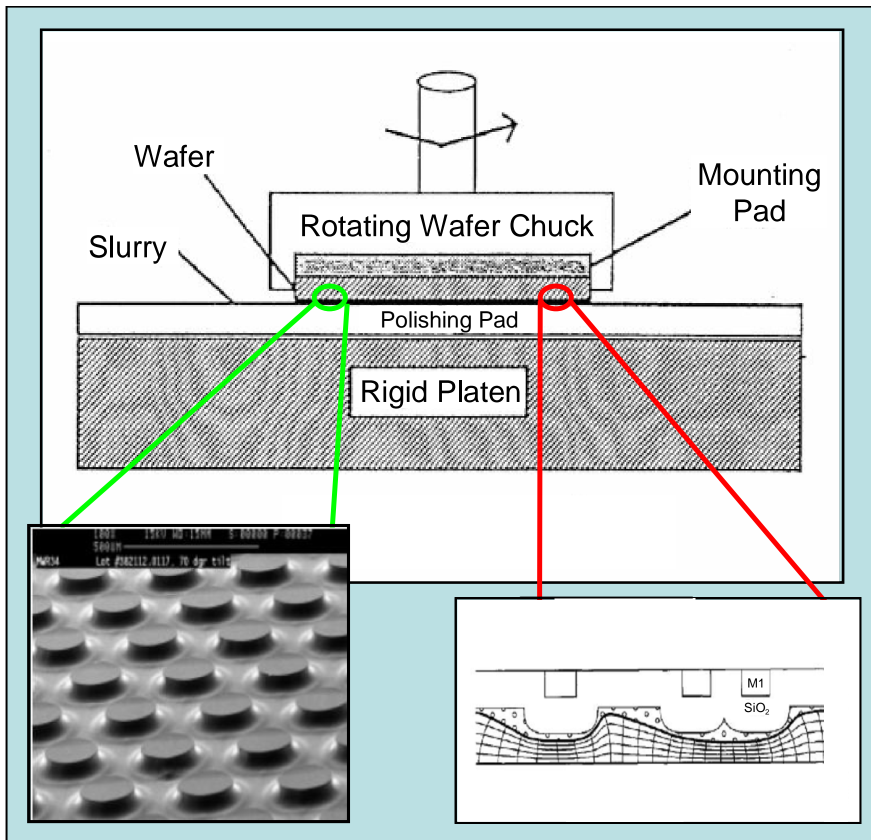
ESPOO 2006 VTT PUBLICATIONS 611



Martin Kulawski

Advanced CMP Processes for Special Substrates and for Device Manufacturing in MEMS Applications

VTT

VTT PUBLICATIONS 611

Advanced CMP Processes for Special Substrates and for Device Manufacturing in MEMS Applications

Martin Kulawski

VTT

Dissertation for the degree of Doctor of Science in Technology to be presented with due permission of the Department of Electrical and Communications Engineering, for public examination and debate in the large Seminar room at VTT Micronova (Espoo, Finland) on Friday the 20th of October, at 12 o'clock noon.

ISBN 951–38–6855–9 (soft back ed.)
ISSN 1235–0621 (soft back ed.)

ISBN 951–38–6856–7 (URL: http://www.vtt.fi/inf/pdf/)
ISSN 1455–0849 (URL: http://www.vtt.fi/inf/pdf/)

Copyright © VTT Technical Research Centre of Finland 2006

JULKAISIJA – UTGIVARE – PUBLISHER

VTT, Vuorimiehentie 3, PL 1000, 02044 VTT
puh. vaihde 020 722 111, faksi 020 722 4374

VTT, Bergsmansvägen 3, PB 1000, 02044 VTT
tel. växel 020 722 111, fax 020 722 4374

VTT Technical Research Centre of Finland, Vuorimiehentie 3, P.O.Box 1000, FI-02044 VTT, Finland
phone internat. +358 20 722 111, fax + 358 20 722 4374

VTT, Tietotie 3, PL 1000, 02044 VTT
puh. vaihde 020 722 111, faksi 020 7012

VTT, Datavägen 3, PB 1000, 02044 VTT
tel. växel 020 722 111, fax 020 722 7012

VTT Technical Research Centre of Finland, Tietotie 3, P.O. Box 1000, FI-02044 VTT, Finland
phone internat. +358 20 722 111, fax +358 20 722 7012

Technical editing Anni Kääriäinen

Valopaino Oy, Helsinki 2006

Kulawski, Martin. Advanced CMP Processes for Special Substrates and for Device Manufacturing in MEMS Applications. Espoo 2006. VTT Publications 611. 80 p. + app. 60 p.

Keywords CMP, micro electro mechanical systems, polishing, fixed abrasive, MEMS, SOI, silicon-on-insulator, direct wafer bonding, DWB, low temperature bonding, FA

Abstract

The present work reports on studies and process developments to utilize the chemical mechanical planarization (CMP) technology in the field of micro electrical mechanical systems (MEMS). Approaches have been undertaken to enable the manufacturing of thick film SOI (silicon-on-insulator) substrates with a high degree of flatness as well as utilizing CMP for the formation of several novel MEMS devices.

Thick film SOI wafers are of high interest in MEMS manufacturing as they offer obvious benefits as a starting material or foundation for more complex structures. Precise control of the SOI layer thickness as well as the removal uniformity is of critical importance to fully utilize the benefits of this technology. By combining fixed abrasive (FA) pads for polishing and novel grinding techniques it is shown that major improvements can be achieved over the standard manufacturing sequence. Analysis of the material removal rate (MRR) dependency on several process parameters is made. Together with the FA pad vendor a suitable consumable set for SOI is generated, which shows long term stability in the generated process. A comparison with standard methods is undertaken to prove the surface and crystalline quality of the resulting substrate material is equivalent. Analysis is done to understand the microscopic mechanism of removal.

The CMP process is applied to several MEMS structures to smooth deposited oxide films and to enable direct wafer bonding (DWB) at low temperatures. This allows the design of bonded multiple stack layers including heat sensitive materials such as metals.

FA CMP is applied to large pattern MEMS for total planarization but also for smoothing of the surface of single protruding structures while minimizing edge rounding and preserving the original intended pattern shape. With dedicated CMP steps thick film polysilicon smoothing is demonstrated enabling DWB. The chemo-mechanical particularities of the FA pad are investigated in detail.

Preface

It is about 10 years ago, that I was exposed to the newly introduced CMP Technology. As a student I developed first polishing processes at the Fraunhofer Institute for Silicon technology ISiT in Itzehoe, Germany.

The Technology was rather unknown in Europe at that time and only a few people were actively working on CMP in Germany. A lot of development has happen since then. I kept involved with CMP from that time on and was able to follow the rapid evolution of this process and its aggressive introduction into more and more areas of the IC production.

With my re-entry into the world of research and development I was able to contribute myself to the amazing success story of one of the youngest and most widely growing processes. Being exposed to the world of MEMS and responsible to establish the CMP technology at VTT it was a logic consequence to introduce the convenient polishing technology to micromechanical devices.

By connecting the experience of earlier work and having the great opportunity to work together with world leading companies like Okmetic, VTI, 3M and Strasbaugh it was possible to create in short time and with limited amount of work force a new technology platform for the future demands of the growing MEMS world. Finally I have been able to result my experimental work with this dissertation summing up about 3 years of exciting research and development.

Martin Kulawski, Espoo, July 2006

List of Publications

This work is based on the following publications, which are referred to in the text by their alphabetic numerals. Furthermore, unpublished results and results of other own publications [Ref. 74, 78] are included in the text to provide the reader with a most comprehensive view of the status of the overall research.

Paper A: M. Kulawski, K. Henttinen, I. Suni, F. Weimar, J. Mäkinen; *A novel CMP Process on Fixed Abrasive pads for the Manufacturing of highly planar thick film SOI Substrates;* Mat. Res. Soc. Proc. **767**, (2003), pp. 133–139.

Paper B: M. Kulawski, H. Luoto, K. Henttinen, I. Suni, F. Weimar, J. Mäkinen; *Advances in the CMP Process on Fixed Abrasive Pads for the Polishing of SOI-Substrates with High Degree of Flatness;* Mat. Res. Soc. Proc. **816**, (2004), pp. 191–196.

Paper C: M. Kulawski, H. Luoto, T. Suni, F. Weimar, J. Mäkinen; *Integration of CMP Fixed Abrasive polishing into the Manufacturing of Thick film SOI Substrates;* Mat. Res. Soc. Proc. **867**, (2005), pp. 111–116.

Paper D: M. Kulawski, H. Luoto, K. Henttinen, T. Suni, F. Weimar, J. Mäkinen; *Polishing of Bulk Micro-Machined Substrates by Fixed Abrasive Pads for Smoothing and Planarization of MEMS Structures;* Proc. IEEE/SEMI Advanced Semiconductors Manufacturing Conference, Munich 2005.

Paper E: J. Molarius, M. Kulawski, T. Pensala, M. Ylilammi; *New Approach to Improve the Piezoelectric Quality of ZnO Resonator Devices by Chemomechanical Polishing;* The Nano-Micro Interface: Bringing the Micro and Nano Worlds Together; Ed. H. J. Fecht, M. Werner; Wiley-VCH Weinheim 2004; ISBN: 3-527-30978-0.

Paper F: H. Luoto, T. Suni, M. Kulawski, K. Henttinen, H. Kattelus; *Low-temperature bonding of thick-film polysilicon for MEMS;* Journal of Microsystems Technology, Vol. 12, No. 5, pp. 401–405, (2006).

Author's Contribution

The author Martin Kulawski is the sole writer of the Papers A to D. All direct CMP related experiments, design and analysis were made by the author in the Papers A and B. All design and almost all CMP related experiments and analysis were made by the author contributing to the Papers C and D. Supervising and all of the experimental design concerning CMP as well as the related polishing experiments and their analysis was provided by the author to accomplish the Paper E. Writing was contributed to Paper E relating to CMP and its conclusions. Part of the writing and contribution to the experiments and their design as well as a good portion of the results' analysis was contributed to Paper F.

Additionally, related results of the Papers A to F and further results of the recent research has been presented by the author at the Semi MEMS Forum in Munich, Germany in 2005, and several CMP User Group Meetings of the VDE in Germany during 2001 trough 2005 as well as the American Vacuum Society's CMP User Group in Santa Clara, CA in 2005 and the Nordic Semiconductor Meeting in 2005 in Oslo, Norway. The author was invited lecturer at the one-day short course for CMP manufacturing in conjunction with the CMP-MIC 2006 in Fremont CA, as well as invited speaker at the 6th Spring Meeting of the ISE in Singapore in 2006.

Contents

Abstract 3

Preface 5

List of Publications 6

Author's Contribution 8

List of Acronyms and Symbols 11

1. Introduction 14
   - 1.1 History and Background of CMP 14
   - 1.2 Scope and Objectives of the Thesis 17
   - 1.3 Facilities, Equipment, Methods and Material 18
   - 1.4 Summary of the Papers 19

2. CMP Technology 21
   - 2.1 The CMP Process 21
   - 2.2 Oxide CMP 24
   - 2.3 Silicon CMP 26
   - 2.4 Characteristics of Conventional CMP 27
   - 2.5 Characteristics and Technology of Fixed Abrasive Pads 33

3. Formation of Thick-Film SOI Substrates 38
   - 3.1 The Thick-Film SOI Manufacturing Sequence 38
   - 3.2 The Sub-Surface Damage Layer 40
   - 3.3 Uniformity of Silicon CMP 42
   - 3.4 Surface Quality of CMP 50
   - 3.5 Stability of the New Sequence 53

4. CMP of MEMS Structures 57
4.1 Surface Smoothing and Planarization 57
4.2 Pattern Conservation 63
4.3 CMP of Polysilicon Films 66

5. Conclusions 69

Acknowledgements 70

References 73

Appendices
Papers A–F

List of Acronyms and Symbols

AFM	Atomic force microscopy
BAW	Bulk acoustic waves
BEOL	Back end of the line; meaning the metallization layer formation on wafer level of IC circuitry after the transistors are ready
BOX	Buried oxide
C	Capacitance
CMOS	Complementary metal oxide silicon field effect transistor technology
CMP	Chemical mechanical planarization
COF	Coefficient of friction
CVD	Chemical vapour deposition
die	Short for one microchip on the wafer during production
DIW	De-ionized Water
DOF	Depth of focus
DSP	Double side polished (Wafers)
DWB	Direct wafer bonding
FA	Fixed abrasive
FBAR	Film bulk acoustic resonators
FEOL	Front end of the line, describing the part of the wafer fab in which the transistors are formed
FTIR	Fourier transform infrared spectroscopy
HSS-Slurry	High selectivity slurry (selective between oxide and nitride for STI processing)
IC	Integrated circuits
ILD, IMD	Inter-layer dielectric, Inter-metal dielectric
IM	Integrated metrology

ITRS	International technology roadmap society
K_P	Preston coefficient
LOCOS	Local oxidation of silicon; older isolation/separation technology
Low-k	Describing dielectric materials with lower dielectric constant than silicon dioxide
LT bonding	Low temperature bonding technique
MEMS	Micro electrical mechanical systems
MOEMS	Micro opto electrical mechanical systems
MRR	Material removal rate
NU	Non-uniformity
OISF	Oxide induced stacking faults
P	Down pressure
PECVD	Plasma enhanced chemical vapour deposition
Q-factor	Quality factor for resonators, filters and oscillators describing energy losses
R	Resistance
RC-delay	Delay created by resistance of conductors and parasitic capacitances inside of a fast microchip
rf	Radio frequency
rf-MEMS	Radio frequency micro electrical mechanical systems
rms	Root mean square (averaging factor)
SAM	Scanning acoustic microscope
SAW	Surface acoustic waves
SEM	Scanning electron microscope
SOG	Spin-on-glass
SOI	Silicon on insulator
SSD	Sub-surface damage

SSP	Single side polished (Wafers)
STI	Shallow trench isolation; current isolation /separation technique
SW-tool	Software-tool, program
TTV	Total thickness variation
v	Velocity
WIWNU	Within wafer non uniformity
WTWNU	Wafer to wafer non uniformity

1. Introduction

1.1 History and Background of CMP

Using polishing materials in order to achieve a smooth and planar surface is a very old method. It was recognized early that the right type of liquid combined with an abrading substance would result in faster removal of material and often provide better surface finish, while each component on its own would maybe have very little or even no effect. In the long run, a huge variety of different combinations of abrasive and chemistry were found to polish almost any material and surface to the desired level. The ancient concept of polishing was the basis for the actual chemical mechanical polishing or chemical mechanical planarization (CMP), which is used in the semiconductor industry today. Either an abrasive particle can remove atomic clusters with the support of chemical active species or, vice versa an abrasive particle mechanically weakens the chemical bond of a crystalline network, enhancing the chemical dissolution during the polishing procedure.

As industrial manufacturing was developing, ever higher accuracy and planarity of surfaces were needed. As early as 1927 Preston made his first attempt to calculate the achievable removal rate of glass, based on the process parameters of the polishing procedure [1]. Glass plate polishing achieved a certain level of quality, but more science was required to further improve the results and to gain better predictions of the outcome of a complicated and uninterruptible procedure. Lessons learned during these investigations were also used to influence the design of new polishing tools.

From these humble beginnings, CMP has evolved to become one of the fastest growing and most important processes used in the IC industry [2] today. Over the past fifteen years the IC industry has further developed the CMP process technology. One of the latest examples is the upgrade of the tool sets with integrated (in-situ) measurement (IM) techniques. CMP is now considered to be ***the*** enabling process for the current technology [3] and it is expected to also guide the chip makers further [4] along Moore's law [5].

In 1961 R. J. Walsh adopted the idea of Monsanto Company to use colloidal silica rather than conventional abrasives for improving the results on raw silicon wafer polishing. The patent over the new wax-less polishing apparatus for thin wafers was issued in 1974 [6]. Together with alkaline chemistry the use of silica particles resulted in very flat and smooth surfaces. Furthermore, a significant reduction in process time was gained, because of well increased removal rates.

CMP was further improved by the efforts of IBM at the end of the 70's and in the early 80's [7, 8]. As the device density was growing under continues down scaling, more than one connecting metallization layer was required. This in turn led to an increased topography which resulted in poor step coverage at the secondary and following metallization layers. Established planarization techniques such as SOG (Spin on glass) were no longer able to provide sufficient flatness. Surface topography became a major issue due to limited depth of focus (DOF) associated with lithography processes. Yield and long term stability were the new issues, so that a more global planarization of the intermetal dielectric (IMD) layers became necessary [9]. By increasing the thickness of each single IMD and planarizing the oxide by CMP prior to next metallization topography was reduced and multiple layers of wiring became possible without suffering from yield problems due to the above mentioned problems.

With further increases in transistor density the LOCOS process (local oxidation of silicon) for transistor isolation, used successfully up to that point, was no longer feasible as it consumed a comparably large amount of chip area (die). Shallow trench isolation technology, STI for short, was developed during the eighties [10, 11]. Also here CMP played the key role as the enabling technology for precise removal of the excess oxide being filled in the pre-etched bulk silicon with accurate stop on top of the thin nitride mask. This marked also the transition of CMP from BEOL (back-end-of-the-line) into the FEOL (front-end-of-the-line) region in the IC (integrated circuit) processing.

Meanwhile CMP has also been introduced to the metallization process itself. The (dual-) damascene technique was developed to form plugs and connecting lines by pre-patterning of the IMD, overfill and CMP for excess metal removal. This was done first with aluminium later with tungsten [12]. Also on device level the first contact formation using highly doped polysilicon was formed by

CMP damascene processing as well as e.g. the novel technique of deep trench capacitor formation [13].

With the increased speed of the IC circuitry the RC-delay (series resistor and parasitic capacitor causing notable switching delay of transistor circuits) had to be considered, which resulted in the implementation of low-k dielectrics and copper metallization [14]. Again, CMP enabled the new approach as no feasible etching process was available for copper so that damascene processing became the mandatory metallization sequence [15]. A lot of continuous research and development is required however, to keep pace with the ever decreasing line widths, which helps to keep CMP up-to-date for the future technology nodes established by the ITRS (International roadmap Society) road map [16].

Besides the conventional method of slurry-based polishing also novel approaches have been developed in order to improve the well known drawbacks of the CMP process. Abrasive free polishing of copper utilizes a well balanced chemistry as lubrication liquid and only the polishing pad acts as the mechanically abrading body for the controlled removal of copper [17]. Fixed abrasive (FA) pads contain the abrading particles embedded in micro-replicated features rather than free floating particles used in the dispensed slurry to gain better planarization results and to avoid the dishing and erosion of the pattern structure [18]. Modified movement by orbital or belt systems try to overcome the problems with non-uniformity of the classic rotary systems as well as using through the pad slurry feeding instead of central dispensing [19, 20].

Outside of the IC industry adjacent technologies have also recognized the apparent benefits of the CMP process. Providing unique possibilities of smoothing surfaces and planarizing patterns CMP is also interesting for the MEMS (Micro electrical mechanical systems) area, where constantly more sophisticated structures are developed. The materials, the scale and pattern densities required for the fabrication of MEMS devices will however necessitate additional process development work and cannot rely on the available processing techniques developed by the IC industry.

1.2 Scope and Objectives of the Thesis

The research work and publications contributing to this thesis are aiming at the improvement of the utilization potential of CMP in the area of MEMS technology and special substrate manufacturing. This is done by applying novel technologies and combining also the knowledge of both the standard silicon polishing and the IC manufacturing processes.

Advanced MEMS device formation often utilizes SOI (silicon on insulator) wafers instead of standard silicon substrates. As these wafers are often made according to the special needs of the latter products, they require individual oxide and device layer thicknesses, which usually can only be achieved by a more mechanical approach than the ion cutting method for the IC SOI-substrates. Grinding and polishing is used to form the device layer to the desired thickness level. This causes problems in terms of repeatability and uniformity with the classic silicon polishing techniques, as requirements in thickness control and uniformity of the SOI layer are often very high and ever increasing. The so-called pad-edge-effect prevents the optimum result and slurry-based silicon polishing requires a large amount of total removal in order to provide suitable surface quality, often at the cost of good flatness.

Therefore significant effort has been dedicated in this work to improve the flatness of thick-film SOI substrates by enabling the use of novel CMP methods and their development towards substrate manufacturing. The work also includes improvements in the preceding thinning process, surface grinding, as substantial benefits can be generated when approaching these two process steps concurrently.

A very practical approach for MEMS formation is the use of engineered substrates, were cavities or other structures are buried below the device layer prior to SOI formation. This process contains a lot of work in enabling the critical LT (Low temperature) bonding after processing the device wafer. CMP processes have been developed to ensure the successful bonding by providing a suitable planarity and surface roughness down to the sub-Å level. Within this development it was possible to utilize the processes also for smoothing and planarization of thick deposited polysilicon films, a novel approach in the functional substrate manufacturing.

Further efforts to improve surface roughness and topography were dedicated to multiple film stacks. The roughness of each single layer is cumulative to the top-level, but a smooth surface is required, e.g. for growth of highly texture dependent active films such as piezo materials or for enabling LT bonding. The maximum allowed removal is often very small and the thickness of the layers as well as the shape of the pattern has to be controlled very precisely because it defines optical and acoustical parameters of the completed device.

The key approach of this thesis was combining the science of IC CMP and silicon processing and introducing novel technologies like the fixed abrasive pads to bring the CMP process closer to the requirements of the MEMS technology. With this development structures beyond today's possibilities are enabled as well as individual substrates, which can be customized for their use and which provide superior uniformity and thickness control.

1.3 Facilities, Equipment, Methods and Material

This work was performed at Micronova, the microelectronic laboratory of VTT. It provides one of the largest clean room facilities available in Northern Europe along with state-of-the-art process equipment for grinding (Strasbaugh 7 AF), polishing (Strasbaugh 6DS-SP), post-CMP cleaning (Contrade Corwet 200) and bonding (Electronic Visions EV801). Furthermore all necessary equipment is available to perform both CMOS (Complementary metal oxide silicon field effect transistor technology) and MEMS manufacturing. VTT Micronova is involved in multiple national Finnish and international research programs as well as in small and medium scale production of different IC and MEMS devices. Furthermore it provides clean room and office space as well as rentable tool time and professional operating services for a group of start-up companies. IC compatible tool sets for CMOS manufacturing down to 0.4 µm are available as well as several processing units including grinding, CMP and post-CMP cleaning are compatible for up to 200 mm wafer size. The work contributing to this thesis however was mainly performed on 100 mm and 150 mm wafers as these are the typical wafer sizes being used for the current MEMS manufacturing.

The laboratory has available all major industrial standard analysis equipment as well as special research tools in-house, including AFM (atomic force microscopy), SAM (Scanning acoustic microscopy), SEM (Scanning electron microscopy), capacitive wafer thickness gage (“ADE”), profilometry (“DEKTAK”) and several film thickness measurement tools including reflectometry and ellipsometry.

1.4 Summary of the Papers

Paper A reports the first time use of experimental FA pads for polishing silicon and also thick-film SOI substrates. Material removal rate (MRR) estimation and dependencies on various process parameters are discussed and the general mechanism of FA versus conventional slurry-based CMP is compared.

Paper B continues the research efforts by describing the further development of the process including base line studies and FA pad investigation under long term use. The effective grindline removal is discussed, connecting the FA process to the preceding grinding step for thick-film SOI wafer formation.

Paper C concludes the preceding Papers A and B with the development of a feasible industrial process sequence by use of low sub-surface damage (SSD) grinding and FA CMP. Further base line studies and crystal damage analysis corroborate the full compatibility of the sequence for reaching prime wafer surface quality on thick-film SOI wafers. Along with highly improved surface flatness and thickness control cut in half material removal enhances the throughput.

Paper D describes the chances and challenges of implementing CMP into MEMS processing. With the use of FA pads on patterned MEMS structures close to ideal results are presented, in terms of pattern conservation and surface roughness. The differences between FA and slurry-based CMP are explained.

Paper E describes the benefits for piezoelectric films grown on polished oxides for the formation of FBAR (Film bulk acoustic resonator) filters with high Q-values. Because of conventional CMP processing however, rounding of the acoustic mirrors occurs, which is one of the discussed items as well as the defects in the polished film after CMP, exposed by the wet-chemical cleaning.

Paper F presents CMP as enabling technology for smoothing thick polysilicon layers. By developing a customized process solution, low temperature (LT) bonding is enabled and successfully demonstrated. This in turn opens new capabilities in design and manufacturing of MEMS devices utilizing polysilicon.

2. CMP Technology

In this chapter the technology of chemical mechanical polishing will be briefly explained, mainly presenting the general mechanism and recent developments with emphasis on the fixed abrasive pad technology as it is widely used in the scope of this work. Profound discussion of the CMP process, its mechanics and chemistry can be found in many publications [e.g. 21]. To introduce the FA technology and to connect to the MEMS area the typical characteristics of conventional slurry-based CMP are discussed and related to the actual situation in micromechanical systems. Furthermore, especially the mechanism of removal in oxide and silicon polishing is presented as they have high relevance for this work.

2.1 The CMP Process

The general schematic of a CMP process is shown in Figure 1. The wafer to be polished is held upside down by the rotating carrier chuck. Its backside is protected from damage by a soft insert felt (mounting pad). Polishing occurs usually on a micro-porous cloth made from polyurethane, which is glue-mounted to the polishing table.

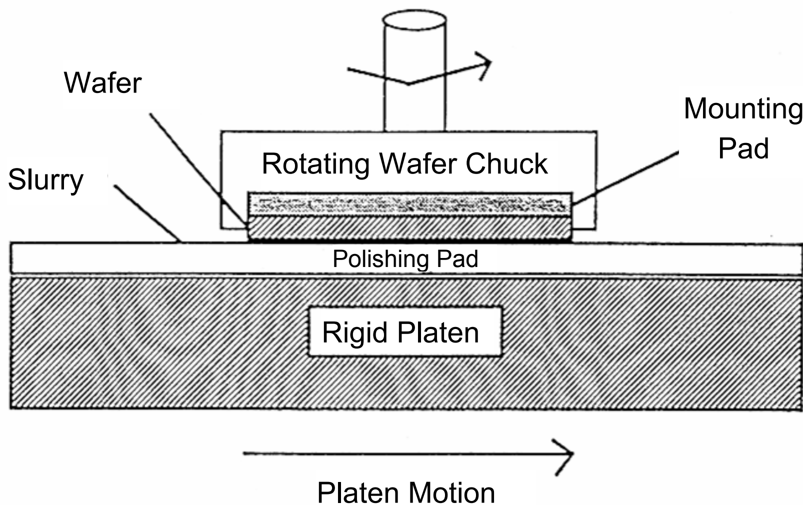


Figure 1. General Schematics of the CMP Process [22]

During processing the polishing liquid (slurry), containing abrasive particles and chemistry in aqueous dilution, is dispensed under particular dosing onto the pad. Rotational speed of the platen and chuck are as well controlled as are the applied downforce of the carrier on the platen and the processing time. Additionally, air back pressure can be present either in zones or at the entire backside of the wafer to enhance the overall uniformity control of the process. Often, the carrier oscillates laterally on the table to maximize the utilization of the polishing pad and to improve the slurry flow under the substrate.

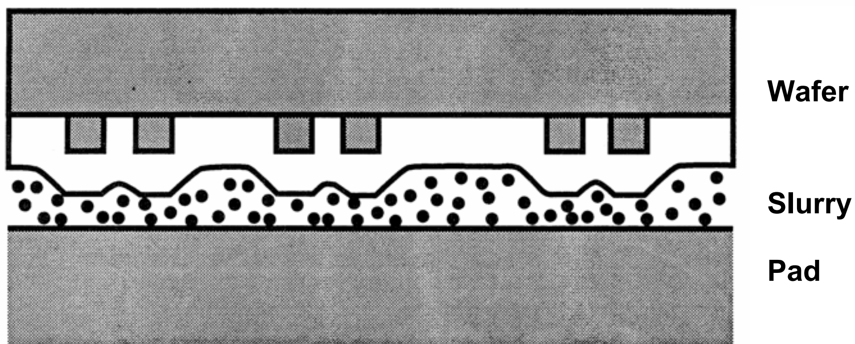


Figure 2. Schematic view of the Pad-Slurry-Wafer Interface [23]

Depending on the above mentioned macroscopic process parameters and other input variables like slurry flow, its viscosity and composition and especially its conjunction with the mechanical properties of the applied polishing pad, different regimes of polishing conditions are present at the pad-slurry-wafer system (Figure 2). The tribological conditions of the CMP process in this aspect have been studied extensively and a variety of modelling work has been done [24, 25, 26, 27, 28]. It is the concerted action of the microscopic asperities of the polishing pad with the nanoscale abrasive particles in the slurry, which defines the removal of material. Being either accelerated by the asperities and impinging the wafers' surface or being dragged between the asperity and wafer the particles act as the weakener of the surface layer or plough away the atomic clusters of the film. This in turn reflects to the material removal rate (MRR) and the created surface quality as well as the uniformity of removal.

Especially Phillipossian et al. have been able to gain fundamental understanding of these different contact modes by investigating the coefficient of friction (COF) directly with a special apparatus, thus enabling its in-situ measurement [29, 30, 33]. The COF is defined by the ratio of the shear force F_{shear} and the normal force F_{normal} being applied to a surface (Eq. 1).

$$COF = \frac{F_{shear}}{F_{normal}} \tag{1}$$

Different pads as well as slurry types have been investigated and the influence of the pattern structure has been included in their studies [31]. To visualize the findings in dependency of CMP-specific parameters the Sommerfeld number So is being introduced:

$$So = \frac{\mu U}{p \delta} \tag{2}$$

In the above equation μ is the slurry viscosity, U the relative pad velocity; p is the applied pressure and δ the effective fluid layer thickness between pad and wafer. The result can be plotted as a so-called Stribeck curve diagram, of which a general version is presented in Figure 3. Based upon the Sommerfeld number and the region of COF one can obtain the different regimes of lubrication, namely the hydrodynamic, partial and boundary lubrication area according to Ludema's definition [32].

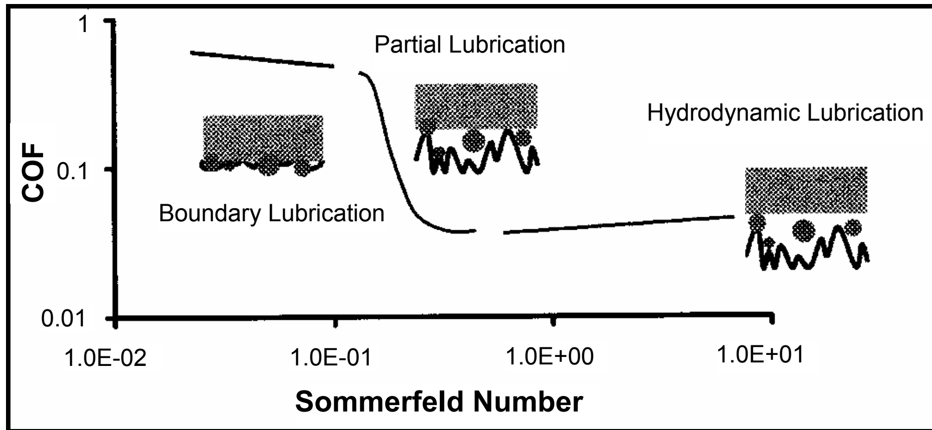


Figure 3. The Stribeck curve based on COF and Sommerfeld number with the indicated three different regimes of lubrication [33]

By this tribological investigation the COF has been re-connected to the Preston's coefficient K_P, (see Eq. (5), p. 25) included in the very first mathematical approach of describing the dependency of MRR to process parameters [1]. Depending on the lubrication regime, predictions can be made about how the polishing process performs in the respect of MRR, non-uniformity (NU) and planarization capability. This approach can be generally utilized in analysing any kind of CMP process based on conventional pads and slurries.

2.2 Oxide CMP

One of the most widely studied processes in the area of CMP is the polishing mechanism of silicon dioxide. Since the roots of this CMP steps are coming from the polishing of glass substrates, some fundamental understanding was available together with a lot of experience, when research started. The details of the studies can be found in [34]. The basic mechanism was adapted from glass polishing, where the softening effect of water as it penetrates into glass was reported already earlier [35]. Landis and Burke et al. developed this idea, when reporting about the integration of CMP into CMOS IC manufacturing in 1992 [36]. The general mechanism is described by the following reaction equation:

$$= \bar{\ } Si - O - Si \bar{\ } + H_2O \Leftrightarrow 2 - Si - OH + 2e^- \quad (3)$$

Water penetrates into the oxide network breaking the Si-O bonds to form single Si-OH links. The hydration of the Si-O bond occurs especially near the surface and $Si(OH)_4$ (silanol) is formed:

$$(SiO_2)_X + 2H_2O \Leftrightarrow (SiO_2)_{X-1} + Si(OH)_4 \quad (4)$$

This in turn is soluble in water at elevated pH-values of about 10 and can be dissolved. The compressive stress caused by the presence of the abrasive particles enhances the reaction during the mechanical polishing action [37].

A further enhancement of this mechanism is provided by chemically active abrasive particles. Whereas silica was often used as a suitable abrasive for glass polishing, it was found that using ceria as abrading material the MRR increased drastically. Cook suggests this effect being due to the so-called chemical tooth effect of ceria abrasives. He presents a model giving raise to increased removal based on the gain of free energy during the formation process of ceria-based components under polishing [38].

In general oxide CMP has a very similar mechanism like glass polishing. Thus the MRR can be described by the input variables velocity (V) and downforce (P) in Prestonian type [1]:

$$MRR = K_P PV, \quad K_P = \text{the Preston coefficient} \quad (5)$$

This concept is widely used and based on Eq. (5) further and more detailed studies were undertaken to model the process more accurately. This led to more precise forms of Eq. (5) and to the elucidation of the content of the Preston coefficient. A good summary of the evolution of the Preston equation can be found in [39].

2.3 Silicon CMP

In the semiconductor area, the importance of silicon polishing has been growing since the very beginning. After formation of the raw wafers by crystal growth, slicing, lapping and etching, a suitable procedure was needed to improve the surface quality and to remove all remaining crystalline damage. Besides solutions with purely mechanical character, the use of the chemical mechanical concept was adopted quite early as mentioned in Chapter 1.1. Mendel suggested in 1967 the use of colloidal silica in alkaline solution on soft planar pads for the stock removal polish [40]. This has since been the usual approach for this step.

However, only few sources can be found, were the actual mechanism of removal has been discussed. Major work has been done by Pietsch et al. who also developed a model for the mechanism. It took him extensive analysis by IR (infra-red) spectroscopy to find a suitable approach for observing the changes, which are occurring at the silicon surface during polishing. Schnegg et al. had already suggested earlier, that the highly hydrophobic surface after polishing was due to hydrogen termination at the surface [41] and this was finally proved by Pietsch, when applying FTIR (Fourier transform infrared spectroscopy) analysis on Si(111) surfaces directly after polishing [42]. The work was then intensified and also Si(100) was investigated [43]. The results show a strong dependency on both the density of abrasive particles, which in this case were of silica type, and the pH-value of the applied polishing slurry. This in turn led to the conclusion that OH^- molecules are the instrument of the silicon etching process under CMP and that they are also consumed as buffering of hydroxides increased the MRR. The silica abrasives are necessary as transporters and transmitters in this process. Dependent on the pH-regime two different models were suggested. Highest removal rates were achieved at around pH 11. The silicon surface is highly hydrophobic and analysis indicated a predominant surface termination by silicon hydrates. An explanation for this scenario is the direct weakening of the Si-Si backbonds as a result of a strong polarization by the ambient OH^- molecules at exposed areas such as atomic steps or defects (subsurface oxide formation). Then ambient H_2O or O_2 dissolved in the slurry directly break the weakened bonds to form either monohydrates (see Eq. 6) or an internal oxide bridge (Eq. 7).

$$Si - Si + H_2O \Rightarrow Si - H + HO - Si \quad (6)$$

$$Si - Si + O \Rightarrow Si - O - Si \quad (7)$$

Dissolution by mechanical abrasion then occurs depending on the “mix” of neighbouring attacked bonds as monomeric, dimeric or trimeric silica as well as complete silanol. During the complete removal process the hydrogen termination of the attacked surface site stays intact, thus the surface is hydrophobic at all times.

Outside this pH-regime, at a much higher pH but also under acidic conditions, predominate surface termination is represented by direct silanol formation at the surface. The hydrogen is replaced by OH^- molecules as a first step. This in turn leads to a more hydrophilic surface. This now allows the ambient water or dissolved oxygen to enter the surface and the rest of the mechanism is, as described above by Eqs. (6) and (7), leading to the oligomeric dissolution of the silica species. Under the standard polishing conditions this slows down the removal as a quartz-like surface net-work has to be removed by mainly mechanical means of the CMP process as discussed in Chapter 2.2 [41, 44]. The particle concentration however, is usually much lower in silicon processing than it is in standard oxide CMP and therefore this regime is inferior to silicon CMP.

2.4 Characteristics of Conventional CMP

The general aim in using CMP is to remove excess material or to planarize surface films. In case of planarization the mechanism is based on the fact, that elevated structures of a pattern face a locally increased polishing pressure over the lower laying areas of the wafer. Due to the Prestonian dependency described earlier by Eq. (5) the removal rate is higher in those up areas and planarization occurs [45]. Slurry based CMP with polishing pads of different kind show particular characteristics in this respect. Due to those characteristics the process engineers face several challenges concerning the planarization capabilities and uniformity of the process. It is evident, that for aiming at the best possible surface smoothness a softer pad and less chemically aggressive slurry should be used. As optimum planarization is required a hard pad should be considered in order to maximize the removal at the elevated pattern features. For the overall

wafer uniformity of removal however, a soft pad would yield best results. The usual compromise for this conflict is often to use a stacked pad for planarization issues with a hard pad on top performing the planarization and with a soft underlying pad to even out and level the wafer during the process. This however leads to NU, especially at the wafer edge.

Another aspect of the planarization evolution is that it is strongly dependent on the pattern width, its density and the total amount of material removal. To describe the efficiency of the planarization process it is therefore convenient to introduce the step height reduction SHR:

$$SHR = \frac{step\ height_{before\ CMP} - step\ height_{after\ CMP}}{step\ height_{before\ CMP}} \quad (8)$$

Using conventional slurry based CMP solutions it is well known that the SHR is decreasing with increasing line width (LW) and increasing with increased material removal. The below figure describes this effect generally.

The different curves in the diagram of Figure 4 represent the remaining step heights for different pattern widths in dependency of the polishing time. As the pattern width is increasing, it takes much longer to get a full step height reduction or planarity. On die level this results in the necessity of over polishing to make sure that the even the largest pattern is totally planarized. This in turn leads to the fact that small features, which are already planarized, face additional removal and effects like dishing and erosion occur (see also Figure 9 on page 32).

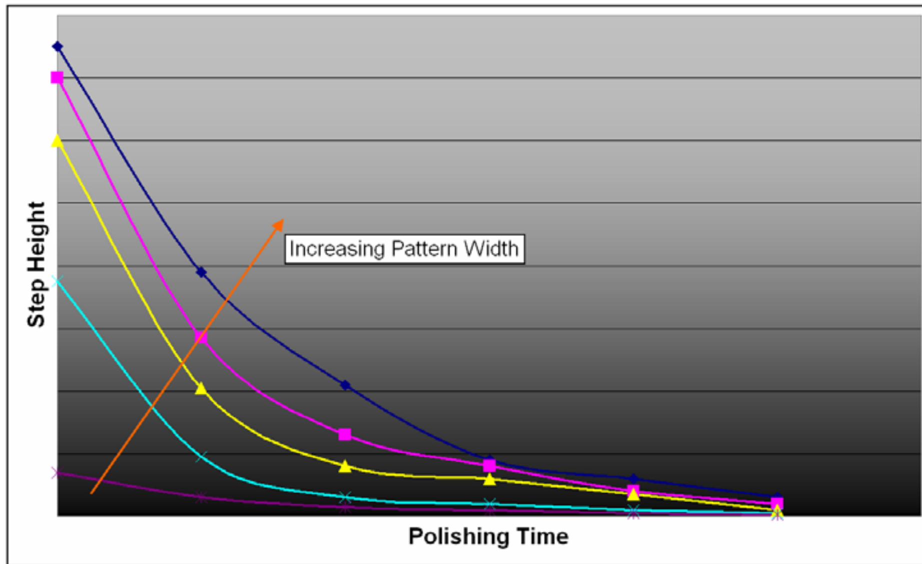


Figure 4. Reduction of the step height with increasing polishing time and material removal. Larger pattern width faces slower SHR

Therefore, planarization by polishing has been from the beginning the object of many modelling trials and investigations in order to understand, improve and overcome the problematic behaviour of this process. The bending of the pad under the presence of topography was modelled by Sivaram [46]. This is one aspect of the problem and has to be considered together with other circumstances like e.g. the presence and properties of a liquid film, which led to the model of Runnels [47], introducing fluid based wear. Warnock directly used the pads' compression to model and predict planarity [48]. Figure 5 depicts the bent polishing pad during process at the presence of a patterned wafer. Due to the pads' relaxation it surrounds the features to be planarized. The very same effect occurs also at the wafer edge, where the pad transits from the substrate to the retainer ring. The gap between ring and wafer as well as the height difference of ring and wafer surface leads to relaxation effects in the pad causing uniformity issues at the outer edge. Further development and understanding of the first models of the early nineties was therefore constantly achieved and they got finer and more accurate. Non ideal conditions are nowadays integrated [49] in comfortable software-tools and the different tribological aspects of the process are included in the considerations [28].

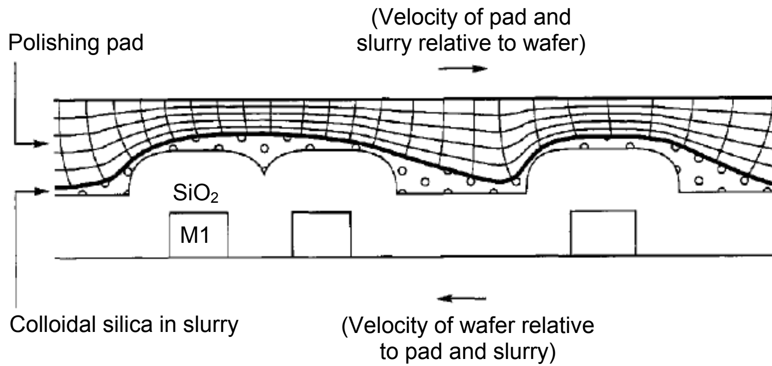


Figure 5. Pad bending under presence of topography. At elevated areas higher pressure is applied through the compression of the pad [9]

One way to prevent high NU due to the pad effect at the wafer edge was followed by the tool vendors, who have been e.g. inventing the pneumatically adjustable retainer ring. An extra force by the retainer ring is applied outside around the wafer and this pre-compresses the pad. The edge effect, caused by the time dependent relaxation of the polishing pad can be minimized by the optimization of this pressure (Figure 6). It has to be considered that the type of pad and the process parameters itself influence the edge effect to large extent and therefore also pad vendors aim at all times towards better pad technology with higher production consistency and process control.

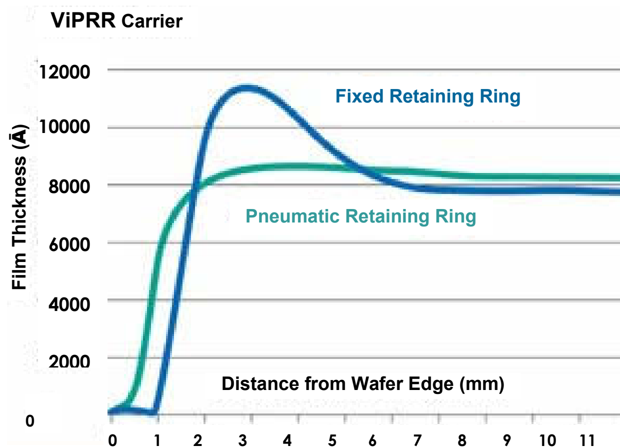


Figure 6. Comparison of the remaining wafer edge profile after CMP. By use of a pneumatically driven retainer ring the edge effect can be minimized [50]

With zoned backpressure at the backside of the wafer, bending can also be applied on the wafer itself to overcome uniformity problems originating from pad and rotation. The more holes are present inside the carrier and the more zones are available the finer a bending can be adjusted to the polished sample (Figure 7) and the better the process can be controlled in terms of non-uniformity.

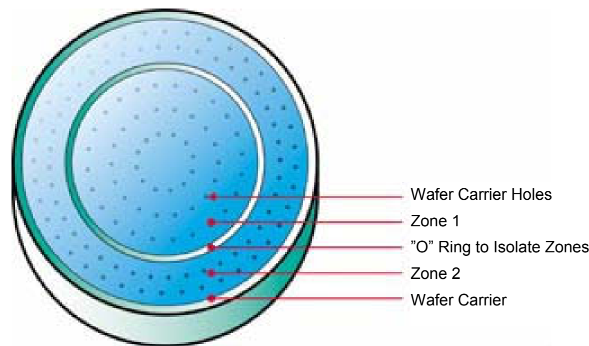


Figure 7. Schematic drawing of a wafer carrier with many backside pressure holes and two independent pressure zones for controlled wafer bending under CMP [50]

The general mechanism of the slurry-based planarizing process however is the attack of the pattern at its corners and its proceeding towards the centre of the elevation as polishing time continues. Thus the pattern is firstly rounded at its corners and then continuously planarized with evolving polishing time. Simultaneously, the down areas of the pattern are also subject to substantial removal, which in turn increases the required thickness of the film to be removed for planarization. The polishing of a single free standing step has been well described by Patrick et al. and is depicted in Figure 8 [45].

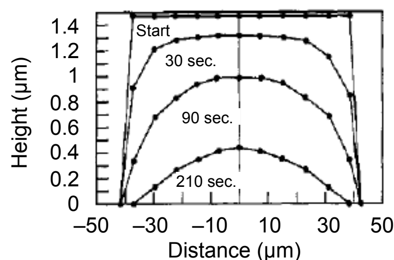


Figure 8. The evolution of the pattern of a wide step under planarization. Attack starts at the edge of the features and proceeds under continuous rounding of the step [45]

Not included in the above figure is the simultaneous removal of material in the open field areas, which would even more clarify the uniformity issue. Due to this behaviour features get ever more flat but never vanish totally, as the removal rate on top of the pattern also erodes with decreasing height difference. Therefore a good amount of total material removal is required in general in order to achieve sufficient planarity, especially with the widely varying pitch of pattern size and density in modern IC circuitry (see also the above Figure 4).

In most of the recent applications however it is the removal of excess material on top of a stop layer that is required, when CMP is used; for example at FEOL processing for STI formation [51] or the dual damascene process for the metallization BEOL [52]. The above discussed mechanical properties of the polishing pad are of especial high importance in these cases. When polishing the deposited metal layer to form interconnects, the process has to be well controlled and stop on the ILD (Inter layer dielectric). As the pattern density and feature shape varies, a certain amount of overpolishing is required in order to clear all the metal and to avoid shorts in the circuitry. Polishing rates are different for the different pattern densities and widths on the die and the process tends to abrade also ILD material by purely mechanical means on small features, which is called erosion. Comparably wide metal lines on the other hand face a removal of material after their clearance during the over polish time and are washed out in the centre, which is called the dishing effect (see Figure 9).

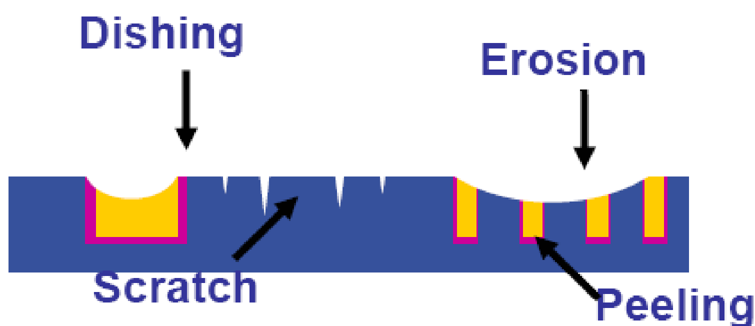


Figure 9. Schematic view of dishing and erosion amongst other defects like scratching [53]

In case of the STI process, shallow trenches have been etched in the bulk silicon and the oxide fills the trenches to isolate the transistors from each others. The CMP process has to remove the excess oxide around the trenches and should stop exactly on top of the masking nitride. It is however difficult to avoid simultaneous nitride removal during planarization due to similar removal behaviour. In order to overcome these problems a lot of different approaches have been undertaken; among others the development of high selectivity (HSS)-slurries [54] or abrasive free slurries [17], but also new design rules have been adopted for better process results. For example by implementing dummy structures [55] or adding additional features by reverse mask processing [56] the maximum step height prior to CMP has been reduced. Also totally new CMP process developments have been undertaken, like for example the development of fixed abrasive (FA) pads.

2.5 Characteristics and Technology of Fixed Abrasive Pads

Especially the STI process requires a well adjusted CMP process, which often has to be monitored by in-situ measurement to prevent oxide and nitride loss [57]. A new approach for this delicate process was introduced by 3M in the mid-end nineties, when they presented their fixed abrasive pads. The polishing pad features a micro-replicated layer of composites with a diameter of some hundred micrometers and height of about 40 micrometers (see also Figure 10). The shape is varying depending on the application and the resin binder holding the abrasive particles (e.g. CeO_2) can be adjusted in its hardness for process purposes as well. The abrading particles are thus bound inside the pad and instead of slurry only pH-value adjusted DIW is necessary as a lubrication liquid, which is fed onto the pad during processing. The composites wear off slowly during polishing and due to the presence of the applied pattern feature fresh abrasives are exposed at all times. The design of the pad allows a good lubrication with the fluid and polishing debris can be swept away easy during the process as wide channels are existing on the pad in between the micro replicated posts. After a slow start FA CMP pads are nowadays well accepted in the industry and further development has brought down starting issues with defects due to scratching to state-of-the-art level and even below. Due to the remarkable benefits of FA pads in terms of Planarization STI processes have been developed at the 65 nm node level [58].

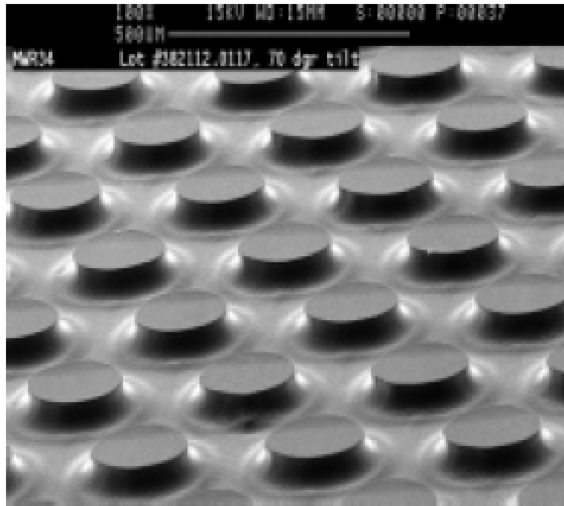


Figure 10. SEM photograph of a 3M fixed abrasive pad. This sample has a micro-replicated composite in cylinder form [59]

In the IC industry the most recent form of using this type pad is in web-roll based polishers. The pad is supplied in rolls and indexed after each run for a certain length, so that each wafer is exposed to an equally used pad surface (Figure 11). With a complete web roll many thousand wafers can be processed without the typically necessary pad change. The FA web rolls are available in different types of pattern according to the specification of the process.

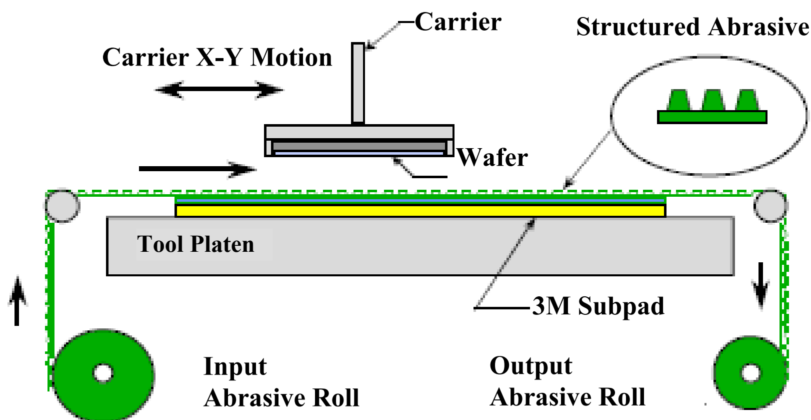


Figure 11. The schematic view of a web-roll based polishing tool [59]

Analysing the mechanism of removal by FA CMP one has to consider the pad-“slurry”-wafer system as done in Chapter 2.1 for slurry-based CMP. The tribology of the fixed abrasive-wafer system is of other nature being depicted in Figure 12, where the conventional, slurry-based CMP and FA pad-slurry-wafer systems are compared. Assuming, that the preferred hydrodynamic lubrication regime for the slurry-based CMP process is present the abrasion mechanism is driven by a 3-body contact mode. In the case of FA pad use however, the surface of the polished substrate is abraded via a 2-body contact mode. The active abrasive particles are fixed in their position inside or on top of the micro-replicated composite respectively.

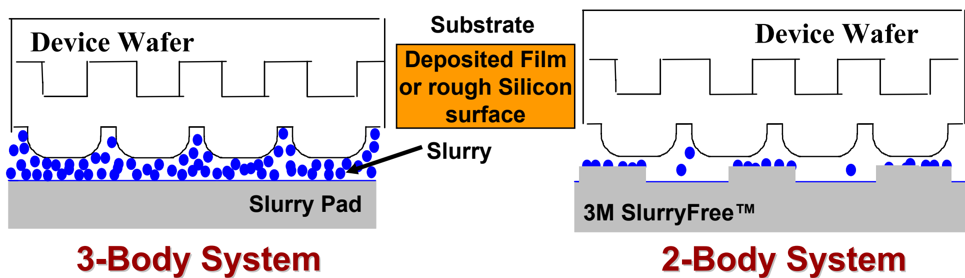


Figure 12. Schematic view of slurry-based and FA CMP, the picture is not to scale [Paper A]

The principle advantage of the FA process is evident; as abrasive particles are positioned at the top of the rather stiff composites of the pad they are mainly active in abrading the elevated parts of the applied wafer surface. The planarization is more efficient than in the case of slurry-based polishing, where the freely moving conventional slurry particles impinging also the lower areas of the die (left in Figure 12).

A sketch of the FA STI polishing is given in Figure 13. The scale does not match all cases of the reality but the figure gives a good idea of the novel CMP step. One composite of the pad is in contact with the top of a large area of the pattern on the wafer surface and does not bend around single features, as in the case of conventional processing with a compressing polishing pad (see Figure 5 in Chapter 2.4).

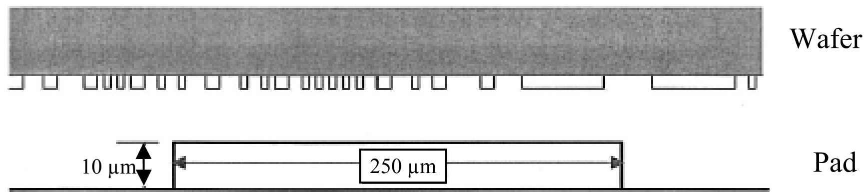


Figure 13. Situation during STI polishing with FA CMP. One composite of the pad is in contact with a large part of the die [60]

The discussion about the evolution of the planarization in Chapter 2.4 does not match in case of FA polishing. The removal is strongly preferential at the top of the pattern and evidently much less rounding of the features is generated due to the shape of the mechanical active posts. Further the removal at the down areas is obviously much lower as the single stiff composites do not approach this area very well and thus erosion is minimized. The planarizing effect of FA CMP is therefore much higher than in case of conventional CMP. Figure 14 shows a comparison for large pattern planarization of STI structures versus field oxide removal.

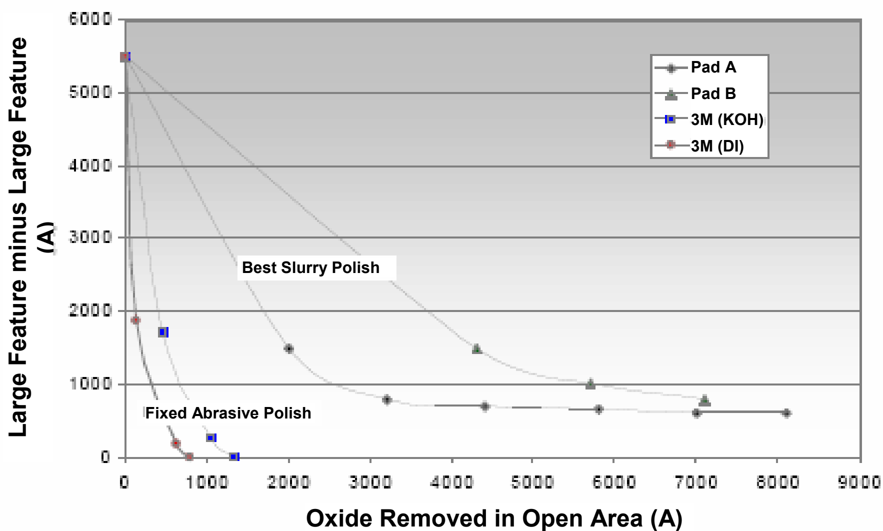


Figure 14. Comparison of large pattern removal efficiency for slurry based and FA CMP. The planarizing effect is strongly enhanced for the fixed abrasive [61]

While the best slurry process leaves a residual step height of about 700Å between small and large features, even when as much as 6000Å of field oxide are removed, the FA is able to remove the pattern completely without thinning the field oxide much more than 1000Å [61].

Another positive effect of the highly reduced bending of FA pads comparing to conventional pads is better overall uniformity around large pattern areas and at the wafer edge. As polishing continues and planarization is achieved, a third positive aspect of the FA technology becomes apparent. As long as there is topography left, the pad will be activated by the pattern and refresh the surface of its composites; the pad is self conditioning. When the pattern however is planarized, no activating topography is left and the pad reacts by reducing the MRR as no fresh abrasive is exposed. The process leads therefore to almost complete planarization when compared to conventional CMP were residual step height remains, this allows substantial overpolish without risking the removal of too much material from the field areas; the FA process is self-tuning [62]. This technology is therefore very interesting for damascene processes involving metals especially copper and some promising results have already been achieved [63]. With the close to ideal planarization capability of the FA pad the necessary compromise using very soft sub pads in the pad stack can be overcome and a better WIWNU can be reached, especially at the wafer edge giving possibility to minimize the edge exclusion. With dedicated two-step processing outstanding results were achieved [64]. As the IC technology moves towards 90 and 65 nm nodes the apparent advantages have been further raising the interest of using the fixed abrasive technology. Due to these results it became apparent that the FA pads could be used also for substrate polishing, especially on thick-film SOI or on large pattern features utilized in several MEMS designs.

3. Formation of Thick-Film SOI Substrates

This chapter is dedicated to the manufacturing process of thick-film SOI wafers. These wafers are of increasing importance for the MEMS industry as they provide convenient processing capabilities. The buried oxide underneath a customized SOI-layer thickness can be used e.g. as sacrificial layer to etch free bulk micromachined features in the top layer [65]. This saves additional process steps and often enables more sophisticated structures. After describing the general approach of the manufacturing sequence, the problems of keeping pace with the increasing demands on the accuracy of the SOI layers will be contrasted to the conventional formation process. With the work presented in the Papers A, B and C a new approach has been developed, which shows highly improved results. Production related issues like throughput are discussed in order to provide a suitable alternative for the current production process.

3.1 The Thick-Film SOI Manufacturing Sequence

For advanced MEMS device formation it is often useful to start with an SOI wafer instead of standard silicon substrate. In contrast to the IC world these SOI wafers do not only require a much thicker SOI film in general but demand also varying thicknesses of both the silicon- and oxide layer. However, the often used Smart-Cut™ technology, invented by Bruel [66, 67] can only be utilized for SOI layers up to about 1,5 µm thickness. The layer cleaving hydrogen implantation cannot be driven deeper inside the bulk silicon of the bonded device wafer. Besides the possibility to grow epitaxially silicon on top of the smart cut layer, which is getting too expensive with increasing thickness often a more mechanical approach is used to manufacture these thick-film SOI wafers, by grinding and polishing the device layer to the desired thickness level.

To gain good results, often two double-side polished (DSP) wafers are used to begin with. The DSP process provides wafers with best possible flatness, often far below 0.5 µm TTV. Then, the oxide layer with customized thickness is grown thermally on the handle wafer. By fusion bonding and annealing the two wafers are connected to form a wafer stack. To avoid chipping during thinning of the device layer, an edge grinding step is introduced to remove the outer edge of the upper wafer, where the bonding is not solid due to the rounded shape of

the substrates. This removes about 2 mm from the device wafers diameter, but leaves a defined edge for the thinning process by mechanical grinding with high speed diamond wheels. Typically a two step process is performed as standard. The coarse step uses wheels with larger diamond particles of around 40 µm and is followed by fine grinding with smaller diamond particles. The abrasives in the wheel can be bond by different ways to form the cutting teeth. The major techniques are the very solid ceramic-like vitrified bond and the softer resin bond, which allows are wide area of adjustment for the cutting teeth strength. Generally the grinding process leaves a very flat surface and a mirror-like finish, however including residual grind lines, which are swirl-shaped from wafer centre to edge (see also Figure 25 on the left in Chapter 3.3). Besides this type of topography, SSD (sub surface damage) is introduced propagating typically some 6 to 8 µm deep into the substrate.

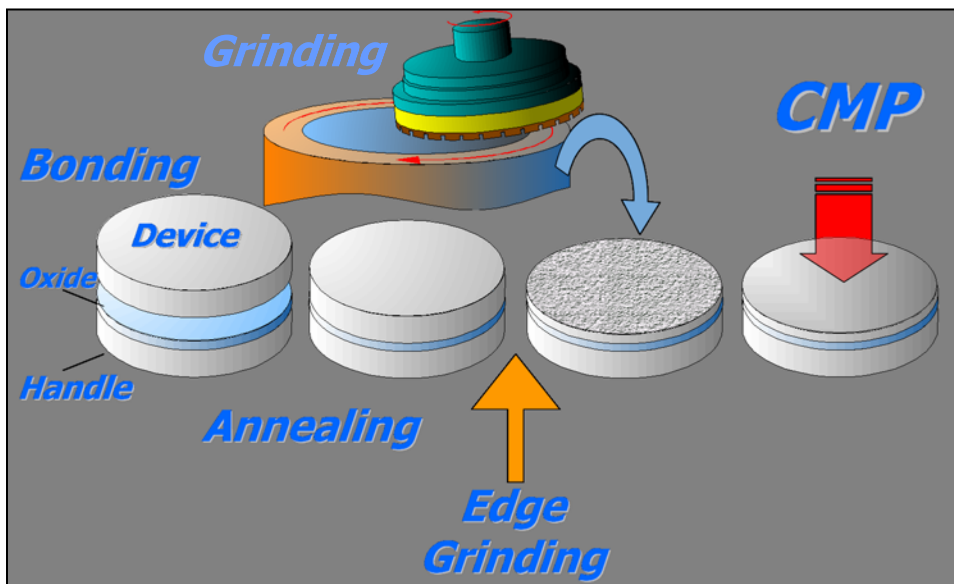


Figure 15. Manufacturing sequence for thick-film SOI Wafers

Removal of this damage layer is done with a sequence of stock removal and fine polishing by CMP. The surface is simultaneously finished to prime wafer quality, removing all grind lines and leaving a planar surface. The entire sequence is shown above in Figure 15.

3.2 The Sub-Surface Damage Layer

The crystalline damage induced by mechanical grinding has been studied by Haapalinna et al. [68]. Figure 16 depicts the different depths of the induced damage, suggested by Hadamovsky [69].

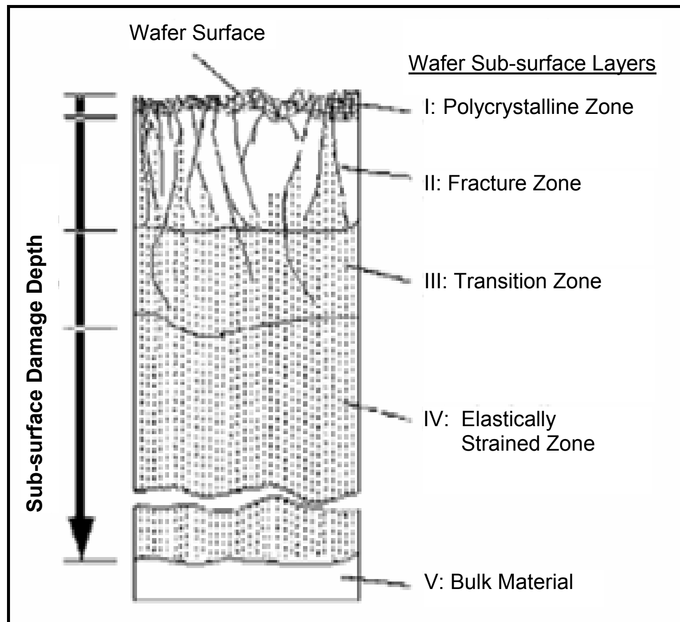


Figure 16. Schematic view of the induced SSD by mechanical grinding [69]

Starting from the wafer surface, which is strongly degenerated, so that Hadamovsky speaks of the polycrystalline zone (I in Figure 16), the big cracks propagate through the fracture zone (II) into the transition zone (III). Still some stress is present in the following elastically strained zone (IV) before finally getting into the bulk material (V) with no further damage. The total depth of the damaged zones and the thickness of each single layer are strongly dependent on the grinding process being applied to the wafer. With state-of-the-art processing, the depth of the total damage stack is about 6 to 8 µm.

Grinding typically results in very flat surfaces but the necessary CMP steps to remove the above characterized damage can often degenerate the flatness. For best performance in terms of uniformity it is evident that one has to minimize

the required polishing removal. Therefore it was very important in this work to investigate the grinding process as well, to achieve best possible flatness for the SOI wafers. Polishing is required as long as damage is left in the ground layer and topography in the form of remaining grind lines is left on the surface. The goal of reducing damage and topography caused by grinding has thus direct impact on the amount of removal required by the CMP process.

Together with the grinding wheel vendor DISCO several approaches were made to improve the SSD performance of the fine grinding step. With the use of smaller diamonds the damage due to the cut would naturally be reduced, but also the applied down force during cutting for maintaining the fixed feed rate of the process is of great importance. Therefore especially the bond of the diamonds within the cutting teeth of the wheel and its porosity are within the scope of the grinding wheel developers. All tested wheels were of resin-type bond and could therefore be adjusted well according to the special needs. On the other hand the lifetime of the wheel is very important for the cost of the process and has to be in balance with a simultaneously soft enough bond to maintain a suitable surface renewal at decent down force for low SSD. For investigating the depth of damage, one has to make it visible at the surface of the wafer, so that it can be detected by inspection either optically or by scanning tools.

One means of detection is the decoration of faults by an oxidation, annealing and etching sequence [70] with the so-called oxidation induced stacking fault (OISF) method. After grinding the wafer, material is removed stepwise by conventional polishing. The OISF are counted after their decoration and drawn up versus the material removal. In Figure 17 the defect counts of standard grinding wheels (right) are compared to those of newly developed grinding wheels (left in Figure 17). As can be seen the new wheels are capable of keeping the SSD at around 3 to 4 μm. These wafers would require much less CMP removal in order to reach the reference level of defects of the compared standard wheels. The polishing time after grinding with the newly developed wheels can therefore be reduced.

The use of improved fine grinding wheels for reduced polishing removal was suggested from the beginning of the investigation [Paper A] and was further studied. The base line studies the Papers B and C showed that the newly introduced process was stable and provided tightly controllable device layer thickness as well as good TTV values of about 0.5 μm.

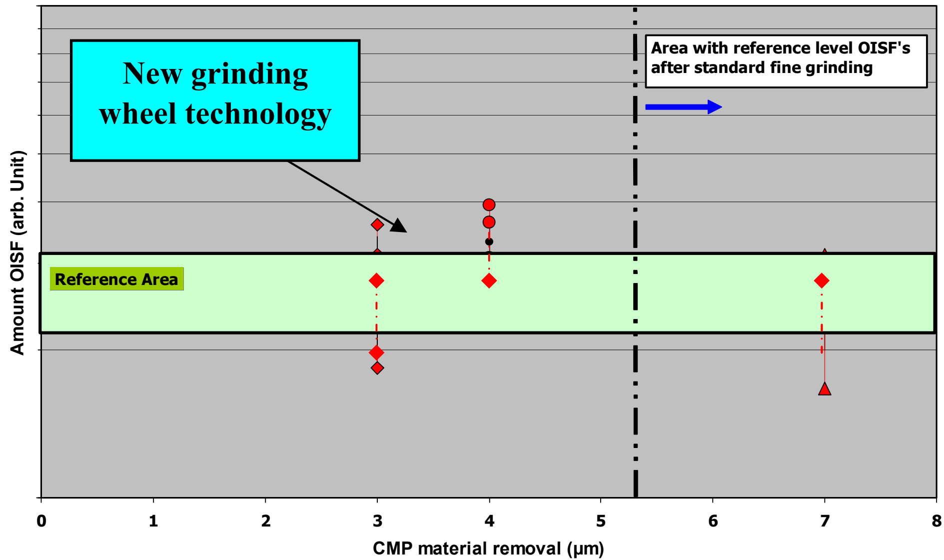


Figure 17. Comparison of OISF counts after CMP polishing on ground wafers with different fine grinding wheels. The wheels on the left show comparable defect level counts after significantly reduced polishing removal

3.3 Uniformity of Silicon CMP

The polishing sequence of the ground wafers is divided into several steps. At first the majority of material is removed by the stock removal polishing. As this step normally removes about 5 to 7 µm it is therefore the most critical in terms of TTV degeneration. The following fine polishing step smoothes the surface down to Å-level and evens out the remaining roughness from the more aggressive stock polish. The typical removal of the fine polishing step is around 0.5 to 1 µm, thus it is not very critical in terms of TTV degeneration. The haze polish then removes the atomic roughness and leads to sub-Å level roughness; this leads to prime wafer surface quality. The removal is very low, usually some tens of nanometres.

With the standard silicon polishing sequence problems arise in achieving the high specifications for the uniformity of the SOI layer, especially the stock polishing step with its large material removal. As the polished device layer features a smaller diameter than the overall substrate (due to the edge grinding)

the earlier mentioned pad-edge-effect (see Chapter 2.4) leads to strong rounding in the stock removal process. The generated edge roll-off by CMP polishing reaches several millimetres inside the device layer as the gap between the carrier's retainer ring and the polished device layer's surface edge is now even larger than with standard substrates. The high importance of the gap between retainer ring and wafer edge for the TTV performance has been recently investigated again and a new model was developed [71]. The strong influence of the gap size on the wafer edge geometry was reconfirmed and it could be shown that uniformity increases strongly with increasing gap size. The resulting edge shape after conventional processing therefore often precludes meeting the stringent specifications of down to 0.5 µm TTV at edge exclusion of 3mm of the total wafer diameter [Paper A]. This means for the SOI wafers' device layer with its smaller diameter an edge exclusion of about 1 mm is required, a value that is even below the tightest specification for IC wafer manufacturing.

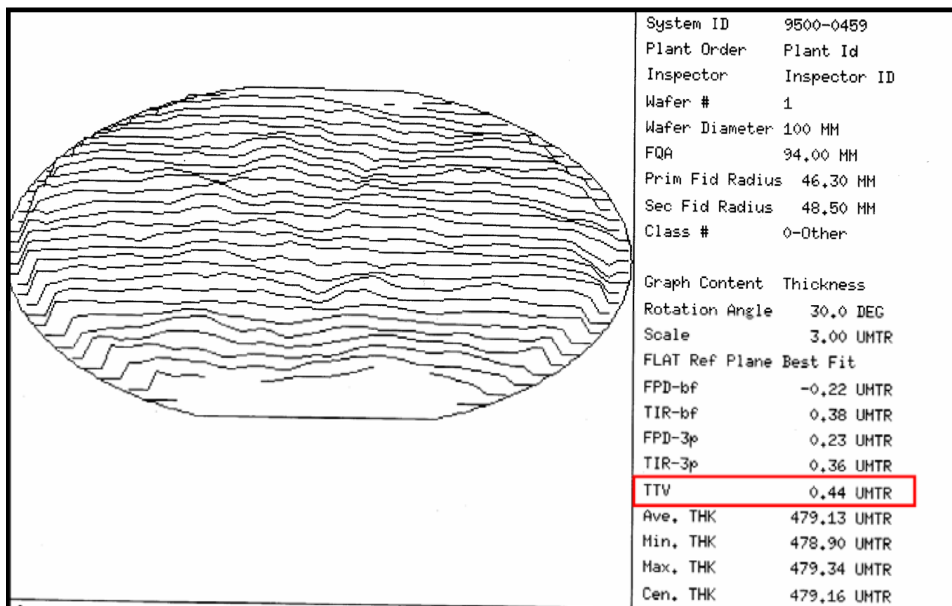


Figure 18. Typical result of a ground SOI wafer. TTV below 0.5 µm indicate very flat surface

Typical results of both states after grinding and after removal of the SSD layer by conventional CMP are shown in Figure 18 and 19 respectively. In this case the total removal by CMP is about 5 µm, which marks the absolute minimum

stock removal needed for taking off all SSD of standard ground SOI wafers. A clear rounding after polishing is visible at the outer wafer edge as well as some additional NU in the centre of the wafer, caused for example by non-optimized backpressure.

The TTV is increased to about 1 µm and the calculated WIWNU (Within-wafer non-uniformity) is about 15 %, based on the k-value, a factor often used in IC-CMP for sensitive evaluation of CMP process non uniformity. The calculation is given by Eq. 9:

$$k\,[\%] = \frac{\Delta - \mathrm{TTV}}{\text{total Removal}}\,\mathrm{X}\,100\,;\ \ \Delta\text{-}\mathrm{TTV} = \mathrm{TTV}_{\text{pre CMP}} - \mathrm{TTV}_{\text{post CMP}} \qquad (9)$$

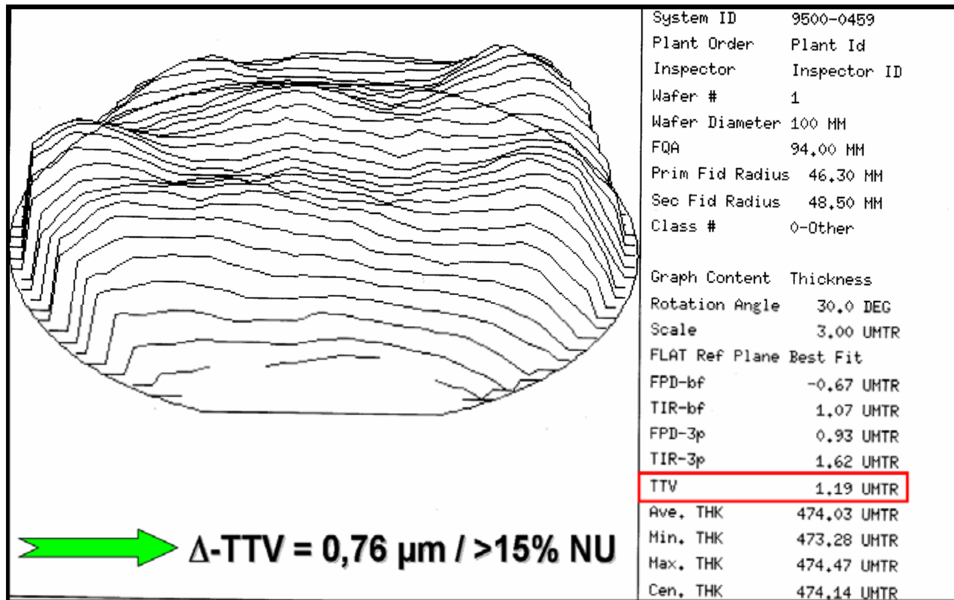


Figure 19. After conventional CMP the rounding of the wafer edge is visible, but also other NU in the wafer centre leads to TTV above 1 µm

Due to its remarkable results in the IC area the idea was born to use FA pads for overcoming the problem with the uniformity at the wafer edge. With a set of prototype FA pads from 3M a new process was set up therefore to investigate its behaviour on silicon.

The first trials of silicon polishing on fixed abrasive pads are depicted in Figure 20. One can see that the TTV change of the process is almost neutral or even improving so that the shape and good flatness of the incoming ground wafer is maintained during FA CMP processing. Even though the total removal of about 1 µm at this early stage was rather small, the calculated WIWNU of the process was around 5% versus about 15% WIWNU with conventional CMP indicating a tremendous advantage for the FA process.

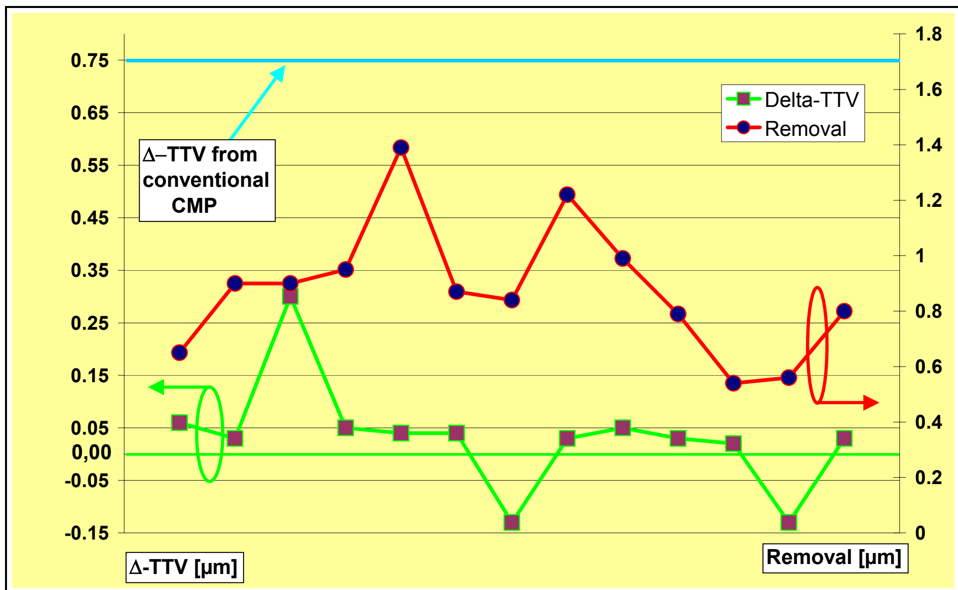


Figure 20. First polishing results of FA CMP on silicon. The TTV behaviour is superior to conventional CMP. The total achieved removal is rather small

To understand more of the mechanism behind the removal, several tests were made, especially with the background of increasing the total achievable removal and improving the MRR. When applying sequential polishing it was discovered that the removal would drop further and also the MRR was going down in the second step, while slightly increasing in the first step [Paper A]. This was connected to the specific removal mechanism of the FA pad, which needs activation of the pattern for its performance. As long as topography is left on the wafers' surface, the abrasive containing posts could get refreshed, but with realized planarization the process stops itself as seen earlier in case of IC device manufacturing [72]. While this effect is highly desired for the STI process, one

would need a pad for SOI polishing that has an effective removal even after topography is no longer present. This so-called zero-rate would ensure the removal of the deeper laying SSD. With this input the vendor supplied a different type of pad to be used with the silicon process. This pad showed an increased MRR with stable uniformity behaviour in the beginning and a higher total removal was achieved. After longer use however, the MRR dropped and could not be recovered. The surface of the pad was analysed by SEM. When inspecting the details of the composites, it was seen that the constant renewal of the surface due to slow wear was working in principle, as the composites' height of the used pad were clearly lower (see Figure 21).

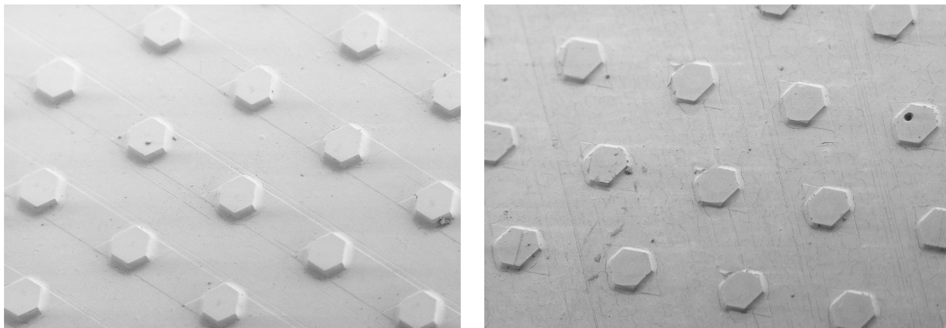


Figure 21. New (left) and used (right) FA pad. The abrasive containing composites are clearly lower after several hours of processing

The used pad however showed a lower density of abrasive particles at the surface of the posts and its topology was smoother. The balance of the abrasive particles wear and their loss with the resin material removal was not well adjusted and led to depletion of particles on the surface. The abrading particles appear as round "balls" in the left picture of Figure 22. Clearly fewer of them are visible on the used pad surface. The overall surface looks clotted (Figure 22 on the right).

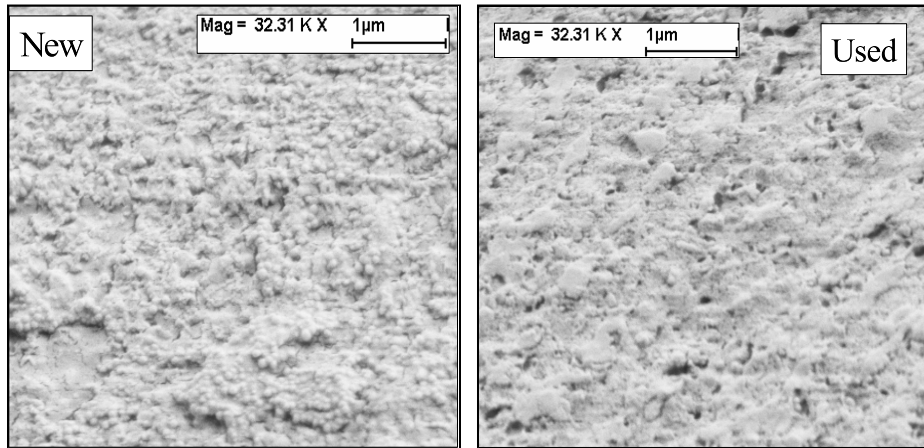


Figure 22. Detailed view on the composites of a new and used FA pad. The unused pad features clearly more abrasive particles (left) than theused one (right) and has a generally higher topology

With another resin-type FA the research was continued and more detailed analysis was done on the influencing parameters of the process. This pad finally showed a stable behaviour on silicon with respect to MRR after grind line topography removal and deeper investigation was enabled.

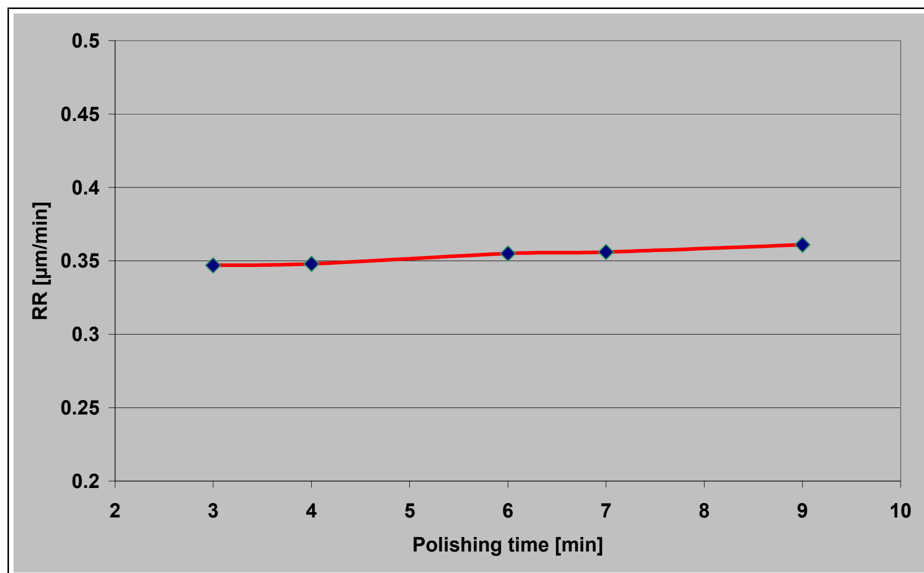


Figure 23. MRR over polishing time. Stable removal of about 0.35 µm/min independent from the applied processing time

The pad continued working after several runs with stable rates and it was possible to adjust the total removal by omly varying the polishing time (Figure 23). Now other influencing parameters were analysed.

Another yet important point to investigate was for example the strong dependence of the MRR on the pH-value of the applied lubrication liquid. With a detailed polishing experiment fine scale pH adjustment was done to the lubrication liquid and the MRR was studied. The removal peaks at pH 11.8, as can be seen from Figure 24. This is very similar to that what has been found in earlier trials on STI oxides [73], rather than on conventional silicon polishing [42, 43]. This finding indicates the special mechanism of removal on the ceria based FA pad for silicon. Ceria is known for its chemical tooth effect when being used for abrading silicon dioxide [38], but no such effect would be expected when removing silicon. According to Pietsch et al. however, a loose quartz-like network is formed on top of the silicon surface, when the polishing takes place at higher pH-regimes. This oxide in turn slows down the conventional polishing process as it is much more difficult to be dissolved by the typically low particle density slurry of the standard silicon CMP. In case of FA CMP however, ceria can act with its chemical activity and enhance the removal as soon as the pH-regime allows the formation of the surface silanol. It is therefore suggested that the removal of silicon by FA pads is supported by the chemically active ceria abrasives, facing an oxide-like surface being formed due to the elevated pH-regime. The silicon removal is thus driven by the surface silanol formation under exchange of the hydrogen by OH^--molecules and the resulting silica dissolution via the Bronsted-base reaction of the chemically active ceria as suggested by Cook [38].

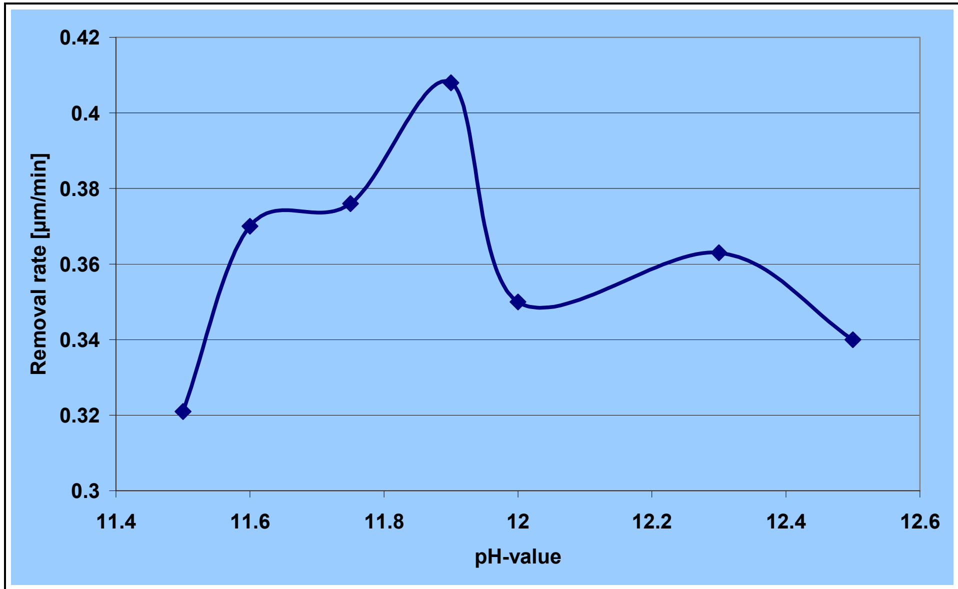


Figure 24. pH-value dependence of the MRR

When compared to conventional CMP it was also interesting to note, that the planarization using an FA pad took place within the first micrometer of material removal, whereas slurry-based CMP would need more than 5 µm to remove all topography from grinding [Paper B]. This in turn was indicated even more of an advantage using highly improved grinding technology as the only limiting factor of reduced removal by using FA CMP now was the SSD (see Figure 25).

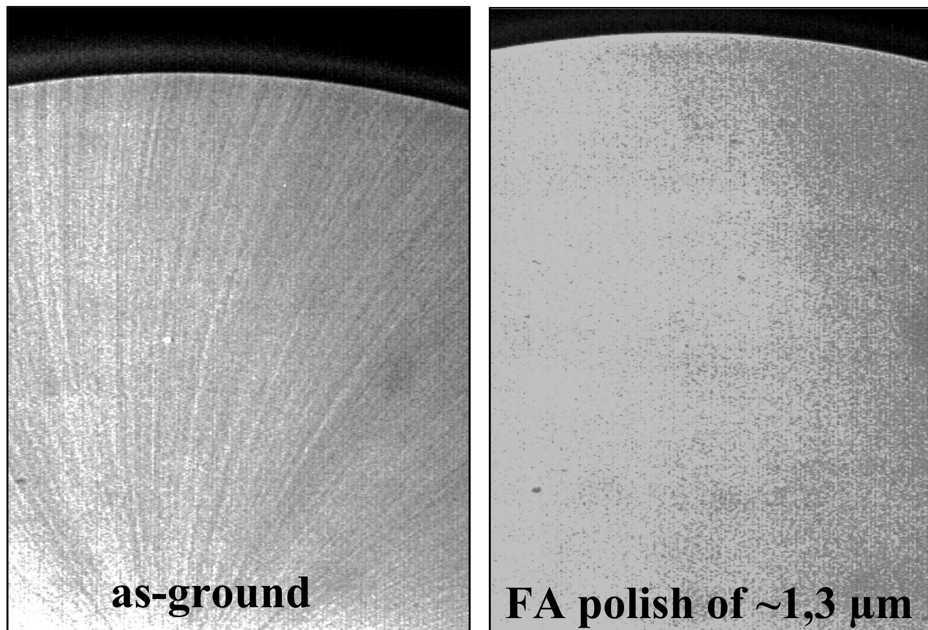


Figure 25. Magic mirror images of ground silicon wafer (left) and FA polished sample (right). Only little more than 1 µm removal is needed to planarize the entire grind line topography

3.4 Surface Quality of CMP

For the successful integration of the FA CMP polishing it was necessary to study the surface quality extensively. In order to replace conventional stock polishing with FA polishing, a similar surface quality after the process needed to be ensured. AFM scans were done for investigating the surface roughness. Figure 26 shows the comparison of an as-ground surface and an FA polished wafer with about 1 µm total removal. The rms roughness is significantly reduced from about 15 nm down to 0.75 nm. This value is as good as or even better than that being typically achieved by standard slurry-based CMP after several micrometers of removal. The subsequent fine polish should therefore require no change, but could maybe even be shorter, while enabling the same quality as is achieved using standard processing [Paper A].

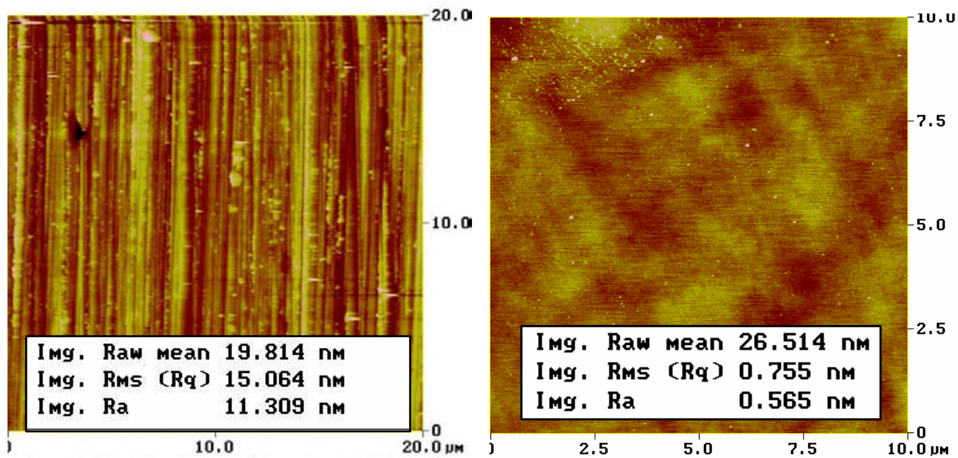


Figure 26. AFM results of as-ground silicon surface (left) and FA polished wafer (right). The Surface quality after 1 µm removal is at least as good as after slurry-based CMP or several µm

As the principle of FA CMP removal is based rather on contact with the stiff resin-type composite pattern than a soft polishing cloth, it was expected to see an influence on the surface defect level after polishing. Even when removing all SSD caused by the grinding step the FA process itself may leave its own damage on the surface to be removed by the subsequent polishing steps. Again the defect decoration method was used to investigate this behaviour. After FA CMP, the wafers were polished with different times by the standard fine polishing process and the decoration etching was done afterwards. The surface was at first inspected at 9 points on the wafer and the defect data were processed and drawn up (Figure 27). Indeed a huge amount of defects was visible directly after FA CMP. A 60 seconds fine polish however removed almost all of them. This indicates that the defects are very shallow and that they can be easily removed by a standard fine polishing process, which is mandatory for the surface quality in any case. Further polishing up to the standard time resulting in about 0.5 to 0.7 µm of removal did not seem to have any greater effect on the OISF count according to the 9-point analysis and the defect level of the wafers stabilized slightly above the compared references (right in Figure 27). To get a more detailed view with better statistics further analysis were necessary, scanning along the entire wafer radius, thus preventing the emphasis on the outer areas of the standard 9-point pattern. The result of the processed data can be seen in Figure 28.

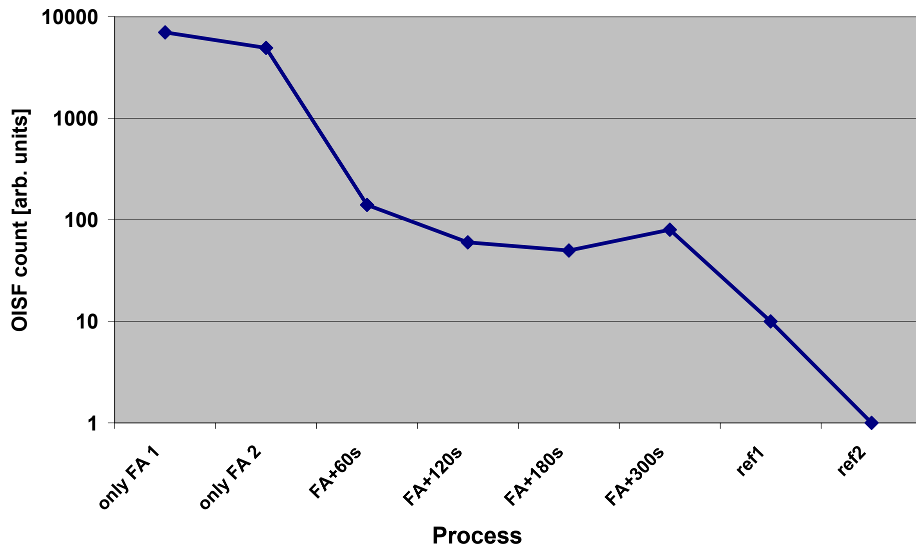


Figure 27. Cumulated OISF data from a 9-point inspection of differently processed wafers after FA CMP. The FA induced SSD is very shallow and is removed almost completely after 60s of fine polishing

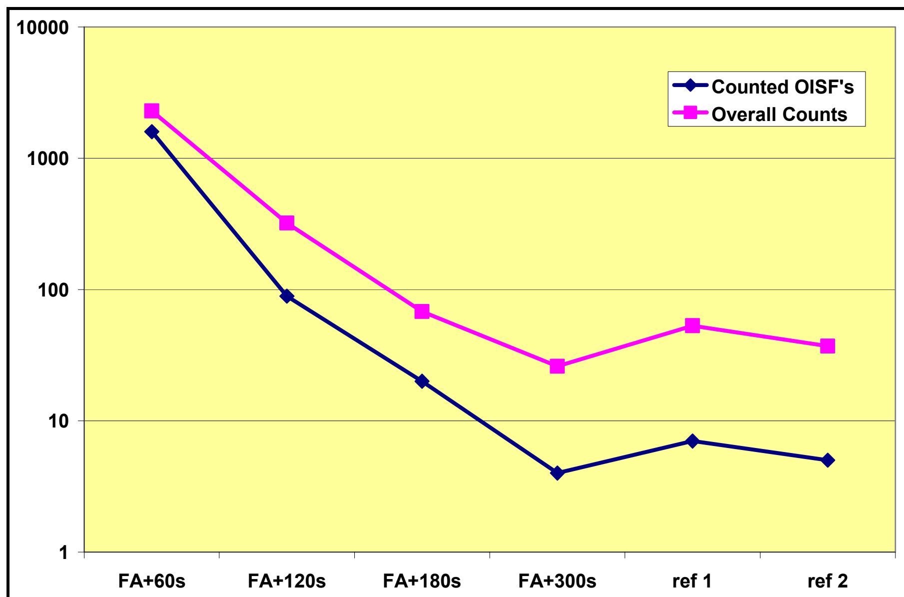


Figure 28. Diameter scans of the defect counts. The more detailed analysis shows a continuous reduction of the defects with increasing fine polish time. After standard polishing time (300s) the defects are at reference level

With the larger inspection area along the wafer radius the continuous reduction of the shallow defects becomes visible. After 300 seconds of polishing or about 0.7 µm removal the defect density reached the reference level of the two parallel analyzed non polished prime monitor wafers.

This result corroborates, that a replacement of the stock removal polishing by FA CMP is highly feasible and easy to integrate into an existing manufacturing sequence as the subsequent processes are facing no need for change. The occurring SSD of the FA process is very shallow as already the first 9-point analysis confirmed and it can be removed by standard fine polishing. The achieved surface roughness as such is at the same level or even slightly better than that of conventional stock polishing. Therefore, a manufacturing sequence with low-SSD grinding and FA CMP is very feasible [Paper C].

3.5 Stability of the New Sequence

From the beginning of the investigation, it was most important for the work to focus also on the stability of the processes with suitable base line studies. Both, the MRR and the TTV have to behave stable over a longer period of time in order to make a process suitable for production. With the adjusted process it was possible to keep the MRR stable over a longer time of processing with more than 80 wafer runs (Figure 29). The process performance of this base line run showed stable results also in terms of NU over the entire sequence as can be seen from Figure 30. Comparing the incoming and post-CMP TTV values as demonstrated by the lower graph, the almost neutral behaviour of the FA CMP step can be obtained. In many cases it was even possible to enhance the flatness of the ground wafers. This is usually not the case with slurry based CMP polishing. The details of the study can be reviewed in Paper B.

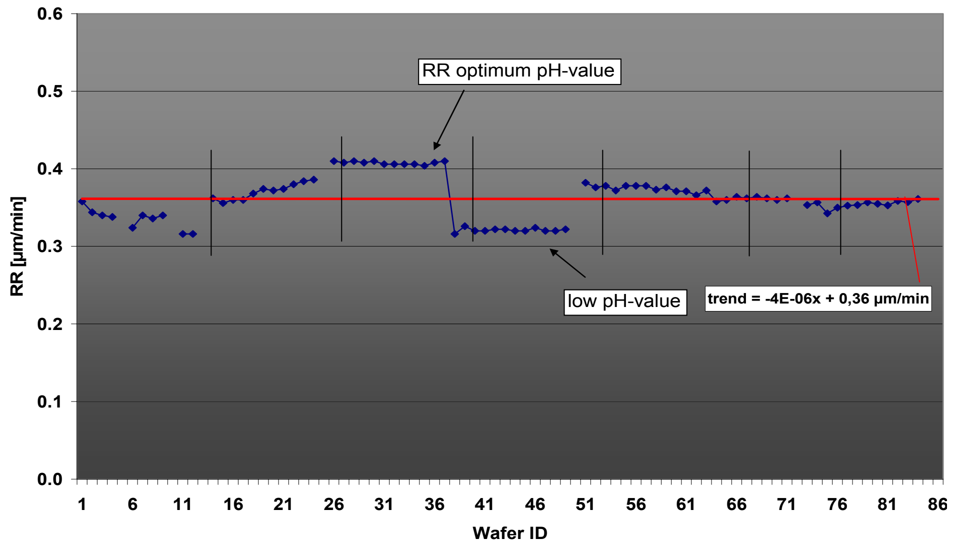


Figure 29. MRR of a base line study. The rate is very stable and shows only influence on the variation of the pH-value of the lubrication liquid

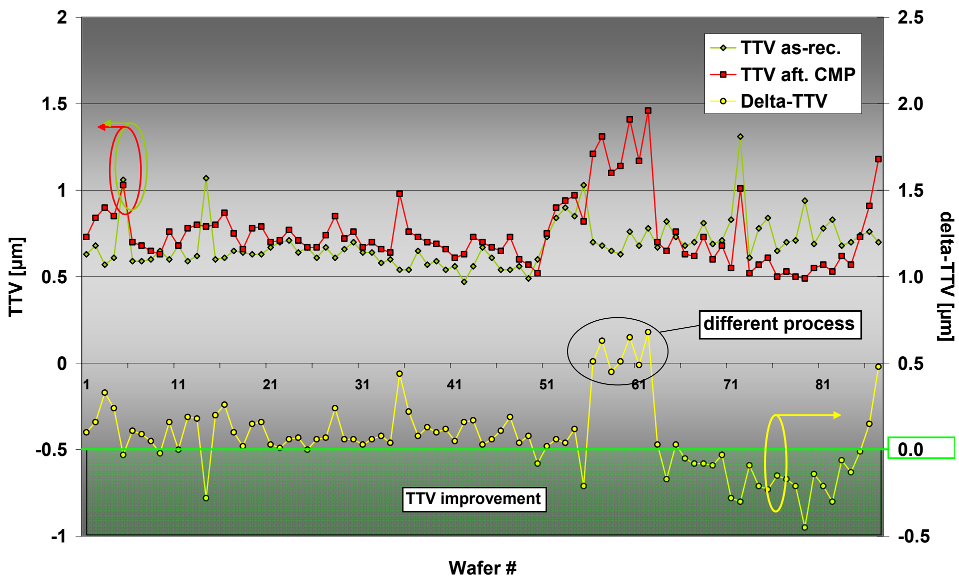
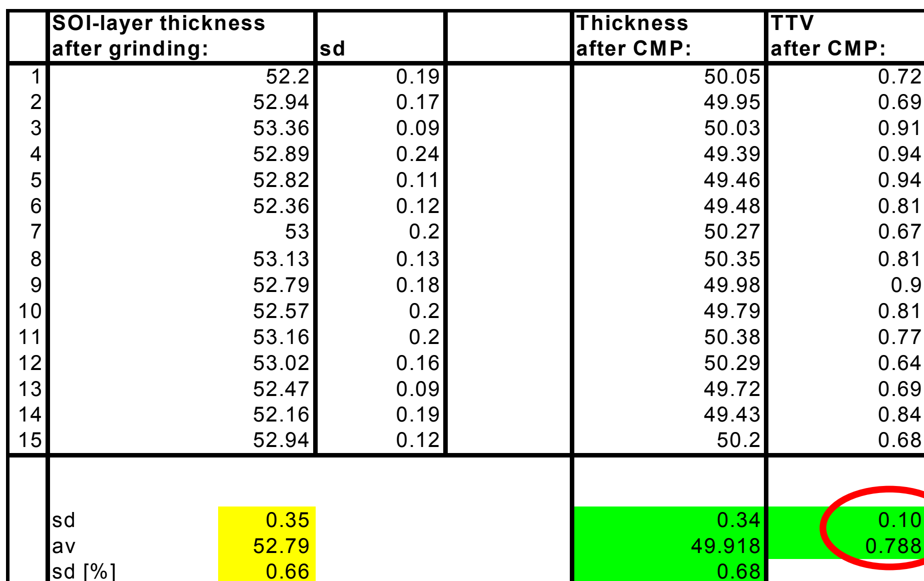


Figure 30. Comparison of incoming and outgoing TTV values of the FA CMP base line study. The lower graph corroborates the almost neutral behaviour of the polishing in terms of TTV

In a final experiment the overall performance of the new sequence was tested including the low SSD grinding, FA CMP and final polishing CMP. The set of 15 wafers with precise thickness control after grinding of 3 µm above target was polished by FA CMP and finished by slurry based polishing. In the final measurement the goal thickness of 50 µm was well targeted, which indicates the stable MRR of the fixed abrasive process. The wafers had an average TTV of clearly below 1 µm with some wafers tending towards 0.6 µm and none of them being above 1 µm. Thus also the TTV was under tight control for the test set with no bigger deviation. The detailed results are depicted in Figure 31.



	SOI-layer thickness after grinding:	sd		Thickness after CMP:	TTV after CMP:
1	52.2	0.19		50.05	0.72
2	52.94	0.17		49.95	0.69
3	53.36	0.09		50.03	0.91
4	52.89	0.24		49.39	0.94
5	52.82	0.11		49.46	0.94
6	52.36	0.12		49.48	0.81
7	53	0.2		50.27	0.67
8	53.13	0.13		50.35	0.81
9	52.79	0.18		49.98	0.9
10	52.57	0.2		49.79	0.81
11	53.16	0.2		50.38	0.77
12	53.02	0.16		50.29	0.64
13	52.47	0.09		49.72	0.69
14	52.16	0.19		49.43	0.84
15	52.94	0.12		50.2	0.68
	sd 0.35			0.34	0.10
	av 52.79			49.918	0.788
	sd [%] 0.66			0.68	

Figure 31. Overall performance of the low-SSD grinding and FA CMP sequence for thick-film SOI wafer formation. Most precise film-thickness and excellent TTV of below 0.8 µm on average (av) with low variation (sd, standard deviation 1σ) was achieved

A final comparison of the performance between the standard method with the use of conventional grinding and polishing and the novel sequence with the use of low-SSD grinding and FA CMP sequence is given in Table 1.

Table 1. Comparison of typical performance values for the standard and novel thick film SOI wafer formation

THICK FILM SOI:	**STANDARD SEQUENCE**	**LOW-SSD GRINDIG AND FIXED ABRASIVE**
Typical Required CMP Removal after Grinding	6.5–8 µm	3–3.5 µm
Achieved TTV	>1.0–2.5 µm	0.5–1.0 µm
Qualified Edge Exclusion (SOI-Layer)	3.0–4.5 mm	1.5–2.5 mm
Typical Removal Rate	0.5–0.8 µm	~0.4 µm
Final Polishing Removal	0.5 µm	0.5 µm

The advantages are evident. Because of the improved grinding process the total required removal was cut in half and the lower MRR of FA CMP compared to slurry driven stock polishing was well acceptable. Much better overall performance is possible in terms of flatness indicated by the TTV at simultaneously much more stringent edge exclusion by the novel sequence. The newly developed process enables thus the production of ultra flat thick-film SOI wafers. This type of performance cannot be achieved using standard manufacturing methods [Paper C].

4. CMP of MEMS Structures

In addition to the outstanding results being achieved by fixed abrasive CMP for the formation of the thick film SOI substrates, chemical mechanical polishing in general has also been able to improve and enable the direct formation of MEMS structures. It is already an established sequence to thin bonded wafer stacks down to dedicated thickness by grinding and do subsequent CMP processing for surface finishing, but also several other applications have been identified, where CMP plays a key role for the success of the entire MEMS process. For SOI substrates with buried cavities uniformity issues of the bonded and mechanically thinned capping silicon layer are in the scope of the researchers. With an attempt to improve the uniformity of large unsupported areas, it has been demonstrated, that using pillars to prop these diaphragm-like areas resulted in better flatness after grinding and polishing [74]. As soon as bonding is required improved surface quality of the pre-processed surfaces has to be ensured for a successful outcome. This chapter summarizes different approaches to use CMP for the smoothing of deposited films as enabler for direct LT bonding as well as developments done with the FA technology in order to preserve the pre-processed pattern of MEMS structures during polishing or to planarize large scale patterns by the CMP process. Furthermore it illustrates the possibility to use alternative materials like thick film polysilicon to be integrated and combined with established MEMS manufacturing methods.

4.1 Surface Smoothing and Planarization

Bonding technology enables the stacking of several substrates on top of each other, upon which a mechanically stable device can be formed. Different bonding techniques are used, depending on the application. The direct wafer bonding by room temperature (RT) pre-bond and subsequent LT annealing is of high interest, as the choice of materials involved in the film stack can be widened and due to its low required process temperatures even include metals. For enabling this process, one has to pay special attention to the surface roughness of the two bonding partners. The formation of SOI wafers often uses a silicon-oxide interface and in other applications in MEMS also silicon-silicon bonds are of principle interest. As long as the used substrates are of prime quality and the silicon surface is having a sub-Å roughness level they are well

suited to meet the requirement of 3 to 5 Å rms roughness, being suggested for successful LT bonding in several publications [e.g. 75, 76]. A thermally grown oxide on top of prime quality silicon usually is also well inside this specification and bonding is no issue, as long as the bonding surfaces are also free of larger particles. In order to meet advanced MEMS process requirements however, customized SOI wafers are needed and thicker oxide films are gaining more interest. With the increased thickness requirements for oxide films longer thermal oxidation times arise and beyond the level of some micrometers the thermal growth process alone is no longer feasible for the insulation layer formation due to process cost and time.

The deposition of oxides by CVD techniques provides a much cheaper, fast and reliable method with good uniformity to obtain thicker layers of the insulating material. The drawback of this method is however, that the resulting surface roughness often exceeds the requirements for a direct LT bonding process. While sputtering would lead to smoother surfaces it offers very slow deposition rates and the roughness is still in the nm-range, thus would need CMP. Therefore, CMP processes have been developed to enhance the roughness level. Combining soft polishing pads used in silicon processing and oxide slurries from the typical IC ILD polishing with suitable process parameters is leading to well controllable removal with good surface quality achieved on unpatterned wafers.

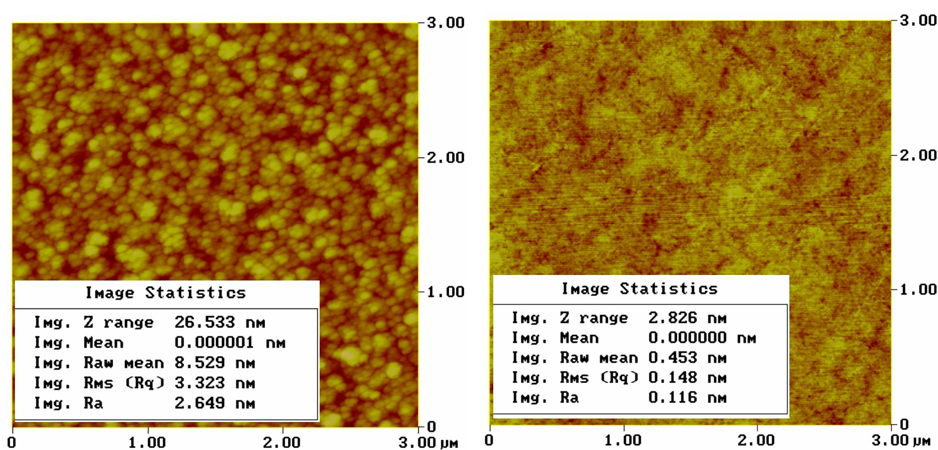


Figure 32. AFM analysis of LTO oxide before (left) and after CMP (right) smoothing. The removal of around 700 Å by the dedicated CMP process reduces the roughness, so that the surface is suitable for direct bonding

The level of roughness can be reduced to Å-level, while as-deposited CVD oxides provide rms roughness values at nanometre range. The required total removal for Å-level surface quality is able to be minimized to about 100 nm and the polished surfaces can be bonded at RT after suitable cleaning. The above Figure 32 shows typical AFM nanographs of an as-deposited CVD oxide (left) and a polished surface (right) respectively.

For encapsulation of patterned structures it is mandatory to simultaneously provide a both plane and smooth surface, which then can be bonded to another substrate. Wafer-level packaging (WLP) technology for example has gained a lot of interest, as the completed components are easy to handle and the packaged devices are completely protected due to the hermetic seal encapsulation of the bond with substantial cost saving comparing to established packaging methods [77]. Using bonding as a manufacturing approach can for example begin with a deposition of a thick CVD or LTO oxide layer on top of the ready device. A suitable CMP process is then applied to planarize the topography of the sacrificial and connecting oxide and to smooth the surface to bondable level. Typical MEMS patterns however are usually much larger than the features used in IC devices and therefore conventional ILD CMP processes would only be able to planarize such a pattern to a certain level leaving a residual step with a rounded shape (see Figure 8, Chapter 2.4). With this insufficient planarization level the required planarity for successful bonding cannot be reached. Therefore FA CMP pads have been used to enable a process for large scale pattern planarization. Figure 33 shows the result of the polishing sequence.

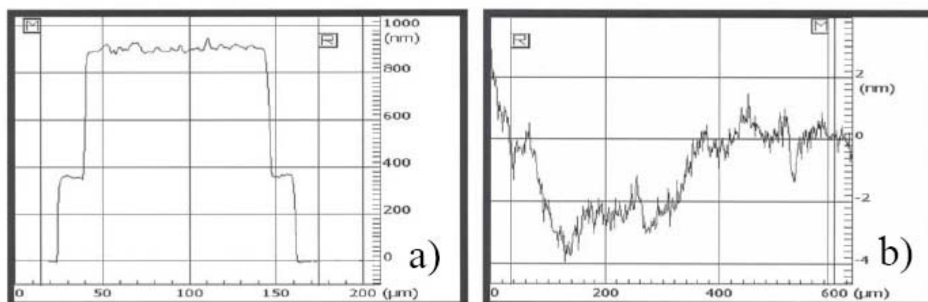


Figure 33. Large scale pattern before (a) and after CMP planarization (b). The pattern is completely removed (note the vertical scale!) and leaves a smooth surface for bonding [78]

CMP by FA is able to remove the large scale pattern totally. The required removal for the total planarization is meanwhile only slightly higher than the initial step height itself. This once again indicates the efficient planarization capability and close to ideal CMP behaviour of the FA pad. The surface quality can be even further enhanced by a short second polishing step on a very soft pad to reduce roughness. This again leads to Å-level roughness, which clearly ensures direct LT bonding capability [78].

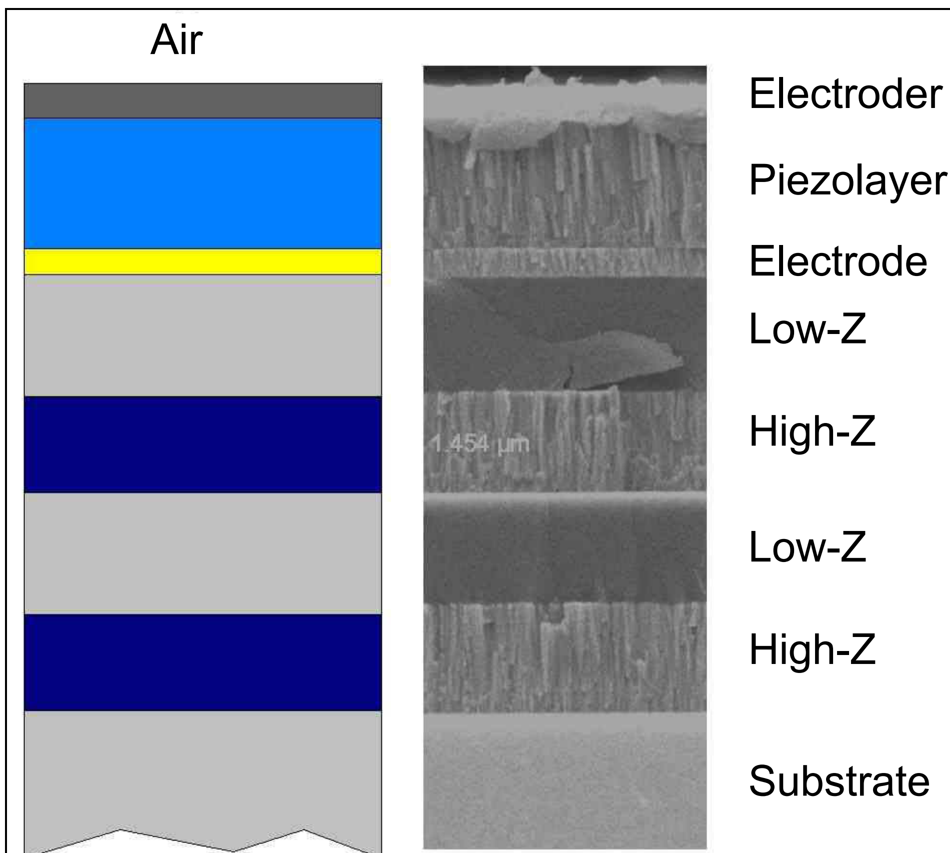


Figure 34. Film stack for the formation of FBAR filters

Aside from bonding there are other MEMS related processes, which benefit from smooth surfaces that result from CMP. For optical and acoustical applications in MOEMS (Micro opto electrical mechanical systems) and rf-MEMS (radio frequency-MEMS) the roughness of the wave conducting layers plays a major role in the losses of the device.

It is known that the surface roughness is cumulative with each deposited layer if no smoothing interlayer such as flow glass is used. As layer deposition starts on a rough surface it can lead to undesired disturbance of the materials integrity and quality. This is especially the case for active layer formation, for example with piezoelectric materials. In Paper E CMP is utilized for the smoothing of an acoustic mirror stack for the formation of FBAR filters.

Figure 34 depicts such an FBAR structure and shows an SEM graph of the filter stack. Starting from the substrate a total of seven films are deposited for filter formation. The most critical part in terms of losses and Q-factor (quality factor) of the filter is the piezolayer between the top and bottom electrode. Below this active part the acoustic mirror stack is formed by alternate deposition of tungsten and PECVD oxide respectively. The mirror stack reflects the acoustic wave and enhances its orientation.

Highest influence on the Q-factor of the device is expected to come from the acoustic coupling of the rf-wave forming piezolayer to the mirror stack. As roughness of the interlaying oxide film increases, energy losses are resulting due to interference phenomena at the interfaces. This in turn reduces the Q-factor of the filter. Furthermore the piezolayer itself has to have a high degree of texture and well orientated crystallites for highest possible piezo-activity.

Therefore the piezo-material carrying up most oxide layer below the bottom electrode of the mirror stack is polished by a slurry-based CMP step and the roughness is reduced down to Å-level. The subsequent sputtering of the piezo-active ZnO shows a drastically reduced surface roughness after CMP, as the film deposition process now starts from the atomically smooth surface (see Figure 35). This in turn may have positive impact on the piezo activity of the ZnO and therefore could lead to higher Q-factors of the resonator structure. It was however not possible within this study to connect the change of the Q-factor to the presence of the CMP process, as other factors of the resonator formation were of great influence too and the polishing process also introduced some other issues [Paper E].

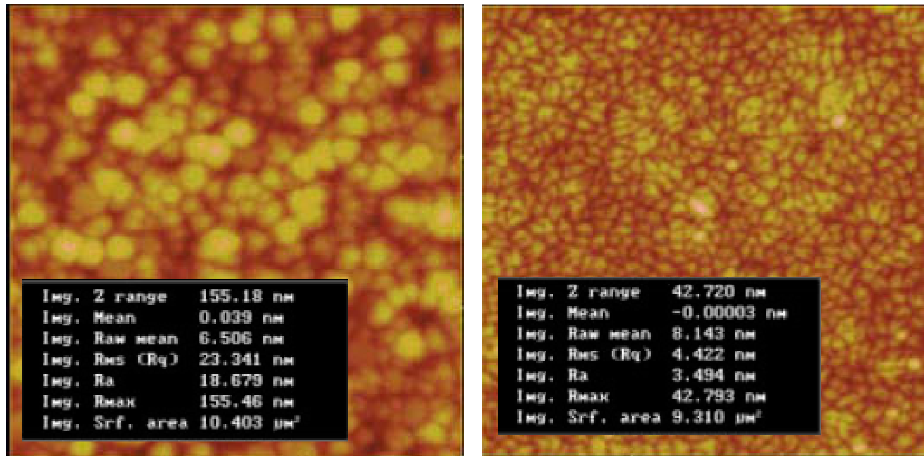


Figure 35. AFM nanographs of the sputtered ZnO film without (left) and with prior CMP smoothing (right) of the underlying oxide film. The roughness and structure of the piezo-active film is greatly improved in the case of polished oxide [Paper E]

The two factors of greatest importance for the successful integration of CMP and the best resulting benefit of the smoothing process are the particle contamination after polishing and the level of rounding of the free standing structures. Due to heavy particle contamination after slurry based CMP an additional SC-1 cleaning was introduced. The particle contamination was removed, but the oxide film showed pin-holes after this cleaning step. The formation of these holes is most probably attributed to defects from the underlying tungsten film, which weakens the deposited oxide. As the wafer is cleaned the weak areas tend to get etched by the ammonia of the required SC-1 bath and this in turn leads to the obtained pin holes [Paper E].

4.2 Pattern Conservation

The rounding of the pattern, its erosion and dishing between single pattern features by conventional CMP is a known fact, especially with the use of soft polishing pads. These are generally utilized for smoothing surfaces. The process leads to a very good surface finish, but for the pattern conservation a more rigid polishing cloth would be required. A hard pad however leads to inferior surface quality but still could not prevent the edge attack totally.

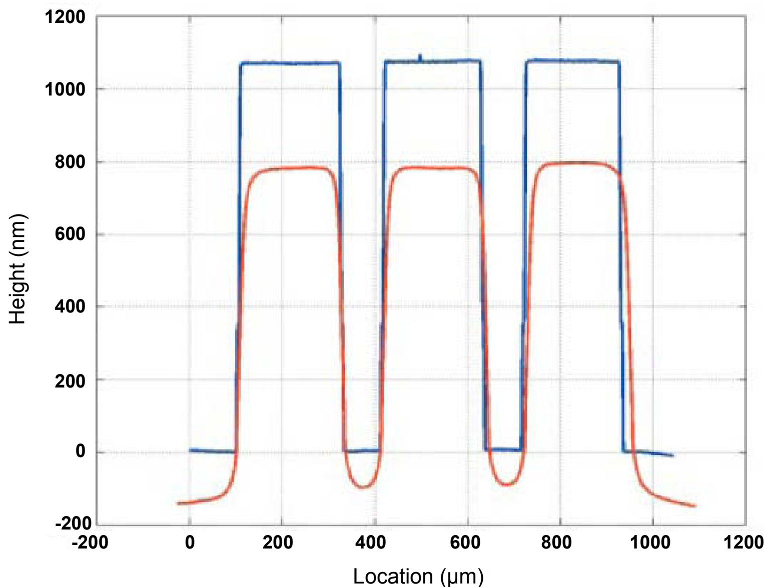


Figure 36. Filter structure before (blue) and after CMP smoothing (red). Despite the desired material removal on top of the pattern, rounding, erosion and dishing of the film stacks occurs with conventional polishing [Paper E]

In Figure 36 the impact of the smoothing process on the structure is visible. The filters experience rounding at the edges, which reduces the active area and could in turn lead to losses in the Q-factor of the resonator. The more detailed picture on the left of Figure 37 depicts the erosion clearly. Furthermore, dishing occurred between the film stacks as the soft polishing pad reaches the down areas of the pattern. This can be observed from the rounded bottom of the polished sample in Figure 36.

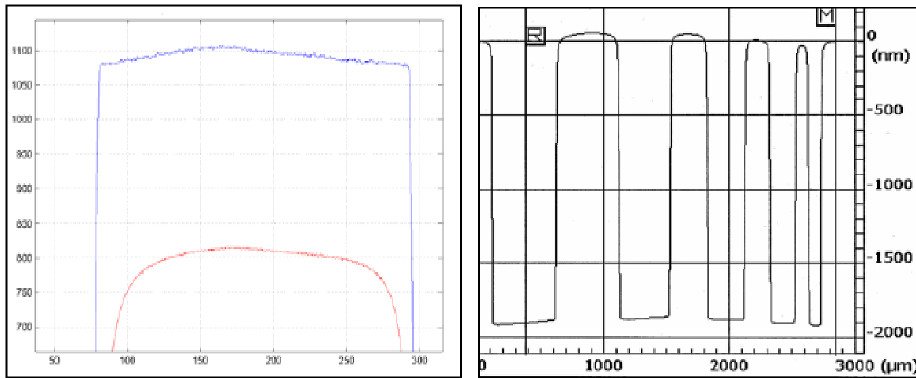


Figure 37. Erosion of the filter structure (left) and improved conventional CMP process with reduced rounding and no visible erosion on the pattern bottom (right) [Paper D]

A lot of development work has been done to overcome this trade-off and improvements have been realized. With the new process another oxide pattern was polished. Now rounding and erosion were greatly reduced and dishing was totally absent (Figure 37 on the right). Still this was not sufficient for the application as major losses would further be expected from still persistent rounding.

Therefore fixed abrasive pads were used to work on the smoothing of elevated patterns. As the abrading composite is rather stiff and decomposes constantly during polishing to expose fresh abrasives rather than to just deform due to the applied load the rounding should be greatly reduced [Paper D]. For ensuring a good surface quality special care was taken that the polishing occurred with sufficient lubrication. As it has already been seen in case of silicon polishing (Chapter 3.3) and with the removal of big oxide patterns (see above), that the required removal for removing the roughness of the deposited film was very low. This in turn was a benefit for the process as the required surface finish would be gained quickly and the film thickness could be adjusted accurately to the needs of the device by adjustment of the polishing time.

Figure 38 compares the details of the critical corner of an elevated oxide structure, polished by conventional CMP (left) and by FA CMP (right). The corner rounding in case of slurry-based CMP reaches several tens of micrometers into the pattern and the slope of the pattern as such is reduced by

the erosion resulting from the process. Applying the FA pad polishing on the same pattern keeps the slope in original shape (besides the systematic error introduced by the finite rounding of the scanning stylus!) and no rounding is visible on top of the oxide structure (note the arrow on the right of Figure 38).

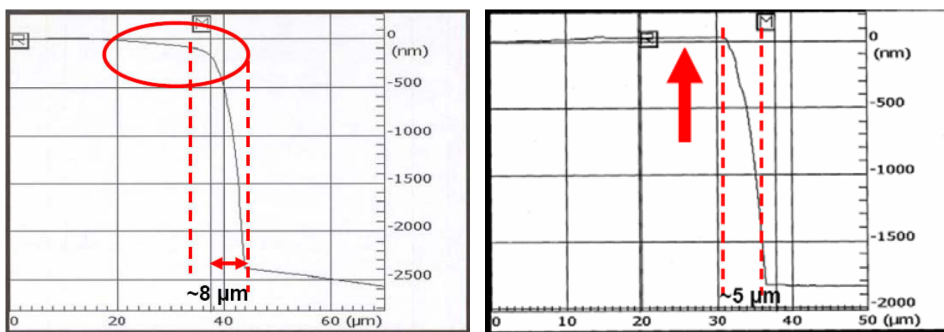


Figure 38. Impact of CMP on the pattern. Conventional CMP (left) tends to strong rounding, while the FA process has very little influence [Paper D]

Besides maintaining the pattern integrity it was of high importance to get a good surface finish as later bonding is used to connect the pre-processed wafer to a cap wafer and therefore an AFM analysis was also made.

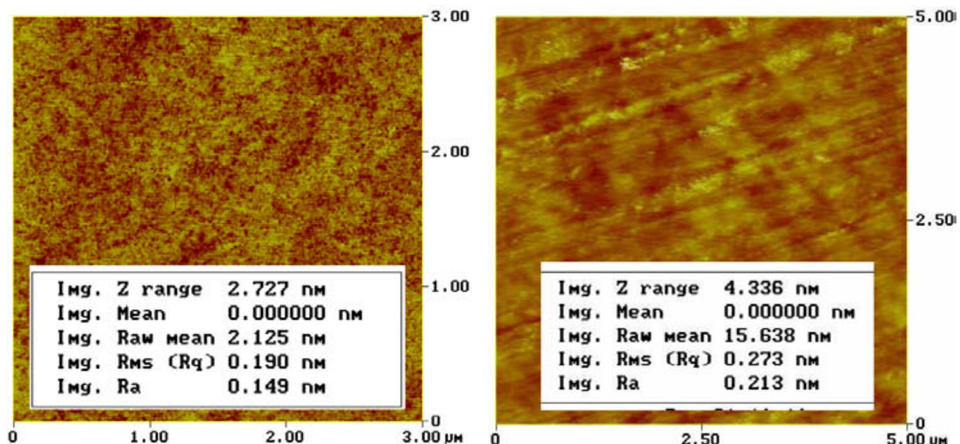


Figure 39. AFM nanographs of slurry-based oxide CMP surface (left) and FA CMP oxide surface (right). While the roughness values are similar the appearance of the surfaces are different. The "wiped" finish of the FA sample is however only about 1 nm in total height difference and of no concern [Paper D]

This made clear another aspect of the novel FA process. The resulting surface roughness was within the range of 2Å like after conventional CMP (Figure 39) and no additional smoothing CMP step was required. The surface however appeared different with a “wiped” finish. A cross-sectional analysis was done to evaluate the topography. A total height variation of less than 1 nanometre was obtained and therefore it was of no concern to use FA, even for the sensitive DWB (direct wafer bonding) process [Paper D].

The bonding test of the FA polished samples resulted in a void-free formation of a wafer stack. A detailed SEM picture of the critical corner after its bonding to the cap wafer can be seen from Figure 40. Bonding occurs to the very edge of the structure providing mechanical stability and the absence of dead pockets. This can be very important for example in the case of using this method for manufacturing micro-fluidic devices.

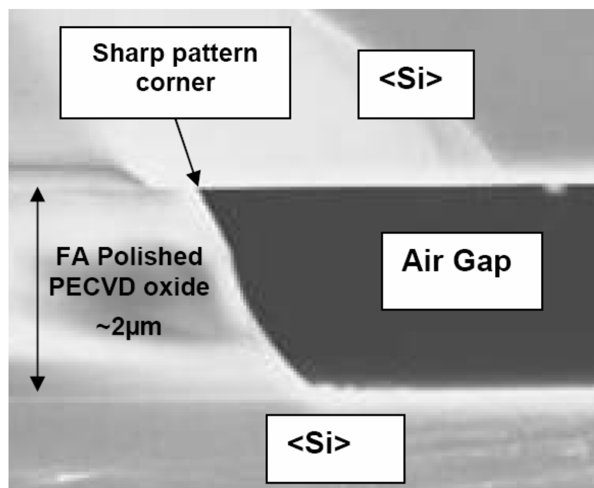


Figure 40. Detailed SEM picture of the bonded corner to the cap wafer. The bonding of the FA polished sample reaches throughout the entire oxide pillar, where the rounding of slurry based CMP would inhibit proper contact

4.3 CMP of Polysilicon Films

The use of polysilicon is very interesting for several MEMS applications, but also for the formation of alternative SOI substrates, when single-crystalline

material is not required. Several people have been reporting on the use of polysilicon in combination with CMP for their MEMS devices [79, 80, 81]. There is often need to bond the polysilicon surface to another substrate. This is usually done by anodic bonding as the surface quality of the deposited polysilicon layer is below the requirements for DWB. Aiming however for high deposition rate thick film polysilicon such as APCVD films with several tens of micrometers thickness, causes severe roughness [82], which would prevent even the most insensitive bonding process. Polishing is therefore needed to implement these films into advanced device formation and alternative substrate manufacturing.

A dedicated two step process has been developed to provide sufficient roughness reduction and surface quality with lowest possible removal [Paper F]. The initial roughness and all other surface disturbances have been removed by a planarizing first step polishing and by a surface finishing second step the roughness was reduced to Å-level (see Figure 41).

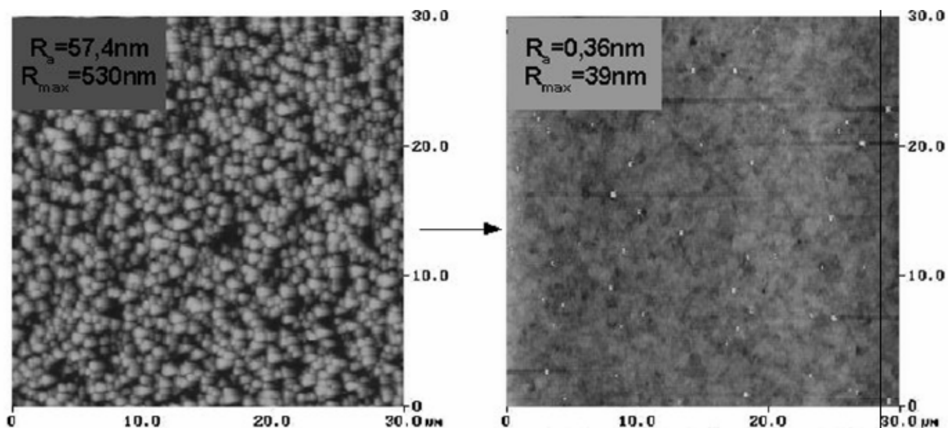


Figure 41. Roughness reduction of thick film polysilicon by dedicated two step CMP process. The resulting surface roughness reaches the quality for enabled low temperature direct wafer bonding

With this CMP sequence it was possible to enable DWB of polysilicon to oxide deposited quartz and glass substrates as well as oxidized silicon wafers at RT and to provide the regular bonding strength of 2000mJ/m^2 as usually seen in silicon wafer bonding.

A SAM picture of a bonded sample can be seen from Figure 42, were only few voids occurred at the outer edge due to wafer handling issues.

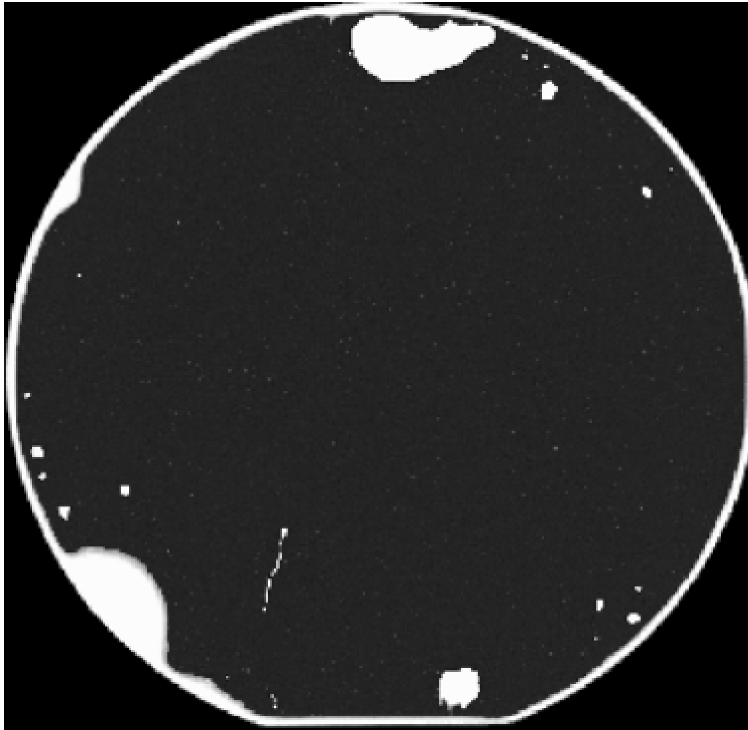


Figure 42. SAM picture of a bonded thick film polysilicon wafer with an oxidized silicon wafer. After applying the developed two step CMP sequence only a few voids caused by wafer handling issues are remaining on the otherwise solid substrate connection

The development of a dedicated CMP process thus enabled the use of polysilicon thick films for the use of WLP or special SOI substrates. With further studies of the polishing process it will be possible to also integrate the simultaneous planarization of the underlying device pattern of a MEMS device and enables the simultaneous capping of a ready device by formation of a double layer SOI wafer. This is an important achievement to manufacture real 3D-MEMS devices, which are a main path for several upcoming developments like smart multi-axis accelerometers for automotive applications.

5. Conclusions

The purpose of this work has been the utilization of CMP in the field of MEMS manufacturing for enabling new capabilities in the area of micromechanical device formation.

Starting from the use of the FA pad technology for thick film SOI wafer processing it was possible to present a new sequence, which results in ultra flat SOI layers. The overall quality of the substrates was examined by utilizing standard metrology techniques of industrial wafer manufacturing. The additional use of low-SSD grinding enabled a greatly reduced polishing removal and led to a highly competitive method ready for industrial production application. The mechanism of removing silicon by FA is studied and a model for abrasion is presented, based on the findings of the intense analysis of the process. The particularities of the FA pad are analyzed and turned into benefits.

CMP was successfully implemented in MEMS structure manufacturing. By polishing of thick deposited oxide films Å-level roughness enabled the DWB at RT and LT annealing, and allows the use of a wide variety of materials in the stack including metals. Planarization of large features often mandatory in MEMS is enabled by the use of a suitable FA CMP step. Conventional CMP processes would lead to inferior results and are compared with the FA sequence.

Smoothing the surface of elevated patterns is demonstrated by FA CMP, resulting in Å-level roughness. No edge rounding or erosion of the features is observed and successful bonding corroborates the beneficial outcome of the process. A comparison with slurry based CMP indicates the tremendous benefits of the novel planarization technique.

With the results of this work it is possible to utilize CMP for several new applications in the field of micromechanical structures as well as significant knowledge on the behaviour of fixed abrasives is generated. A comprehensive overview of CMP technology and its tribology in both conventional and fixed abrasive polishing is given. The removal mechanism of oxide and silicon during polishing is discussed and connected to the actual fabrication challenges being faced in today’s processing.

Acknowledgements

To the achievement of this work many people have been supporting me greatly from earliest days on and I shall make the attempt to name them here know that this list is not exhaustive.

At first I would like to name my parents Angela and Artur Kulawski who have been supporting my technical interest from childhood on, even they did not always comply with my humble ways to discover the world of mechanics and electricity (and god gave me his best guardian angels on my way too...). With their support during school days and studying time it was possible for me to educate myself and to find my way. Their protection and self-abandonment for my sisters and my own future has been invaluable for our development and cannot be expressed in words.

I further want to thank the rest of my family, my sister Angela for being able to stand me all these years and for having a very first look at the draft of this thesis, giving her language advice. It was a great help and improved my further writing to great extent. My Cousin Jörg Brekeller as he was one of my great idols in childhood. He had a great patience in showing and explaining me as far younger boy all the electric things he was experimenting with; he maybe is the initiator of my wish to once become an electrical engineer. Both of my grandmas who passed away, for their warm support and interest during my development and my uncle Rudolf for all his generous support during the tight days and for giving me accommodation when being needed.

I would to thank my teacher Mr. Stert for all his support during school times in further developing my technical skills far beyond the scope of daily education and my teachers Mrs. Harms and Dr. Mewes for their excellent preparation for the university times.

I would like to express my deepest thanks to the technical faculty of the Chistian-Albrechts-University of Kiel in Germany for a very profound education, especially my teachers Prof. Günzler and his co-operating Docent Blessenohl, Prof. Dirks and Prof. Seegebrecht.

I would like to express my thanks to the Fraunhofer Institute of Silicon Technology ISiT for guiding me with a high degree of freedom to semiconductor technology and CMP and to my first employer Peter Wolters for a very intense but highly educational time and good team work especially with Dr. Georg Mörsch.

I would like to thank Jouni Heleskivi and Ilkka Suni for considering my employment at VTT and giving me again a high degree of freedom to develop my work place. The entire team of VTT to welcome the foreign stranger take him into the group, especially Kimmo Henttinen, Hannu Luoto and Tommi Suni who all have also greatly supported the work contributing to this thesis and Wesa Wegelius for all his technical assistance.

One of my best friends and greatest support from the first hour here in Finland Dr. Jyrki Molarius I owe more than many thanks. He has been able to integrate me into the Finnish and VTT culture and it is his fault that you now have to read this dissertation, thank you once again! He also contributed to this work as my mentor and with proof reading to make this book smooth.

I am very grateful to having been getting great support from Tekes in form of funding for the projects I initiated at VTT, especially to Immo Seppänen. Together with the industrial partners Okmetic and their development responsible Dr. Jari Mäkinen and Markku Tilli, VTI Technologies and their responsible Dr. Risto Mutikainen and Micro Analog Systems with their responsible Markku Orpana and Kari Valvisto they have been making this work possible.

A very good friend and great supporter of mine Mike Kirkpatrick I would like to thank gratefully to proof-read the thesis and advise me for proper and readable language. I always enjoy the times when being together with him surely not only for his outstanding language capabilities but for his warmth and delightful personality. Also his company Strasbaugh has been very supportive for this work and a lot of knowledge has been generated due to the tight co-operation.

Big thanks to Frauke Weimar, John Gagliardi and Feben T. Gobena from 3M. It was Frauke who was able to initiate the first tests on fixed abrasive pads. She worked incredibly hard to keep up with the U.S. team. John I would like to thank for all the support he gave me with fruitful discussions and making it possible to

find the right pads for our new application. Feben I would like to thank for helping me incredibly much in getting into touch with the fixed abrasive technology and the team at 3M, when I did my very first steps.

I am very grateful to Dr. Risto Mutikainen and Dr. Christian Diekmann for their pre-examination and valuable comments. I am also thankful to the opponent Dr. Gerfried Zwicker, for agreeing to examine the thesis and my supervisors Professor Pekka Kuivalainen and Professor Ari Lehto for taking me into their custody and to support my work in an unbureaucratic and convenient way.

Last but not least I would like to thank my partner Tarja Koski. It was her to bring me to Finland and she has been ever since supporting all my needs and her love has been bringing me through all the long cold winters. Her family I would like to thank for being often of great support and substitute to the ones I had to leave behind in Germany.

References

1. F. W. Preston, *The theory and design of plate glass polishing machines,* J. Soc. Glass. Technol., Vol. 11, pp. 214–256, (1927)

2. Computergram International, *IPEC; CMP equipment manufacturer is number one of fasted growing companies with 71,136% rev. growth between 1992 and 1996,* Feb 10 1998

3. Semiconductor International, *Process Complexity Fuels Integrated Metrology*, July 2005

4. bcc – Business Communications Company, *RGB-288 Chemical Mechanical Polishing Equipment and Materials: A Technical and market analysis,* Dec. 2003

5. http://www.intel.com/technology/mooreslaw/index.htm

6. R. J. Walsh, U.S. Patent No. 3,857,123, Dec. 31, 1974

7. Ming-Fea Chow, U.S Patent No. 4,702,792

8. Jeffrey W. Carr, U.S. Patent No. 4,954,142

9. Handbook of Multilevel Metallization for Integrated Circuits – Materials, Technology, and Applications; Edited by: S. R. Wilson, C. J. Tracy, J. L. Freeman Jr.; William Andrew Publishing/Noyes; (1993); ISBN: 0-8155-1340-2

10. D. Schramm et al., *Algorithm implementation and techniques for providing more-reliable overlay measurements and better tracking of the shallow-trench isolation (STI) process*, Metrology, Inspection, and Process Control for Microlithography XIII; SPIE Proceedings Vol. 3677, pp. 116–122; Editor: Bhanwar Singh, Advanced Micro Devices Inc.; Sunnyvale, CA, USA; (1999); ISBN: 0-8194-3151-6

11. D. Schramm et al., *Tracking STI using an advanced optical metrology algorithm,* MICRO Magazine Oct. 2000

12. N. Elbel et al., *Tungsten Chemical Mechanical Polishing,* Journal Electrochemical Society, **145**, Issue 5, pp. 1659–1664, (1998)

13. J. M. Steigerwald, S. P. Murarka, R. J. Gutmann, *Chemical Mechanical Planarization of Microelectronic Materials,* Ch. 8, pp. 272–275; J. Wiley & Sons, Inc.; New York; (1997); ISBN: 0-471-13827-4

14. M. Naik et al., *Process integration of double level copper-low k (k=2.8) interconnect,* Proc. of the IEEE intern. Conf. Interconnect Technology (1999)

15. J. T. Pan, P. Li, K. Wijekoon, S. Tsai, F. Redekar, *Copper CMP integration and time dependent pattern effect*, Proc. Int. Interconnect Technology Conf., (1999), pp. 164–166

16. ITRS roadmap of technology, (2003)

17. Takayuki Matsuda et al., *Characteristics of Abrasive-Free Micelle Slurry for Copper,* Journal of The Electrochemical Society, **150**, Issue 9, pp. G532–G536, (2003)

18. Solid State Technology, *Improved Planarization for STI with Fixed Abrasive Technology,* pp. 123–128, June 2000

19. Semiconductor Magazine, *Making CMP Work*, **3**, No. 7; July 2002

20. Semiconductor International, *CMP grows in Sophistication,* Nov. 1998

21. J. M. Steigerwald, S. P. Murarka, R. J. Gutmann, *Chemical Mechanical Planarization of Microelectronic Materials,* J. Wiley& Sons Inc.; New York; (1997); ISBN: 0-471-13827-4

22. Cybeq Product Information, 1994

23. J. M. Steigerwald, S. P. Murarka, R. J. Gutmann, *Chemical Mechanical Planarization of Microelectronic Materials,* Ch. 2, p. 30; J. Wiley & Sons Inc.; New York; (1997); ISBN: 0-471-13827-4

24. T. Yu, C. Yu, M. Orlowski, A statistical polishing pad model for chemical mechanical polishing, in *Proc. IEEE Int. Electron Devices Meeting*, Washington, DC, Dec. 5–8, 1993, pp. 865–868

25. T. Yu, C. Yu, M. Orlowski, Combined asperity contact and fluid flow model for chemical mechanical polishing, in *Proc. Int. Workshop on Numerical Modelling of Processes and Devices for Integrated Circuits: NUPAD V* Honolulu/New York, HI/NY, June 5–6, (1994), pp. 29–32

26. S. R. Runnels, Tribology analysis of chemical mechanical polishing; *J. Electrochem. Soc.*, **141**, pp. 1698–1701, (1994)

27. J. Tichy, J. A. Levert, L. Shan, S. Danyluk, Contact mechanics and lubrication hydrodynamics of chemical mechanical polishing, *J. Electrochem. Soc.*, **146**, pp. 1523–1528, (1999)

28. J. Luo, D. A. Dornfeld, *Material Removal Mechanism in Chemical Mechanical Polishing: Theory and Modeling*, IEEE Transactions on Semiconductor Manufacturing, **14**, No. 2, May (2001)

29. A. Phillipossian et al., *Spectral Analysis of Frictional Forces in ILD CMP*, Mat. Res. Soc. Symp. Proc., **767**, (2003)

30. A. Phillipossian, E. Mitchell, *Micro,* **20**, No. 7, p. 85, (2002)

31. A. Phillipossian, S. Olsen, *Effect of Pad Surface Texture and Slurry Abrasive Concentration on Tribological and Kinetic Attributes of ILD CMP*, Mat. Res. Soc. Symp. Proc., **767**, (2003)

32. Kenneth C. Ludema, *Friction, Wear, Lubrication: A Textbook in Tribology;* CRC Press Inc., (1996)

33. A. Phillipossian, S. Olsen, *Effect of Slurry Flow Rate on Pad Life during Interlayer Dielectric CMP,* Journal of The Electrochemical Society, **151** (6), pp. G436–G439, (2004)

34. J. M. Steigerwald, S. P. Murarka, R. J. Gutmann, *Chemical Mechanical Planarization of Microelectronic Materials,* Ch. 5, pp. 129–180, J. Wiley & Sons, Inc.; New York; (1997); ISBN: 0-471-13827-4

35. L. Holland, *The properties of glass surface*, Chapman & Hall; London; (1964)

36. H. Landis, P. Burke, W. Cote, W. Hill, C. Hoffman, C. Kaanta et al., *Integration of chemical–mechanical polishing into CMOS integrated circuit manufacturing*, Thin Solid Films, **220** (1–2), pp. 1–7, (1992)

37. M. Tomozawa, K. Yang, H. Li, S. P. Murarka, *Basic science in silica glass polishing*, in: S. P. Murarka, A. Katz, K. N. Tu, K. Maex, editors, MRS Symp. Proc., **337**, p. 89, (1994)

38. L. M. Cook, J. Non-Cryst. Solids, **120**, 152, (1990)

39. D. Castillo-Mejia, S. Beaudoin, *A Locally Relevant Model for Wafer Polishing*, J. Electrochem. Soc., **150**, pp. G96–G102, (2003)

40. E. Mendel, Solid State Technology, **10**, 27, (1967)

41. A. Schnegg et al., Electrochem. Soc. Extend. Abstr., **85-1**, 394, (1985)

42. G. J. Pietsch et al., *Chemomechanical polishing of silicon: Surface termination and mechanism of removal,* Appl. Phys. Lett., **64**, 3115, (1994)

43. G. J. Pietsch et al., *The atomic scale removal mechanism during chemo-mechanical polishing of Si(100) and Si(111),* Surface Science, **331–333**, pp. 395–401, (1995)

44. D. Gräf et al., J. Vac. Sci. Technol. **A7**, 808, (1989)

45. W. J. Patrick, W. L. Guthrie, C. L. Standley, *Application of chemical-mechanical polishing to the fabrication of VLSI circuit interconnections,* J. Electrochem. Soc., **138**, 6, pp. 1778–1784, (1991)

46. S. Sivaram et al., *Chemical-Mechanical Polishing of interlevel dielectrics: Models for removal rate and planarity,* SEMATECH, Austin, TX, Tech. report (1992)

47. S. R. Runnels, *Feature-scale fluid-based erosion modeling for chemical-mechanical polishing,* J. Electrochem. Soc., **141**, 7, pp. 1900–1904, (1994)

48. J. Warnock, *A two-dimensionaly process model for chemimechanical polish planarization,* J. Electrochem. Soc., **138**, 8, pp. 2398–2402, (1991)

49. S. R. Runnels et al., *A Modeling Tool for chemical-Mechanical Polishing Design and Evaluation,* IEEE Transactions on semiconductor manufacturing, **11**, 3, (1998)

50. www.strasbaugh.com

51. J. Kalpathy-Cramer et al., *Pattern Density and Feature Size Effects in STI CMP: Their Impacts on Electrical Performance,* 2nd Intern. Symp. Chem. Mech. Plan, Phoenix, AZ, (1998)

52. Y. Gotkis, R. Kistler, *Fundamentals of Cu CMP for Dual Damascene Technology,* 2nd Intern. Symp. Chem. Mech. Plan, Phoenix, AZ, (1998)

53. http://www.jsrmicro.com/download/JSR_041013CMPPresentation.pdf

54. Y. Yoon et al., *Influence of high Selectivity Slurry in Shallow Trench Isolation CMP on junction Leakage Characteristics,* Electrochem. and Sol. State Let., **5**, pp. G19–G21, (2002)

55. R. Tian et al., *Model-based dummy feature placement for oxide chemical-mechanical polishing manufacturability*, Proc. 37th IEEE Conf. Design & Automation, Los Angeles, CA, pp. 667–670, ISBN: 1-58113-187-9, (2000)

56. C. Coming et al., *Method of fabricating a trench isolation structure using a reverse mask,* U.S. Patent # 6015755

57. W. Moser, *Technological Trends in Chemical Analysis to be Used as End-point Detection to Control CMP Processes,* Report, Eco Physics AG

58. T. C. Tsai et al., *Process Development of a hybrid Fixed Abrasive STI CMP for Logic Applications at 65 nm Technology node,* CMP-MIC Proc. (2005)

59. J. Gagliardi, T. Vo, *Total Planarization of the MIT 961 Mask Set Wafers Coated with HDP Oxide*, CMP-MIC Conference, Santa Clara, CA, (2000)

60. V. R. Gorantla et al., *Study of Pattern Density effects in CMP Using Fixed Abrasive Pads,* J. Electrochem. Soc., **150**, 12, G821–G825, (2003)

61. J. Gagliardi, *STI Polishing with 3M's Fixed Abrasives;* VMIC Conference, Santa Clara; CA, (1999)

62. L. Economikus et al., *EVALUATION OF FIXED ABRASIVE PADS FOR STI PLANARIZATION,* CMP-MIC, (2001)

63. Private communication J. Gagliardi, 3M

64. J. Gagliardi, *Fixed Abrasive Direct STI CMP allows Elimination of the Conventional Subpad compromise for Edge NU and WID Ranges,* Proc. of the 204th ECS Meeting, Orlando, FL, pp. 149–156, ISBN: 1-56677-404-7, (2003)

65. J. Kiihamäki et al., *"Plug-Up" – A new concept for fabricating SOI MEMS devices,* Microsystem Technologies, **10**, 5, pp. 346–350, (2004)

66. M. Bruel, *Silicon on insulator material technology*, Electron. Lett., **31**, 1201, (1995)

67. M. Bruel et al., *Smart-cut: A new silicon on insulator material technology based on hydrogen implantation and wafer bonding*, Jpn. J. Appl. Phys., **36**, 1636, (1997)

68. A. Haapalinna et al., *Rotational grinding of silicon wafers-sub-surfaces damage inspection;* Mat. Sc. & Eng., **B107**, pp. 321–331, (2004)

69. *Werkstoffe der Halbleitertechnik,* ed. by H.-F. Hadamovsky, Leipzig, Germany, (2003)

70. ASTM, *Standard Practice for Detection of Oxidation Induced Defects in Polished Silicon Wafers,* Standard **F1727-02**, ASTM (2002)

71. Xiaolin Xie, D. Boning, *CMP at the Wafer Edge-Modeling the Interaction Between Wafer Edge Geometry and Polish Performance,* Mat. Res. Soc. Symp. Proc., **867**, (2005)

72. J. Gagliardi, *Activating Fixed Abrasives Designed for Direct SON CMP*, SEMI Technical Symposium; Innovations in Semiconductor Manufacturing, San Francisco, Proc., pp. 61–83, (2004)

73. J. Gagliardi, *3M fixed Abrasives for CMP,* Poster presentation, Semicon West, (1997)

74. T. Suni et al., *SOI Wafers with Buried Cavities,* Proc. of ECS Spring Meeting in Quebec, (2005)

75. Q.-Y. Tong, U. Gösele, *Semiconductor Wafer Bonding: science and technology,* John Wiley and Sons; New York; (1999); ISBN: 0-471-57481-3

76. T. Abe, J. H. Matlock, *Wafer Bonding techniques for Silicon-on-insulator technology,* Solid State Technology, **39**, (1990)

77. G. A. Riley, *Wafer-level Hermetic Cavity Packaging,* Advanced Packaging Magazine, **5**, (2004)

78. T. Suni et al., *Wafer Scale Packaging of MEMS by Using Plasma Activated Wafer Bonding,* Proc. of ECS Spring Meeting in Quebec, (2005)

79. J. J. Sniegowski, *Chemical Mechanical Polishing: Enhancing the Manufacturability of MEMS*, SPIE Micromachining and Microfabrication Process Technology, Austin, TX, **2879**, pp. 104–115, (1996)

80. A. A. Yasseen et al., *Chemical-Mechanical Polishing for Polysilicon Surface Micromachining,* J. Electrochem. Soc., **144** (1), pp. 237–242, (1997)

81. Dale L. Hetherington, Jeffry J. Sniegowski, *Improved Polysilicon Surface-micromachined Micromirror Devices using Chemical-mechanical Polishing*, International Symposium on Optical Science, Engineering, and Instrumentation, SPIE's 43rd Annual Meeting, San Diego, CA, (1998)

82. P. A. Krulevitch, *Micromechanical Investigations of Silicon and Ni-Ti-Cu Thin Films,* PhD. thesis, University of Berkely, CA, (1994)

PAPER A

A Novel CMP Process on Fixed Abrasive Pads for the Manufacturing of Highly Planar Thick Film SOI Substrates

In: Materials Research Society Proceedings 2003.
Vol. 767, pp. 133–139.
Reprinted with permission from the publisher.

Mat. Res. Soc. Symp. Proc. Vol. 767 © 2003 Materials Research Society F2.11.1

A novel CMP Process on Fixed Abrasive Pads for the Manufacturing of highly planar thick film SOI Substrates

Martin Kulawski[1]; Kimmo Henttinen[1]; Ilkka Suni[1]; Frauke Weimar[2]; Jari Mäkinen[3]
[1]:VTT Microelectronics, Tietotie 3, P.O. Box 1208, FIN-02044 VTT; Espoo; Finland
[2]:3M Laboratories (Europe); Carl-Schurz-Str.1; D-41453 Neuss; Germany
[3]: Okmetic Oy; Sinimäentie 12; P.O. Box 44; FIN-01301 Vantaa; Finland
Contact: martin.kulawski@vtt.fi

ABSTRACT

A new approach using Fixed Abrasive (FA) pads has been undertaken to overcome the problem of non-uniform thick film Silicon-on-Insulator (SOI) wafers after CMP polishing. The theoretical models indicating the advantages of the 2-body system of the fixed abrasive configuration vs. the conventional 3-body system of slurry based polishing have been convincingly demonstrated in practise upon experiments in a wide range of parameters. As a result it is possible to maintain or improve the flatness of wafers after back grinding, while simultaneously removing the sub-surface damage. A surface quality of prime wafers can be reached on the device layer. Capacitive thickness measurement scans and atomic force microscopy (AFM) monitoring confirm the results. A detailed comparison with conventional processing has been carried out to clarify the advantages on bulk silicon wafers. Decoration etching is used to analyse the wafer surface quality in terms of oxide induced stacking faults (OISF). As a result an alternative processing method is proposed for manufacturing thick film SOI substrates with improved uniformity.

INTRODUCTION

The manufacturing of thick film silicon-on-insulator (SOI) substrates requires a significant amount of mechanical treatment. In thin film SOI production the SmartCut™ process leaves an already highly uniform surface, which only requires a small amount of polishing if at all [1]. Processing of thick film SOI however requires extensive grinding and polishing to remove most of the bonded device wafer. Therefore, care has to be taken for the non-uniformity of the thinning processes. While grinding leads to a TTV (Total Thickness Variation) of 0,5 µm on the wafer it leaves a sub-surface damage (SSD) of up to 6 µm deep in the substrate, which has to be removed by subsequent chemical mechanical polishing (CMP). The conventional slurry based processing however often leads to high values of thickness non-uniformity due to the strong bias for rounding the edge of the thick device layer with reduced diameter on top of the handle wafer. Since the specs for SOI-wafers at the time are more and more demanding with TTV values of < 0,5µm at EE (Edge Exclusion) of < 3mm, the conventional processing for highly planar SOI wafers often results in low yields or is not working at all. To overcome this obstacle polishing of ground wafers on so-called fixed abrasive (FA) pads has been investigated in order to improve the CMP process performance and maintain the flatness of the SOI substrate.

EXPERIMENTAL

Polishing was done on a Strasbaugh 6DS-SP Planarizer with 4” wafers ground on a Strasbaugh 7AF backgrinding tool equipped with a #325 coarse wheel and a #2000 fine wheel providing a TTV value of < 0,5 µm. Experimental FA Pads from 3M were used for the polishing. The pads possessed a microreplicated pattern of 200µm wide and 50 µm high posts containing the abrasive material in a resin-like matrix. The density of posts results in a total contact area of around 10% of the entire wafer surface, thus a higher local pressure under the posts on the wafer is achieved. The 3M pads consisted of the fixed abrasive layer stacked on a rigid layer followed by a resilient layer finished by a standard self adhesive for mounting on the polishing platten of the CMP tool. Instead of slurry a lubrication liquid containig DI water with base chemicals for pH value adjustments was applied to the pad during polishing. The time was set to 300s in general but doubled in some cases for long term studies. Starting from a standard parameter set downforce and rotation speed were varied in wide ranges in order to evaluate the potential of the pad. Also the pH-values have been varied under the tests.

THEORY

While under conventional polishing the abrasive particles can reach the complete exposed surface of the wafer, removal occurs both on the elevated and the lower areas. Thus a polishing cycle results in a higher material removal until the entire area is planarized. Also the exact defined edges of the substrate (especially in the caes of the SOI device layer) are attacked by the particles in the slurry film being pressed onto the surface by the bending compressable pad. Removal in conventional CMP thus occurs via the so-called 3 body interaction.

In the case of SlurryFree™ polishing the abrasive particle is bound in the elevated posts of the pad. Thus removal resulting contact is mainly occuring at the elevated areas of the exposed surface. The removal rate ratio between higher and lower areas of the wafer is much higher than in the case of slurry based CMP. A much more effective planarization effect is expected and the overall necessary material removal for complete planarization is minimized. For the fixed abrasive pad removal mechanism one speaks of a 2-body system (See Figure 1).

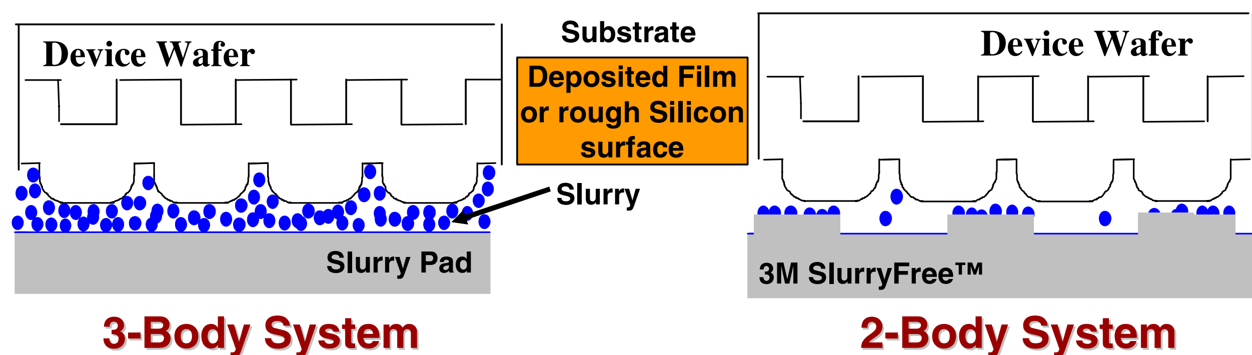


Figure 1. Schematic comparision of the conventional CMP Process and the Fixed Abrasive case

DISCUSSION

First Tests

In figure 2 a summary of various process parameter settings is shown in terms of TTV degeneration (d-TTV) and total removal. As comparison the d-TTV value of 0,76 µm for a conventional CMP step with a 5 µm removal is shown. As one can see the d-TTV value stays well around 0 µm in nearly all parameter settings thus maintaining the superior TTV values of < 0,5µm of the incoming material. However a total removal of 1,3 µm is not exceeded in any case. The calculated removal rate (RR), 0,1-0,2 µm/min is far below the expected 1µm/min of conventional CMP.

Calculating the Non-Uniformity of the removal (NU) however one can see in figure 3 that the achieved values for fixed abrasive polishing are well around 5%. This is a strong improvement compared the reference value of 15% NU in the case of slurry based CMP.

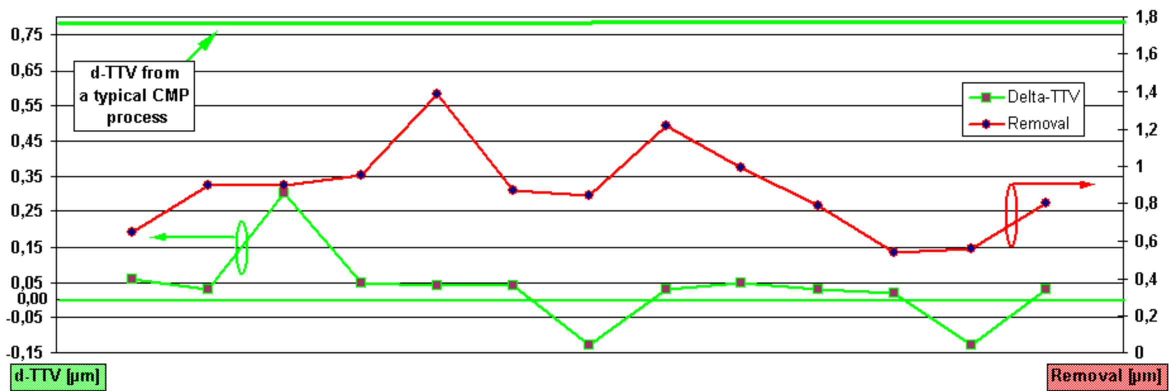


Figure 2. A nearly neutral TTV behavior is visible, while the overall removal is limited

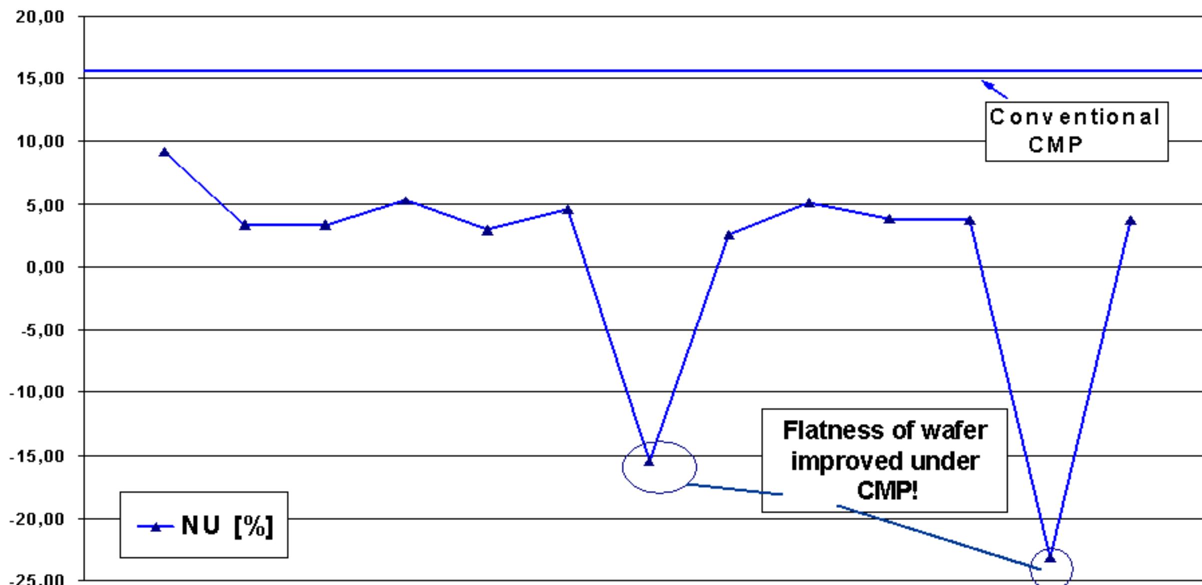


Figure 3. NU of FA pads shows only a third of the value achieved in slurry based CMP

It can be stated that the fixed abrasive technology indeed provides exellent planarization. In terms of TTV degeneration good results are achieved in a wide process window. However the process stopped after the roughness of the surface was eliminated and no further removal could be achieved. In most cases the grindlines were invisible after a 1 µm removal comparing to a minimum of 3 µm in slurry based CMP. For the removal of the deeper laying sub-surface damage (SSD) a ”blank-rate” would be needed and also an increase of the achievable RR would be beneficial in order to limit the needed polishing time.

Second Generation fixed abrasive Pads

Further development was leading to set of FA pads, which is providing improvements in the needed areas. Now a total removal of more than 2,5 µm was achieved while the NU of removal was still low varying in between 1,4-9,7% (see Figure 4). The RR could be increased to 0,35 µm/min by increasing the downforce while lowering the pH-value of the applied lubrication liquid. As major factor for the RR optimization the pH-value of the applied lubrication liquid was identified. Splitting the long process steps of 10 min into 5+5 min resulted in pad blunting since smooth wafers could not provide a sufficient re-conditioning of the abrasive posts, while the single step long time polish could maintain a reasonable RR (figure 5). A dull pad however could be recovered by polishing one rough as-ground wafer and then the original RR level was reached again.

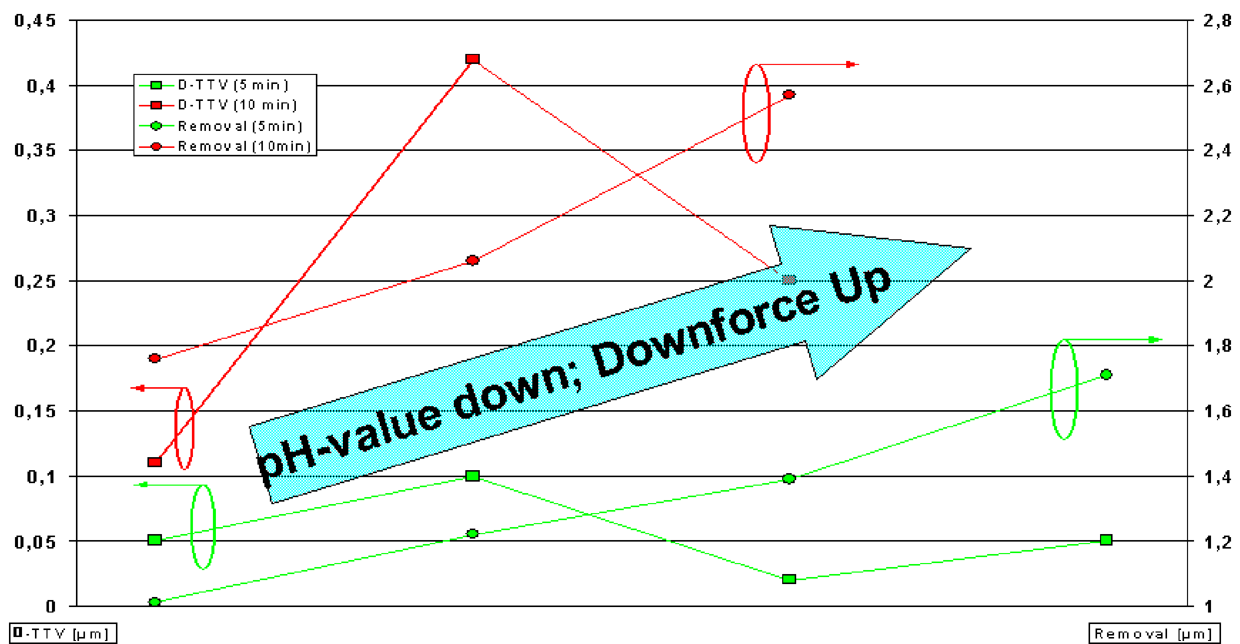


Figure 4. Second generation fixed abrasive pads provide a higher total removal while the d-TTV behavior stays better than in slurry based CMP.

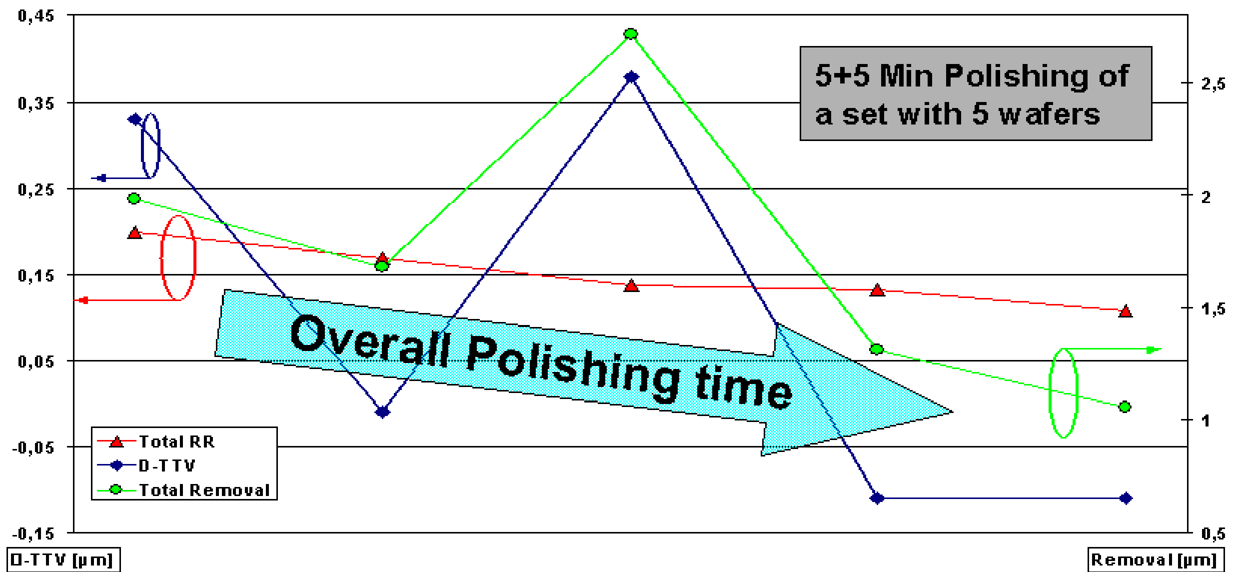


Figure 5. Splitting the process step results in pad blunting but the TTV value is maintained

Surface Quality

The surface quality was analysed by AFM. In figure 6 the as-ground silicon surface is on the left while a FA polished wafer is shown on the right. It can be clearly seen that all grindlines are removed and coming from an rms roughness value of more than 15 nm reaching a superior surface quality with a roughness of below 0,8 nm after only 1 µm removal. This indicates that even the final polishing step for haze removal can be reduced when using FA polishing instead of conventional CMP in the stockremoval process.

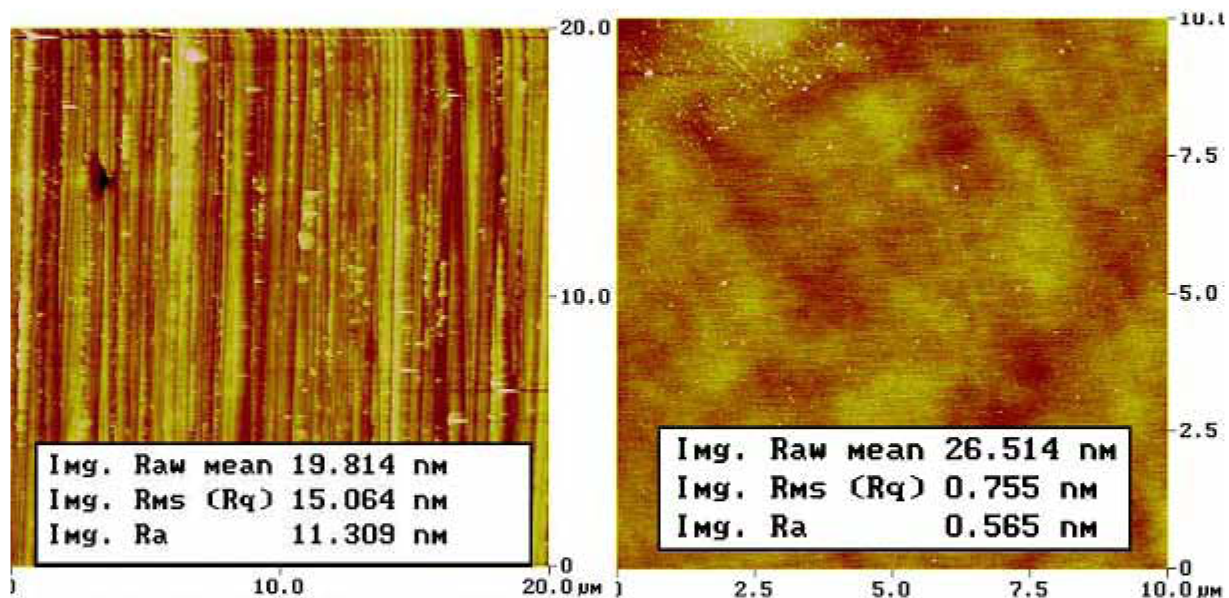


Figure 6. Comparison of AFM scans post grinding and post fixed abrasive polishing. A strong improvement of the roughn ess values is obtained

Improved fine Grinding

While being able to already remove more than 2,5 µm of damaged Silicon with the second gneration FA pads still at least another 3 µm would be needed in order to eliminate all SSD induced by the conventional grinding procedure.

In another test different fine grinding techniques were compared including new grinding wheels. Polishing down stepwise after grinding followed by decoration etching the level of oxide induced stacking faults (OISF) were compared. It could be shown that with advanced fine grinding wheels the reference level of OISF was already reached when removing 3 µm of silicon compared to the standard 6-7 µm in conventional grinding.

This advanced fine grinding enables the reduction of the necessary CMP removal so that further processing with second generation fixed abrasive is feasible.

CONCLUSIONS

With the new approach of using fixed abrasive pads for polishing instead of slurry based CMP for ground silicon wafers it has been shown that strong improvements in terms of TTV degeneration can be achieved. The TTV level of 0,5 µm was maintained in many cases while the surface roughness could be reduced to a level of below 0,8 nm. The second generation fixed abrasive pads also provide the capability of removing more than 2,5 µm with removal rates of up to 0,35 µm/min. In combination with an advanced grinding technology providing a sub-surface damage level of below 3 µm instead of 6-7 µm in conventional grinding the surface can reach prime wafer level in terms of crystal defects. The superior surface quality after the fixed abrasive polish further enables the reduction of the final haze removal polish providing the possibility of even more flat wafers.

With further work a deeper understanding of the overall process shall be gained and after long term tests and stability runs a real alternative process for highly planar thick film SOI substrates can be enabled.

ACKNOWLEDGMENTS

The authors would like to thank the U.S. team of 3M for the conribution of the fixed abrasive pads and the fruitful discussions.

REFERENCES

[1]: FRANCOIS J. HENLEY & MICHAEL I. CURRENT, Semiconductor Fabtech, 12th Edition, PP.204

PAPER B

Advances in the CMP Process on Fixed Abrasive Pads for the Polishing of SOI-Substrates with High Degree of Flatness

In: Materials Research Society Proceedings 2004.
Vol. 816, pp. 191–196.
Reprinted with permission from the publisher.

Advances in the CMP Process on Fixed Abrasive Pads for the Polishing of SOI-Substrates with High Degree of Flatness

Martin Kulawski[1]; Hannu Luoto[1]; Kimmo Henttinen[1]; Ilkka Suni[1]; Frauke Weimar[2]; Jari Mäkinen[3]
[1]:VTT Microelectronics, Tietotie 3, P.O. Box 1208, FIN-02044 VTT; Espoo; Finland
[2]:3M Deutschland GmbH; Carl-Schurz-Str.1; D-41453 Neuss; Germany
[3]:Okmetic Oy; Piitie 2; P.O. Box 44; FIN-01301 Vantaa; Finland
Contact: martin.kulawski@vtt.fi

ABSTRACT

The new approach using Fixed Abrasive (FA) pads for polishing thick film Silicon-on-Insulator (SOI) wafers after bonding and grinding process [1] has been further developed. The aim is a practicable industrial manufacturing process, where the major specifications especially in long term stability and removal rate should be achieved. In base line studies a stable removal rate on suitable level has been reached, while the degeneration of the total thickness variation (TTV) was limited to a clearly smaller value than that being typical for the standard stock removal polishing. The overall removal in these tests was adjusted to 2-3 µm, which removes all sub surface damage (SSD) from wafers ground by ultra fine grinding wheels with very small average abrasive particle size. The process has been able to remove all visible grindlines after removing less than 1.5 µm. In another test with a further developed high density FA pad, removal rates up to ~0.6 µm/min were achieved. The polished samples were further processed and characterized by capacitive thickness measurements gauges, optical surface inspection tool ("Magic mirror"), atomic force microscopy (AFM) and optical reflection measurements.

INTRODUCTION

The manufacturing of thick film silicon-on-insulator (SOI) substrates currently faces a limitation when concerning low TTV values. While grinding tools are able to provide wafers with flatness values of less than 0,5 µm TTV, the subsequent polishing needed for removing the grindlines as well as SSD often degenerates the wafers to a level above 1 µm TTV. This is caused first by the high amount of material removal needed in order to remove all damage and residues from conventional grinding and second by the inability of conventional polishing to take care of the special edge shape formed during the SOI manufacturing process. A strong emphasis to round the edge of the SOI device layer can be seen. Together with the general non-uniformity of the process this results in elevated TTV values when applying the often required stringent edge exclusion of 3 mm based on the handle wafer diameter. Due to the required edge grinding of the upper device wafer this often leads to an actual edge exclusion of only 1 mm to be met for the CMP processing.

The introduced combination of grinding with ultra fine wheels leading to low SSD and the use of FA pads leads to strongly reduced material removal being needed by polishing on the one hand and to greatly increased uniformity due to the extreme good capability of FA pads for planarization and uniform removal on the other hand.

EXPERIMENTAL

Polishing was done on a Strasbaugh 6DS-SP Planarizer with 6” wafers ground on a Strasbaugh 7AF back grinding tool equipped with a #325 coarse wheel. Fine grinding was done mainly on #4000 fine wheel, providing a reduced sub surface damage (SSD). The resulting TTV was ~0.7 µm. Experimental FA Pads, further developed towards the needs of silicon polishing from 3M were used for CMP. The micro replicated posts on the surface were about 125µm wide and 50 µm high, containing the abrasive material in a resin-like matrix. The density of posts resulted in around 10% contact area with the wafer under processing and about 30% contact area for the high density pad version respectively. The polishing time was typically set to be 300s but varied in some cases for removal rate studies. The prior developed standard parameter set [1] was further adjusted in order to optimize removal rate and stability of the process. Also the pH-values have been varied to investigate the process behavior and to find the optimum point for effective processing.

PRINCIPLE MECHANISMS

First tests with FA pads showed already good values, both in terms of TTV as well as removal rate. This performance however has to be ensured for the entire lifetime of the pad. While conventional pads are continuously conditioned to provide a clean and defined surface, fixed abrasive pads are self-conditioning. As the used particles are leaving the posts in which they are embedded, the surrounding matrix material has to wear off with appropriate rate in order to always expose sufficient amount of fresh abrasives. The correct balance of this procedure has to be found for each process application the FA pads are used for. On the other hand the wear rate of the matrix material should provide a decent lifetime of the pads in order to keep costs reasonable.

Besides the mechanical also the chemical part plays a major role in the adjustment of the removal rate. On FA processes it has been seen that the pH-value of the used lubricant is of great influence [1]. In conventional silica-slurry polishing of silicon a strong peak in removal rate at pH ~11 [2] has been found. As ceria (CeO_2) particles are in use with fixed abrasive pads, a different mechanism of removal can be expected. It is known that ceria supports the removal of silicon oxide [3] and FA processing on oxide resulted in elevated removal rates pH ~12 [4]. From the investigation about pH dependence of silicon removal it is suggested that for higher pH than 11 a different mechanism of removal takes place, involving intermediate oxide and silanol formation [2]. An optimized removal rate for silicon FA CMP is thus expected at different pH.

RESULTS AND DISCUSSION

First baseline polishing Tests

After the first encouraging results [1], long term stability has been evaluated with more wafers. The conditions of the process have been kept at similar level in order to obtain changes in the pads’ behavior. Removal and uniformity were measured for fresh pad as well as for a pad being used for around 8 hours and 30 minutes referring to polishing about 100 silicon wafers.

While the uniformity showed continues superior behavior, the removal rate dropped from 0.4 µm/min to about 0.2 µm/min, only half of the promising starting value.

The reason for this degeneration in removal rate was investigated by SEM analysis of the used pad. It was clearly seen that the posts were wearing off under processing as expected. However the density of exposed abrasive particles seemed to be lower on used areas, when observing the posts in detail (Figure 1). After this feed back to 3M, another pad with slightly different formulation (Pad B) was provided for further base line polishing studies.

Base line processing with Pad B and adjusted process parameters

Pad B was further used with slightly adjusted set of process parameters. Nearly 100 Wafers were polished under similar conditions and removal rates, total removal and TTV was studied. Under processing the pH-value of the lubrication liquid was varied from pH 11.5 – 12.5 to find the optimum value. As seen from Figure 2, very stable processing in terms of removal rate was achieved. The only existing variation is caused by different pH-values of the lubrication liquid in the single runs (indicated by the vertical black lines; Fig. 2); an aging effect was not seen.

Within single test runs under constant pH-value, removal rate uniformities of below 1% were seen, responding to 60 nm total variation. The strong influence of the pH-value is visible, however a mean removal rate of clearly above 0.3 µm/min was reached at all times. When plotting the removal rate versus the pH-value, a peak similar to conventional slurry-based CMP [2] is visible, but around pH 11.9 (see Figure 3).

The TTV indicates as well a stable process, even though the incoming material was not flat enough to present the benefits of FA to full extent (Fig. 4). Many wafers improved in TTV.

Also time was varied during the base line run as well as both ground and previously polished wafers were processed to study the so-called bulk rate of the process. Figure 5 shows, that a constantly high bulk rate is achieved with the FA pad under investigation, independent of process time. The removal can thus be adjusted according to the needs of the substrates (Figure 6). Finally, an FA pad with increased contact area (30% instead of 10%) was tested. The removal rate was 40% higher, while the pad showed similar behavior in terms of TTV.

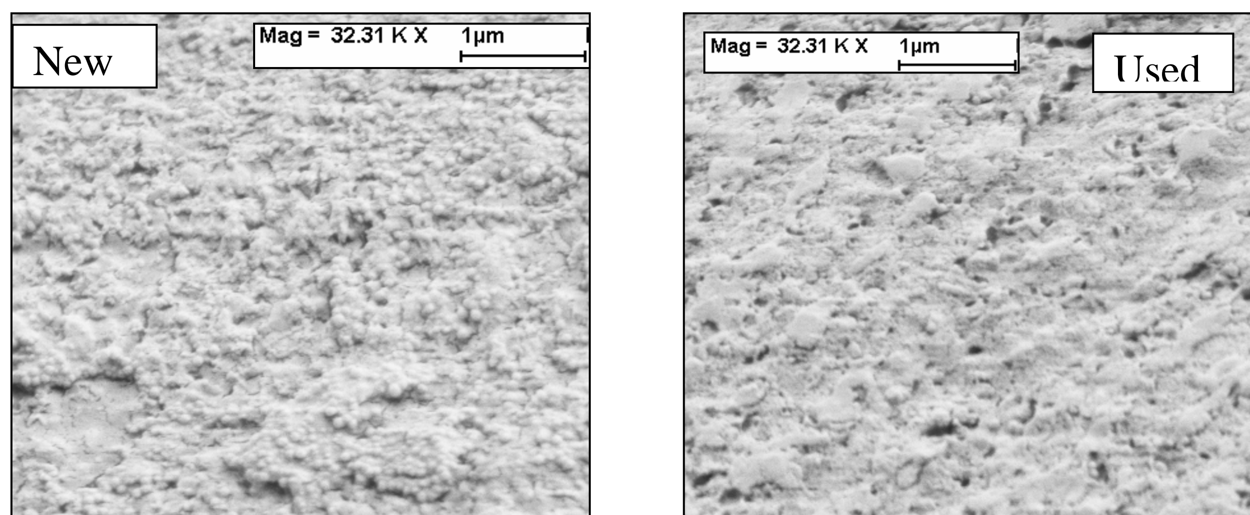


Figure 1: SEM images of new and used posts of the FA pad. More abrasive particles on the left.

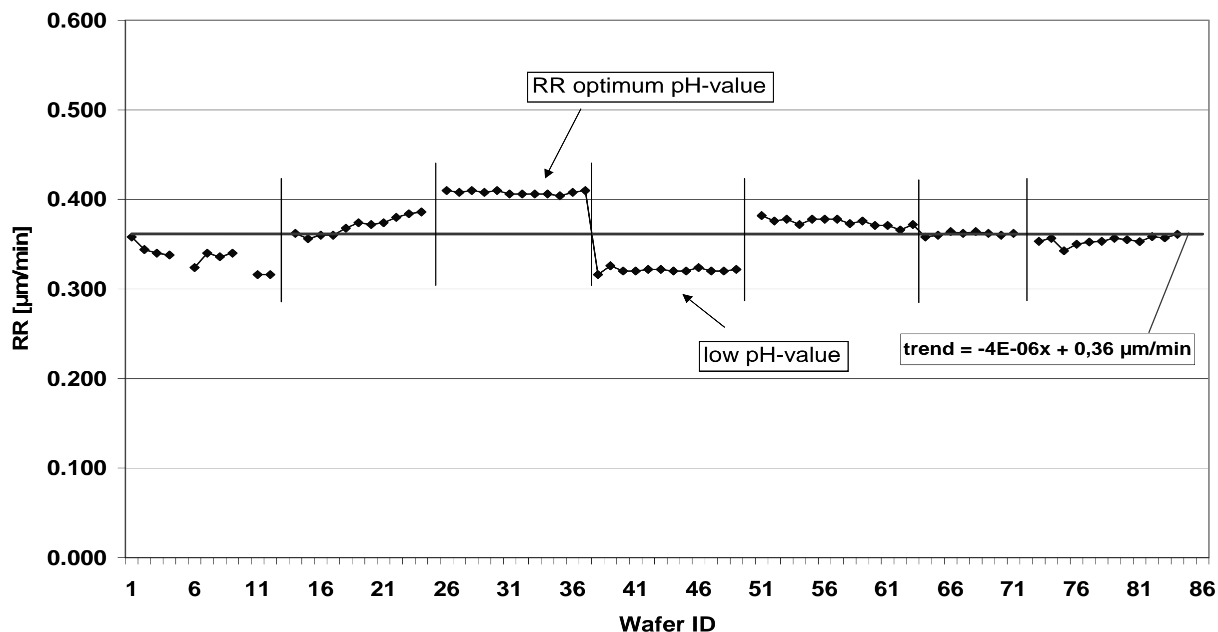


Figure 2: Base line removal rate with FA pad (Pad B). A stable RR is achieved varied only by the change of pH-value.

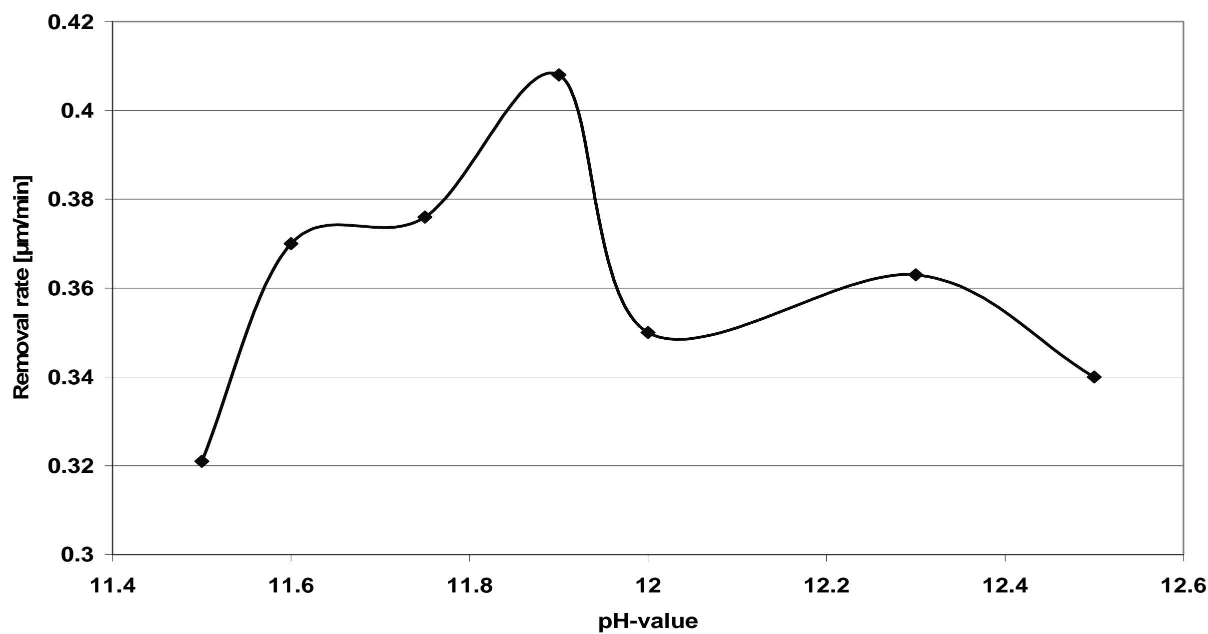


Figure 3: Dependence of the removal rate on pH-value of the lubrication liquid.

Confidence about the extraordinary planarization capabilities of FA pads was gained, when inspecting wafers after 4 minutes polishing in the “Magic Mirror”. This sensitive optical surface inspection tool shows smallest curvature on the wafer, like remaining grindlines and is used frequently for adjusting the necessary removal for high finished surfaces. While, in conventional polishing more than 5 µm material removal for damage-free surfaces are needed, about 1.3 µm removal was enough for fixed abrasive polishing to take off all visible grind marks (Fig. 5).

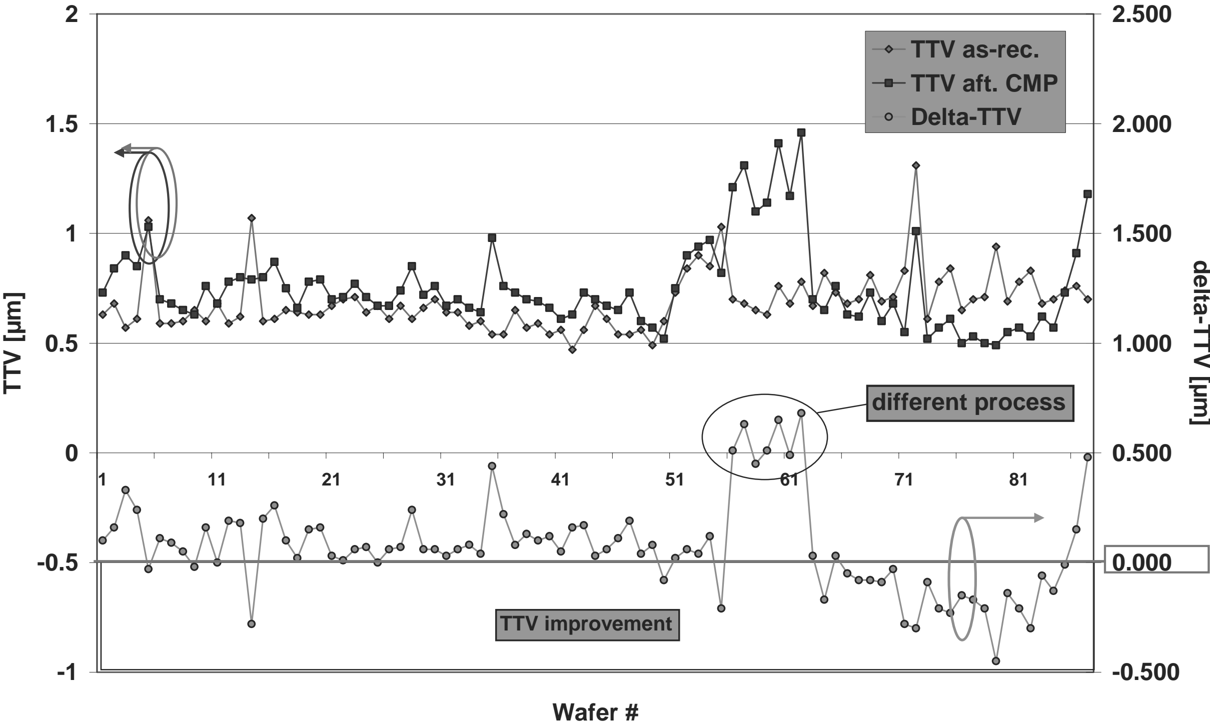


Figure 4: TTV and its change under FA polishing. Untypical for conventional processing is the bigger amount of wafers with improved flatness after CMP.

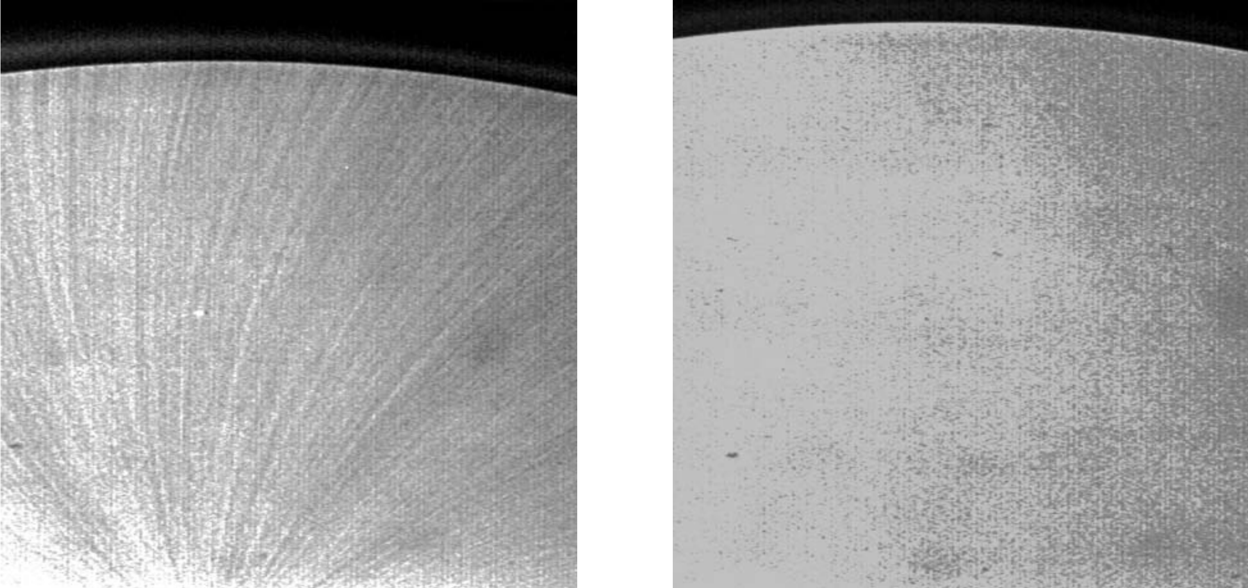


Figure 5: Magic Mirror images of a ground wafer (left) and a wafer being polished by FA for 240s (right). After less than 1.5 µm removal all grindlines have vanished, while conventional slurry-based polishing with standard pad requires more than 5 µm for total damage removal.

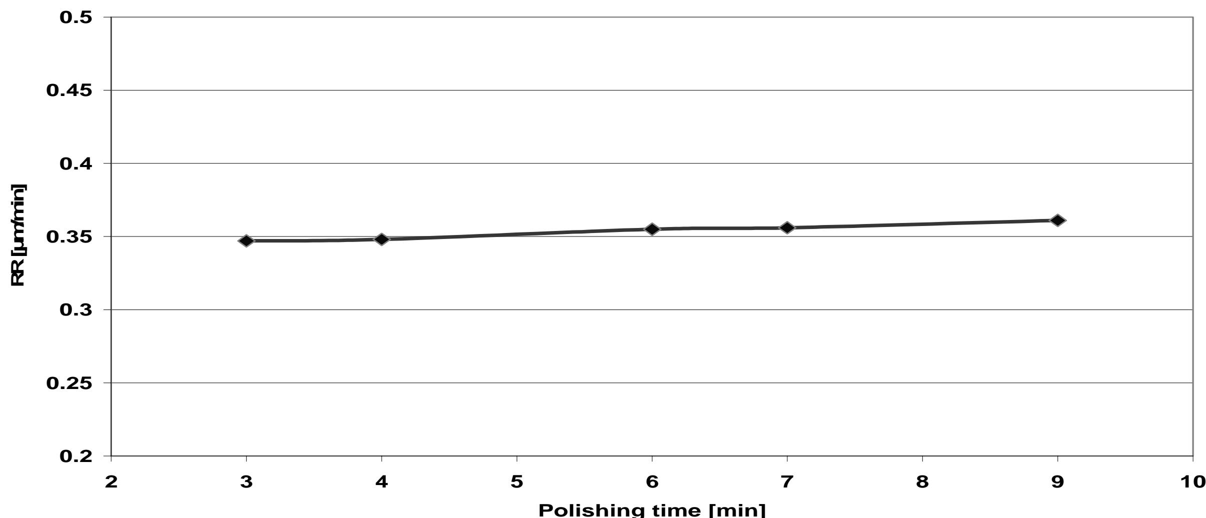


Figure 6: The removal rate of FA polishing is almost independent from the processing time.

CONCLUSIONS

The fixed abrasive polishing for silicon - especially SOI- has been developed further. Long term stability can be reached while TTV behavior of the process is still superior. With high density FA pads removal rates of standard silicon polishing can be reached, while simultaneously removal is independent from the applied processing time. A stable bulk removal can be observed. With the seen pH dependence of the removal rate it is suggested, that the mechanism of abrading silicon is of different nature than in conventional polishing, suggesting more detailed studies. The surface quality of the polished material is also of very high level. After less than 1,5 µm removal, grindlines are not visible anymore in the Magic Mirror. Together with the newly established grinding process with ultra fine wheels (#4000 and higher) the total needed polishing amount can be greatly reduced leading to very flat thick film SOI-substrates.

ACKNOWLEDGMENTS

The authors would like to thank the U.S. team of 3M for the contribution of the fixed abrasive pads and fruitful discussions, as well as Dr. Jyrki Molarius from VTT for his valuable advises while revising the manuscript to its present form.

REFERENCES

[1]: Kulawski et al. in *A novel CMP Process on Fixed Abrasive Pads for Manufacturing of highly planar thick film SOI Substrates,* ed. by D. S. Boning, K. Devrient, M. R. Oliver D. J. Stein, I. Vos, (Mater. Res. Soc. Proc**. 767,** Warrendale, PA, 2003) pp. 133-139
[2]: G. J. Pietsch et al., Surface Science **331-333**, 395-401 (1995)
[3]: J. M. Steigerwald; S. P. Muraka; R. J. Gutmann, *Chemical Mechanical Planarization of Microelectronic Materials* (John Wiley & Sons Inc. NY 1997), pp. 140
[4]: J.Gagliardi, *3M Fixed Abrasives for CMP,* Poster presentation, Semicon West (1997)

PAPER C

Integration of CMP Fixed Abrasive Polishing into the Manufacturing of Thick Film SOI Substrates

In: Materials Research Society Proceedings 2005.
Vol. 867, pp. 111–116.
Reprinted with permission from the publisher.

Integration of CMP Fixed Abrasive Polishing into the Manufacturing of Thick Film SOI Substrates

Martin Kulawski[1]; Hannu Luoto[1]; Kimmo Henttinen[1]; Tommi Suni[1]; Frauke Weimar[2]; Jari Mäkinen[3]
[1]:VTT Microelectronics, Tietotie 3, P.O. Box 1208, FIN-02044 VTT; Espoo; Finland
[2]:3M Deutschland GmbH; Carl-Schurz-Str.1; D-41453 Neuss; Germany
[3]:Okmetic Oy; Piitie 2; P.O. Box 44; FIN-01301 Vantaa; Finland
Contact: martin.kulawski@vtt.fi

ABSTRACT

The specification for the total thickness variation (TTV) of the device layers on thick-film silicon on insulator (SOI) wafers tighten for future applications. Therefore, the bulk removal polishing process of current technology after grinding cannot meet the demands in terms of flatness. The currently required amount of material removal for polishing out the induced sub surface damage (SSD) of the grinding is very high. Additionally, slurry-based CMP processes show unsatisfactory grindline and topography removal. This in turn reflects negatively to processing times, throughput and overall flatness performance.

Encouraging early results of FA pad use for silicon and SOI polishing have already been further developed [1]. Low SSD grinding has been introduced to silicon manufacturing [1]. In this work, an integrated manufacturing process sequence is presented. Starting from low SSD grinding of the bonded SOI wafer couple, an optimized FA CMP step is replacing the conventional bulk polishing with reduced removal. The SSD after FA CMP is investigated by oxide induced stacking fault (OISF) method [2] and results are used to adjust the final polishing step of the substrates. The overall process sequence is highly advantageous in terms of performance in TTV and provides a highly competitive and effective method for achieving best possible surface quality with minimized total silicon removal. This method is not only useful for SOI wafers but also in other areas of silicon processing.

INTRODUCTION

When making thick film SOI substrates a significant amount of mechanical treatment on wafers has to be done. Unlike in thin film SOI the device layer of the wafer has to be formed by removing most of the bonded top substrate during grinding and subsequent polishing. Grinding is used to adjust the required thickness, which can vary from 1 µm to more than 100 µm. Grinding leads to very flat wafers, however it leaves not only mechanical abrasion lines, but also introduces a several microns deep layer with crystalline defects [4, 5]. Therefore, subsequent polishing is needed to provide a smooth and defect-free device layer surface. Conventional slurry-based CMP leads to unsatisfactory results in terms of TTV, as the edge of the slightly smaller device layer is rounded under the removal of the damaged layer. As the required polishing amount is increasing, the TTV degenerates. Currently a polishing removal of 5 µm is needed for slurry-based CMP to remove all grindlines and 6 to 8µm is necessary to remove all crystalline damage from standard grinding processes [1].

For achieving flat thick film SOI wafers it is therefore important to minimize the overall CMP removal by reducing the SSD layer and simultaneously optimizing the polishing process for more effective grindline removal. New grinding wheel technology provides wheels, which will induce a shallower SSD layer as has been shown earlier [3]. With the fixed abrasive technology, an appropriate method has been found to avoid edge rounding under polishing and to remove grind lines much more effectively than in conventional CMP [1].

When integrating these new approaches into a manufacturing sequence the resulting surface quality is essential. After stock polishing, only little material is removed by final polishing in order to provide best surface roughness and haze removal. In this study the influence of replacing the conventional grinding and polishing on the overall manufacturing sequence is analysed. Low-SSD grinding and FA CMP are used. The surface quality is analysed after different final polishing times for remaining damage.

EXPERIMENTAL

Polishing was done on a Strasbaugh 6DS-SP Planarizer on 6" bonded and edge-ground wafer couples, which were thinned by a Strasbaugh 7AF back-grinding tool equipped with a #325 coarse wheel by Norton. Prior to polishing also fine grinding was done on #4000 fine wheel from DISCO, providing a reduced sub surface damage (SSD). The resulting TTV was ~0.5µm. Experimental FA Pads from 3M were used for CMP. The micro replicated posts of these pads were about 125µm wide and 50 µm high, containing ceria abrasives in a resin-like matrix. The density of posts resulted in around 10% contact area during processing. Polishing time was set to be 300s, in some cases 360s. The previously optimized parameter set [1] was used in the process. Final polishing was done on commercially available polishing pads with commercially available polishing slurry under different times. The resulting removal was varying between 0.2 and 0.6 µm. A set of wafers was then investigated by OISF method for stacking faults. Wafers were measured by ADE capacitive measurement gauge for thickness and TTV performance.

RESULTS AND DISCUSSION

Thinning of the bonded wafer couples

A set of 15 wafers was ground to a device layer thickness of about 53 µm, leaving 3 µm for subsequent grindline and crystal damage removal by CMP. The achieved average thickness was 52.79 µm with a standard deviation of 0.66% indicating a stable grinding process. Average TTV of the wafers was 0.46 µm providing very flat starting material for the polishing trials.

Fixed Abrasive and final polishing

Ground wafers were then polished by fixed abrasive pad. The removal was set to be about 2.5 µm. A subsequent final polishing step removed another 0.5 µm. Figure 1 shows a typical result after FA polishing step. No edge rounding is visible rather slight centre fast removal behaviour is detected. In Figure 2 a typical result is shown after final polishing. No bigger influence on the flatness is obtained and the overall wafer remains significantly below 1 µm

TTV. Table 1 gives an overview on the performance of the entire wafer set. All wafers are below 1 µm TTV with an average value of 0.78 µm. As can be seen from figures 1 and 2 the edge exclusion used in the measurements is 3 mm. With an edge grinding process removing around 1.7 mm, this results in a SOI layer edge exclusion of 1.3 mm.

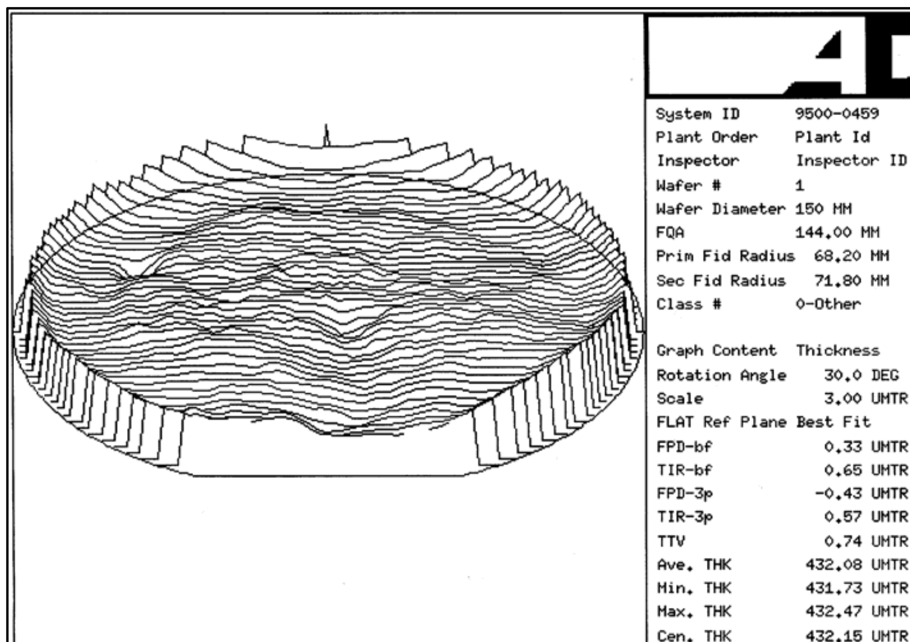


Figure 1: Capacitive thickness scan of the FA polished wafer. No edge rounding is visible. The overall TTV is well below 1 µm

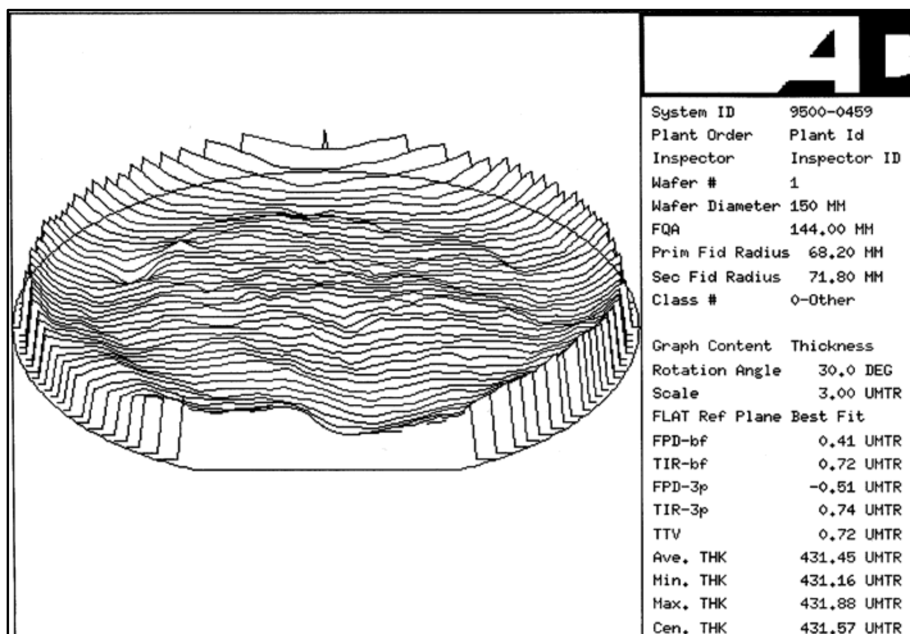


Figure 2: After final polishing and further 0.5 µm removal the wafer is still very flat. The last polishing step does not strongly influence the result.

Table 1: Overview of the performance of the combined grinding and polishing sequence. All wafers are well below 1 µm TTV and the goal thickness of 50 µm is well achieved.

	SOI-layer thickness after grinding:		sd		Thickness after CMP:	TTV after CMP:
1		52.2	0.19		50.05	0.72
2		52.94	0.17		49.95	0.69
3		53.36	0.09		50.03	0.91
4		52.89	0.24		49.39	0.94
5		52.82	0.11		49.46	0.94
6		52.36	0.12		49.48	0.81
7		53	0.2		50.27	0.67
8		53.13	0.13		50.35	0.81
9		52.79	0.18		49.98	0.9
10		52.57	0.2		49.79	0.81
11		53.16	0.2		50.38	0.77
12		53.02	0.16		50.29	0.64
13		52.47	0.09		49.72	0.69
14		52.16	0.19		49.43	0.84
15		52.94	0.12		50.2	0.68
	sd	0.35			0.34	0.10
	av	52.79			49.918	0.788
	sd [%]	0.66			0.68	

Surface damage after FA polishing

A set of wafers was used after FA and final polishing for further surface analysis. As the process involves a rather rigid abrasive containing post rather than a soft polishing cloth, it was expected, that the process might induce defects to the surface. Depending on the depth of those defects an intermediate polishing step would be required to remove the defects before final polishing can take place. This in turn would complicate the integration of FA CMP into any manufacturing sequence. Using a standard final polishing procedure process time was increased stepwise up to 300s, which refers to a typical value. A maximum removal of 0.6 µm was achieved. With the high sensitivity of OISF analysis, all defects should be revealed. Figure 3 shows the result of the OISF analysis involving a diameter scan. After decoration procedure, the wafer is scanned along its diameter and defects are counted by optical inspection. The total count is then processed for comparison.

As expected the FA polishing leads to a high number of defects covering the surface. However, these defects are of very shallow nature. Already after 120s of final polishing, most defects are gone (FA+120s in Figure 3). As the final polishing time is increased towards standard value of 300s and removal of 0.5 µm is reached, the fixed abrasive processed wafers have no significant defect level anymore. For reference two prime quality wafers were analyzed simultaneously, showing (Figure 3) that indeed normal defect density level is achieved after 300s final polishing.

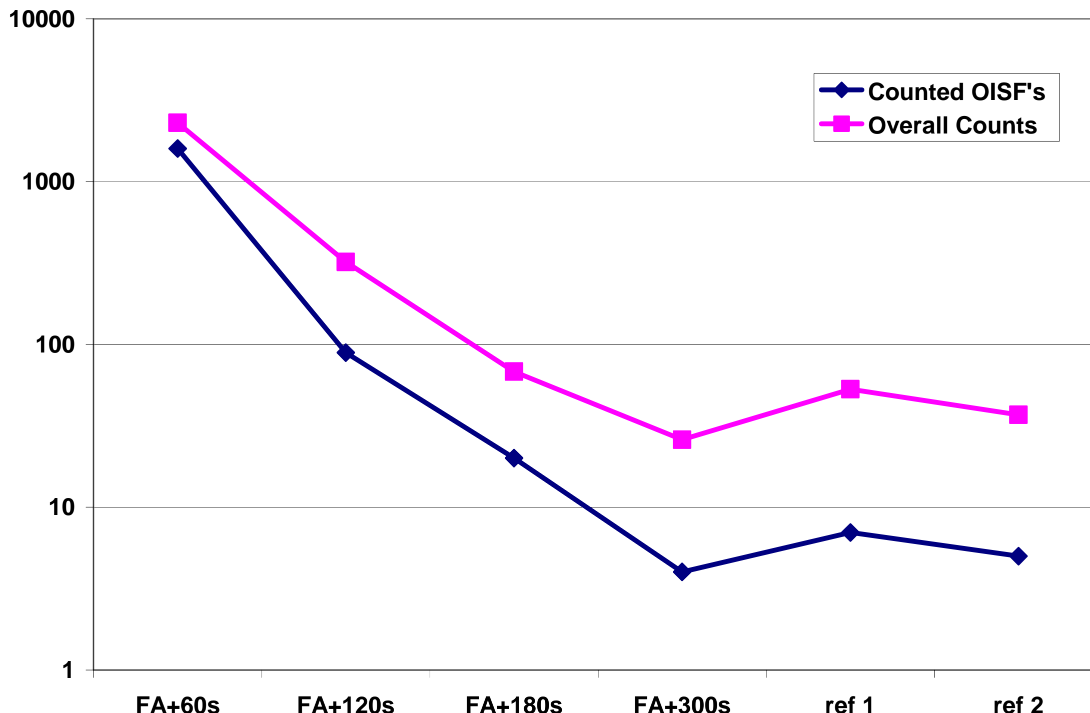


Figure 3: OISF counts on a diameter scan after different final polishing times. The count decreases rapidly with increasing the final polishing time and reaches reference level after 300s referring to 0.5 µm removal.

Process integration

With the above results, it is feasible to compare the standard manufacturing procedure of thick film SOI wafer production with the modified sequence. This is done in Table 2. The advantage of the new process sequence is evident. In best case situation for the typical standard process, the performance is still not as good as the average fixed abrasive and low-SSD grinding sequence and process time or throughput are even or better for the new process.

Table 2: Performance comparison of the new sequence with typical standard manufacturing

THICK FILM SOI:	**STANDARD SEQUENCE**	**LOW-SSD GRINDING AND FIXED ABRASIVE**
Typical required CMP Removal after Grinding	6.5- 8 µm	3- 3.5 µm
Achieved TTV	>1.0- 2.5 µm	0.5- 1.0 µm
Qualified Edge Exclusion (SOI-Layer)	3.0- 4.5 mm	1.5- 2.5 mm
Typical Removal Rate	0.5- 0.8 µm	~0.4 µm
Final Polishing Removal	0.5 µm	0.5 µm

CONCLUSIONS

The fixed abrasive polishing for silicon - especially SOI- has been successfully integrated in feasible industrial manufacturing sequence. Low SSD fine grinding enabled the total required removal after grinding to be reduced to around 3 µm. This corresponds to a reduction of more than 50% of the usual polishing depth. Besides a clearly beneficial behavior in terms of TTV, this also implies a tremendous improvement in throughput for already installed polishing lines in SOI manufacturing. The FA polishing step induced SSD has been identified to be very shallow. The regular final polishing step is able to remove the defects within typical polishing times and no additional polishing step is required. Thus, FA polishing can serve as a full replacement of the standard stock polishing step without any further need of extra processing steps or major modifications elsewhere in the manufacturing process of thick-film SOI substrates. The process can also be utilized in other areas of substrate manufacturing, when a high degree of flatness is required and effective planarization of rough surfaces with good throughput is of importance.

ACKNOWLEDGMENTS

The authors would like to thank the U.S. team of 3M for the contribution of the fixed abrasive pads and fruitful discussions, as well as Dr. Jyrki Molarius from VTT for his valuable advise while revising the manuscript to its present form. Furthermore, the authors would like to thank the Finnish Governmental Funding Organization TEKES for supporting this study under the CMP Development project.

REFERENCES

[1]: Kulawski et al. in *Advances in the CMP Process on Fixed Abrasive Pads for the Polishing of SOI substrates with high Degree of Flatness,* ed. by D. S. Boning, J. W. Bartha, A. Philipossion, G.Shinn, I. Vos, (Mater. Res. Soc. Proc**. 816,** Warrendale, PA, 2004) pp. 191-196

[2]: ASTM, Standard F1727-02: *Standard Practice for Detection of Oxidation Induced Defects in Polished Silicon Wafers*, ASTM 2002

[3]: Kulawski et al. in *A novel CMP Process on Fixed Abrasive Pads for Manufacturing of highly planar thick film SOI Substrates,* ed. by D. S. Boning, K. Devrient, M. R. Oliver D. J. Stein, I. Vos, (Mater. Res. Soc. Proc**. 767,** Warrendale, PA, 2003) pp. 133-139

[4]: A.Haapalinna et al. in *Rotational grinding of silicon wafers- sub-surface damage inspection,* Mat. Sc. & En. B107 (2004), 321-331

[5]: *Werkstoffe der Halbleitertechnik,*ed. by H.-F. Hadamovsky, Leipzig, Germany, 2003

PAPER D

Polishing of Bulk Micro-Machined Substrates by Fixed Abrasive Pads for Smoothing and Planarization of MEMS Structures

In: Proceedings of IEEE/SEMI Advanced Semiconductors Manufacturing Conference (ASMC 2005), Munich, Germany, 11–12 April, 2005. Pp. 5–10.
Reprinted with permission from the publisher.

Polishing of Bulk Micro-Machined Substrates by Fixed Abrasive Pads for Smoothing and Planarization of MEMS Structures

Martin Kulawski
VTT Microelectronics
Espoo, Finland
email martin.kulawski@vtt.fi

Hannu Luoto
VTT Microelectronics
Espoo, Finland
email Hannu.luoto@vtt.fi

Kimmo Henttinen
VTT Microelectronics
Espoo, Finland
email Kimmo.henttinen@vtt.fi

Tommi Suni
VTT Microelectronics
Espoo, Finland
email tommi.suni@vtt.fi

Frauke Weimar
3M Deutschland
Neuss, Germany
email fweimar@mmm.com

Jari Mäkinen
Okmetic Oy
Vantaa, Finland
email jari.makinen@okmetic.com

Abstract
In this work, an approach was made to use chemical mechanical polishing (CMP) by prototype fixed abrasive (FA) pads rather then conventional slurry based polishing for smoothing of bulk micro-machined and oxidized silicon wafers. A comparison is provided to conventional CMP, showing the minimization of edge rounding in case of FA use under the needed polishing step for sub-sequent wafer bonding. Simultaneously the achieved roughness provides a surface quality suitable for direct wafer bonding.

Keywords
CMP, MEMS, Fixed Abrasive, bonding, SOI

INTRODUCTION

Chemical Mechanical Polishing (CMP) has been proving to be the enabling process for state-of-the-art integrated circuit (IC) manufacturing up to the current 300mm technology [1]. While structures are getting ever-smaller [2], the process control has been able to follow the demands of each technology node [3]. Intentionally developed for oxide planarization [4], CMP is used nowadays widely for shallow trench isolation (STI) [5,6], enabling smallest features of today's IC circuitry, for example by use of high selectivity slurries (HSS-STI) [7]. In addition, CMP has entered the metal polishing area by damascene or dual damascene processing of multi metal layer metallization including copper and low-k dielectrics [8].

The benefits of CMP are however not yet widely used in micro electrical mechanical systems (MEMS) as obverse demands are requested [9]. While IC structures are getting smaller, in MEMS area often several micron big structures face the need of not only planarization [9] but also surface smoothing for subsequent bonding processes [10]. Besides oxide and metal, other materials including bulk micro-machined silicon have to be polished. The big structures of highly accurate deep patterning are however object to rounding, when applying the available conventional polishing processes [11]. Standard CMP intends to lead to a smooth surface, however with non-effective planarization of the big pattern surface, when not aiming for its total removal. Therefore, limits are set by the conventional technology for manufacturing of engineered substrates, such as buried cavity silicon on insulator (SOI) wafers or capped structured silicon wafers.

With fixed abrasive (FA) technology from 3M a new and alternative way of CMP has been introduced recently. Due to its different nature, which is to be explained later, not only the already proven benefits in the IC area of minimized dishing and erosion are expected. Also for the polishing of patterned bulk micro-machined silicon and oxide structures in the MEMS technology this new technique should yield in advantageous results.

EXPERIMENTAL

Avert to the conventional CMP polishing with micro-porous polishing pad and particle containing polishing agent, the so-called slurry, the abrading particles of the polishing process in fixed abrasive pads are residing inside of resin-type posts, which are fixed on the polishing pad (See Figure 1).

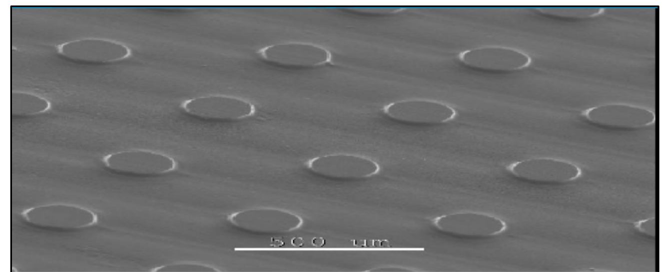


Figure 1 SEM picture of a fixed abrasive pad from 3M. The round shaped posts have a height of around 50 µm and contain the abrasive particles.

Below the micro-replicated layer, a rigid pad and a more resilient pad are stacked in order to adjust for the right mechanical properties of the process like in conventional

CMP. Instead of slurry, a lubrication liquid is provided under polishing, containing mainly water and chemistry to adjust for the appropriate pH-value. Figure 2 shows the schematic of the FA process.

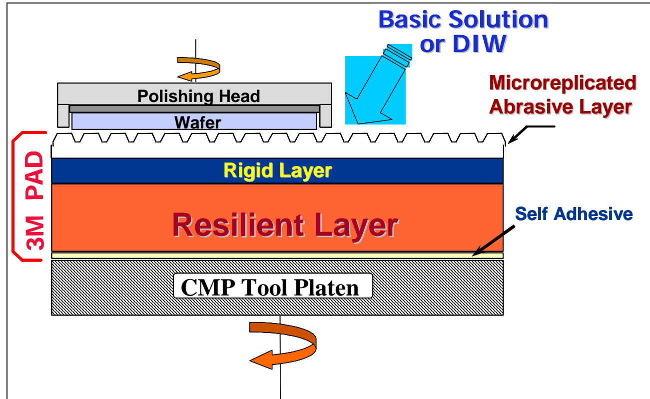


Figure 2. Schematic of the fixed abrasive polishing process.

It is evident, that the abrading particles of the FA process being fixed to the posts have less degree of freedom and thus face mainly the elevated areas of to be polished surface, while the deeper laying fields remain almost untouched. This makes the polishing process a two-body system (Figure 4), while conventional CMP occurs in a three-body system (Figure 3). Here the particles are free to move to all areas of the wafer. Even deeper laying areas are thus attacked by the process, however less than the elevated ones.

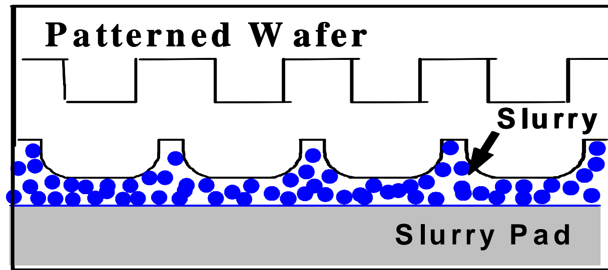


Figure 3 Conventional slurry CMP as 3-body system [12].

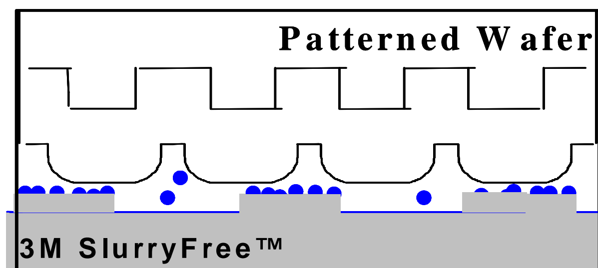


Figure 4 The fixed abrasive CMP from 3M as 2-body system [12].

The aimed planarization occurs therefore slower and under abrasion of material in all areas of the wafer. The process is less effective and sharp corners will round, as the pad can enclose them.

In practice, the fixed abrasive polishing should result in a more effective planarization of the structures and less attack in the lower areas. In addition, another point of interest is to be mentioned; freestanding structures should face less rounding when FA CMP is applied, as the microreplicated area of the fixed abrasive pad cannot surround the features as a conventional pad (See Figure 5).

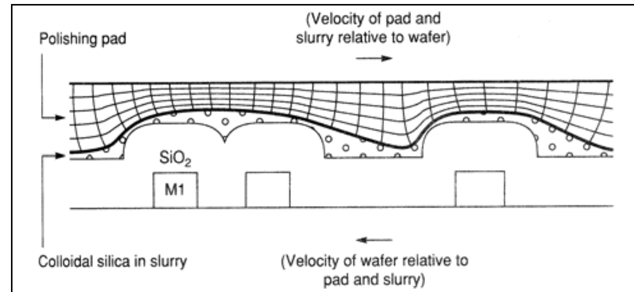


Figure 5. Schematic of conventional CMP. The pad surrounds the pattern features. Highest local pressure at the edges leads to especially high removal and rounds the structure under process [13].

METHODS

Experiments were performed on 4" and 6" standard silicon wafers with bulk micro-machined silicon and oxide pattern respectively. Plasma enhanced chemical vapor deposition oxide (PECVD) was used to deposit films of 1.5 µm to 3 µm thickness. Polishing was done on a Strasbaugh 6DS-SP two-platen polisher. Prototype fixed abrasive pads from 3M were used as well as conventional soft polishing pads with commercially available slurries. Processing was performed based on earlier gained experience and processing time was adjusted to minimum required removal in both cases the conventional and the FA CMP steps to maintain the pattern in original shape as best as possible. This in turn resulted in polishing times in between 60 and 120s and total average removal of in between 70 and 100 nm. Oxide film thickness was measured with Nanoscope 2150, for surface roughness measurements, an atomic force microscope (AFM) from Digital Instruments was used. Step heights and structure geometry was measured by DEKTAK V200.

RESULTS

The designed CMP processes in this investigation are made for smoothing either bulk micro-machined silicon or deposited oxide films in order to enable further processing like direct bonding, which requires a certain level of roughness. Same time the process should be able to remove global height differences of the features, while not changing the features geometry as such. In the first part of the experi-

ment, surface roughness was investigated after polishing while in the second part of the investigation emphasis was put on the pattern geometry after CMP.

Roughness

In Figure 6 the AFM scan of as-deposited PECVD-oxide can be seen. The rms value for the 3 µm thick oxide film is almost 5 nm and a grainy structure is visible. This surface as such is not suitable for direct wafer bonding.

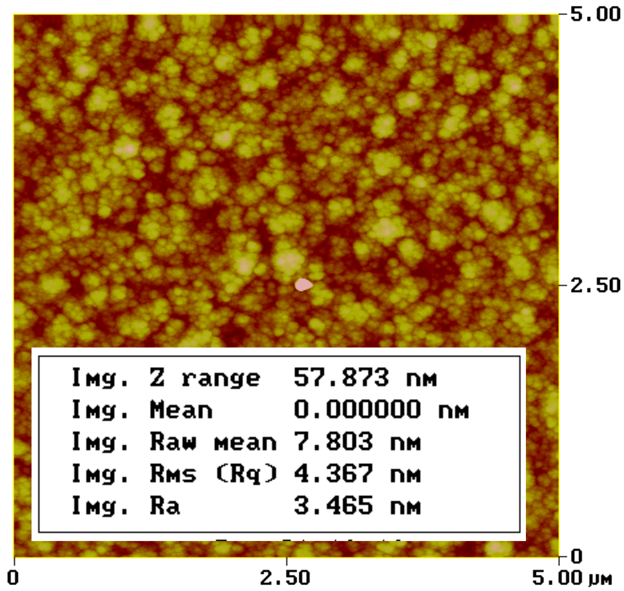


Figure 6. As-deposited PECVD-oxide of 3 µm thickness. The surface has a grainy structure and appears rough.

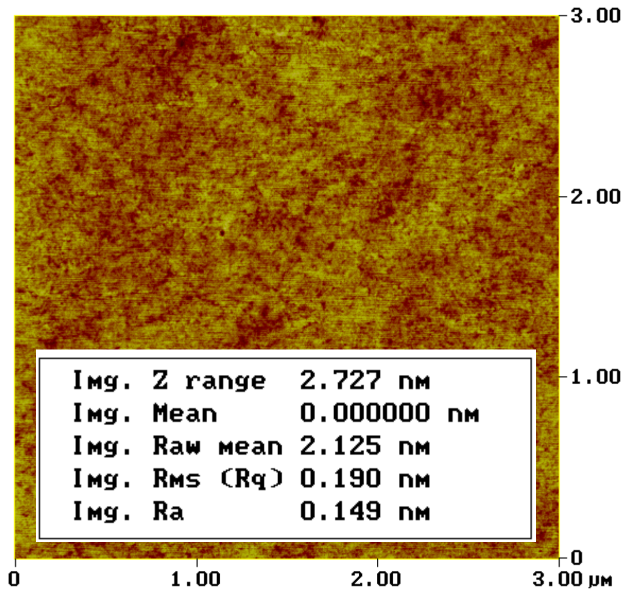


Figure 7. The PECVD-oxide after two minutes of polishing by conventional CMP. The roughness is reduced to Ångström level.

After polishing the film for 120s by conventional CMP, the roughness reduced down to below 2Å at a 3µm x 3µm scan (Figure 7). The total removal was found to be around 100 nm. It has been proven at VTT, that this level of roughness is already able to be bond directly to silicon with low temperature bonding process.

Applying fixed abrasive polishing to as-deposited oxide yield in almost similar result, as can be seen from Figure 8. After 80s polishing time the rms roughness reduces to comparable values of below 3Å at a 5µm x 5 µm scan. This is very close to the result of conventional CMP and thus surface quality is at direct bondable level. Also in this case the grainy structure of the deposition process is vanished. Instead, a slightly wiped surface appears which could result from the regular polishing pad features of the micro-replicated layer. However, it is of no bigger concern since the height differences are in the sub-nm area.

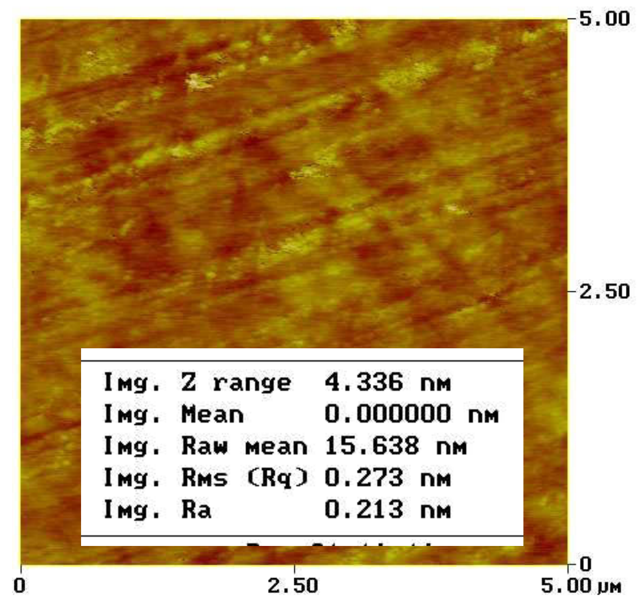


Figure 8. PECVD-oxide after fixed abrasive polishing. The surface is similar smooth as in the case of conventional CMP.

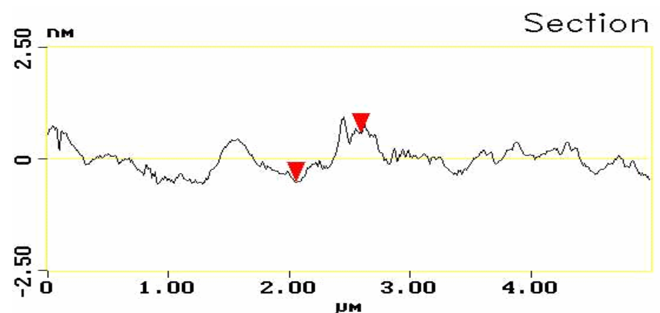


Figure 9. Cross-sectional view of the PECVD-oxide after fixed abrasive polishing. All remaining roughness or structure is at sub-nm area.

Taking a cross section of the AFM scan, one can observe the absolute height differences more distinct (Figure 9) The surface irregularity is within one nanometer and no abrupt height difference is measured, which could lead to voids or unsuccessful bonding.

Pattern Geometry

In terms of roughness, the difference between conventional and fixed abrasive CMP is seen to be small. The FA CMP reaches almost same performance as conventional polishing and can serve as enabling process for direct wafer bonding. The second important issue is to investigate the structure's geometry under the different polishing approaches. The conventional processing does round the features and reduces their width under a polishing time of 120s as can be seen from Figures 10 and 11. This was expected already.

While the removal on top of the structures is already almost 300 nm, Figure 10 shows in addition that dishing occurred in between the pillars at a level of almost 100nm. The total removal on top the structures however is much higher, than in the lower fields, indicating the beginning planarization.

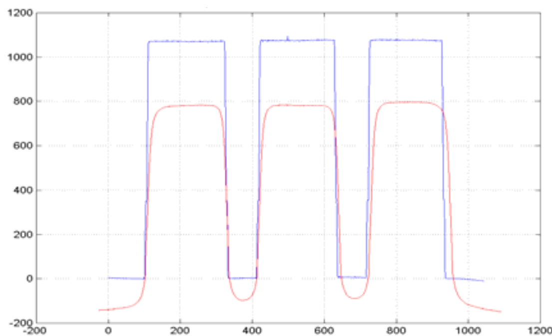


Figure 10 Oxide pattern before and after conventional CMP.

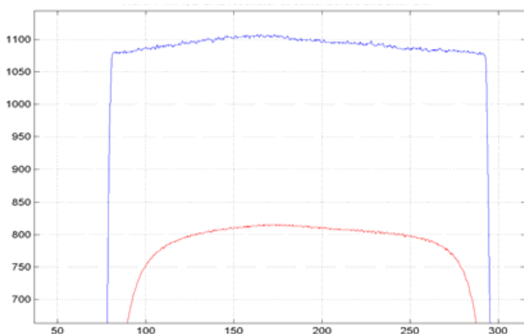


Figure 11 Detail of the oxide pattern before and after conventional CMP. Not only the corners are rounded, but also the feature width is noticeable reduced.

Another set of structures was used to compare directly the behavior of conventional and FA CMP. The total removal was set to be around 100nm in both cases for comparable results. Figures 12 and 13 show the structure before and after conventional CMP. Also here rounding is visible at the top of the features. However, due to further process development, the overall behavior is much better, than in the first approaches. By limiting the polishing time and reducing the downforce, the total removal was reduced to around 80nm. However, rounding could not be avoided totally.

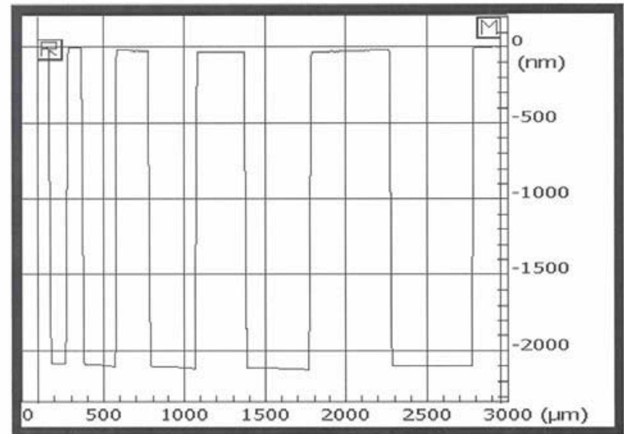


Figure 12 Oxide structure before CMP.

While the top is still facing the rounding, no major dishing occurs at the lower field of the pattern (Figure 13).

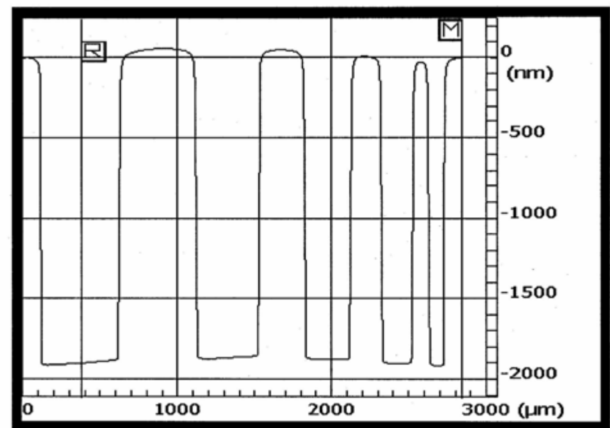


Figure 13 Oxide structure after further developed conventional CMP step. Rounding is still visible at the top but no dishing is seen at the bottom of the structure.

When comparing the details of the pattern when being polished by conventional CMP (Figure 14) and fixed abrasive CMP (Figure 15) the advantage of the new approach becomes evident.

In case of slurry-based CMP the rounding of the pattern top continues almost 20 μm deep into the structure and the slope becomes shallower. The overall pattern widens significantly. When using the FA pad, no rounding is seen in

the detailed picture and the slope remains steeper. Thus, the original shape of the structure is conserved under the advanced CMP process.

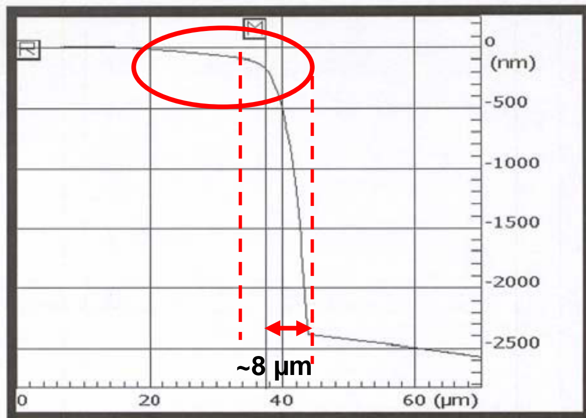


Figure 14 Oxide structure after further developed conventional CMP step at the corner. The rounding of the edge is continuing almost 20 μm into the structure.

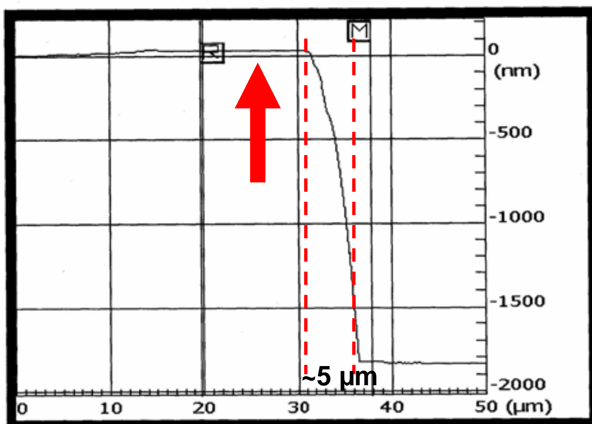


Figure 15 The FA CMP step leaves the corner of the structure untouched. Also the overall slope remains.

The pattern geometry conservation is evidently much better with FA CMP, than with conventional polishing approach. Final confidence in the new process can be gained, when applying the polished samples to the critical direct bonding process.

Bonding

Figure 16 shows an example of the successful direct bonding. At wafer level, no bigger voids were found and the process resulted in a well-connected wafer couple. This indicates that the reached surface roughness is well suiting the needs of direct wafer bonding. In the detailed analysis of the capped pattern by SEM it can be seen, that the bonding occurs well to the edge of the structure due to the conserved geometry under fixed abrasive polishing.

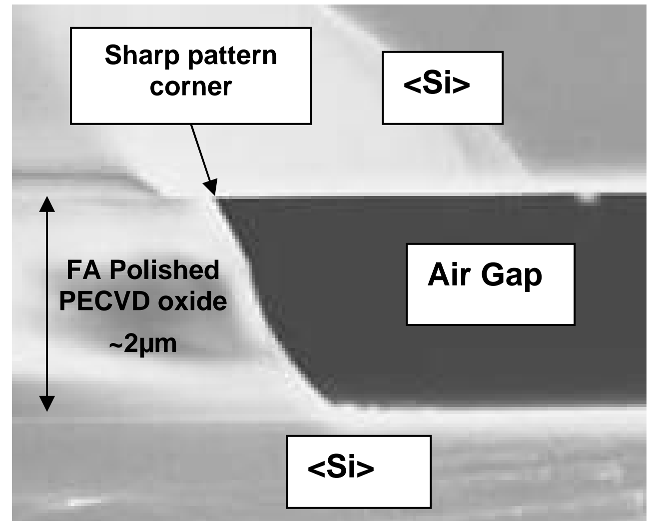


Figure 16 Bonded section of the fixed abrasive polished wafer.

CONCLUSION

The alternative technology of fixed abrasive CMP has been introduced to the area of MEMS manufacturing. The resulting surface roughness is at slurry-based level and enables the critical direct wafer bonding without any additional polishing step. Furthermore, the obstacles of conventional CMP in MEMS processing -the typical rounding of the pattern- can be overcome by FA polishing. The original shape of the pattern can be maintained and CMP can be used, even when structure dimensions are critical. This in turn will enable the capping of bulk micromachined structures by low temperature bonding processes and the use of bigger variety of materials like PECVD oxides. Further investigation shall stabilize the method and will offer new ways of manufacturing future advanced MEMS design.

ACKNOWLEDGMENTS

The authors would like to thank the Finnish research funding organization TEKES for supporting this study.

REFERENCES

[1] http://www.mitsubishi.or.jp/e/monitor/monitor_old97version/monitor9802/wafer.html, © Mitsubishi, 2004

[2] International Roadmap for Semiconductors, 2003

[3] J.G. Ryan et al., *The evolution of interconnection technology at IBM,* IBM J. Res. Dev. 39 (1995) 371

[4] AT&T Bell Laboratory, *CMP Mechanism identified at Bell Laboratory,* Solid State Technol. 37 (12) (1994) 26

[5] W.J. Patrick et al., *Application of chemical mechanical polishing to the fabrication of VLSI circuit interconnection,* J. Electrochem Soc. 138 (1991) 555

[6] S. Wolf et al., *Silicon Processing for VLSI Era II*, Process Integration 45, McGraw-Hill, New York, 1991

[7] S.-Y. Jeong et al., *A study of reproducibility of HSS STI-CMP process for ULSI applications,* Microelectron. Eng. 66 (2003) 480

[8] J. M. Neirynck et al., *Copper/Benzocyclobutene Interconnects for Sub-100 nm Integrated Circuit Technology: Elimination of High-Resistivity Metallic Liners and High-Dielectric Constant Polish Stops,* J. Electrochem Soc. 146 (1999) 1602

[9] G.Zwicker, *MEMS fabrication using CMP*, Presentation at the 10th CMP users Meeting, Munich 2003, www.isit.fhg.de

[10] M.Wiegand et al., *Wafer bonding of silicon wafers covered with various surface layers,* Sens. Act. 86 (2000) 91

[11] .J.M. Steigerwald et al., *Chemical Mechanical Planarization of Microelectronic Materials,* Wiley, New York, 1997, Ch. 5.5.2

[12] Kulawski et al. in *A novel CMP Process on Fixed Abrasive Pads for Manufacturing of highly planar thick film SOI Substrates* Mater. Res. Soc. Proc**. 767,** Warrendale, PA, 2003, pp. 133-139

[13] S.R. Wilson et al., Handbook of multilevel metallization for integrated circuits: materials technology and applications, Noyes Publications, Park Ridge, New Jersey, U.S.A., 1993, Ch.7.3

BIOGRAPHY

Martin Kulawski received his degree in electrical engineering at the Christian-Albrechts university of Kiel/Germany, specializing in solid-state electronics. He is currently working as Project Manager for the CMP Technology group at VTT Microelectronics in Espoo/Finland, which he established about 5 years ago. He simultaneously is aiming for his PhD in special CMP processing.

Hannu Luoto received his masters degree at the Helsinki University of Technology and works currently in the CMP Technology group of VTT Microelectronics.

Kimmo Henttinen received his masters degree at the Helsinki University of Technology. He works since many years in the microelectronics area. One of his major activities is the research on direct wafer bonding and low temperature wafer bonding at VTT Microelectronics.

Tommi Suni received his masters degree at the Helsinki University of Technology and works in the research field of wafer bonding at VTT Microelectronics.

Frauke Weimar is working in the Business Development of electronic applications for abrasives at 3M Deutschland.

Jari Mäkinen holds a Ph.D from the Helsinki University of Technology. He works as Senior Development Manager at the Finnish Wafer manufacturing Company Okmetic Oy

PAPER E

New Approach to Improve the Piezoelectric Quality of ZnO Resonator Devices by Chemomechanical Polishing

In: The Nano-Micro Interface: Bringing the Micro and Nano Worlds Together. Edited by H.-J. Fecht and M. Werner. Weinheim: Wiley-VCH. 2004. Pp. 181–193.
Reprinted with permission from the publisher.

WILEY-VCH K+V Fotosatz GmbH
Fecht/Werner Beerfelden
1. UK 22.7.2004
C. Grössl

New Approach to Improve the Piezoelectric Quality of ZnO Resonator Devices by Chemomechanical Polishing

J. Molarius, M. Kulawski, T. Pensala, and M. Ylilammi Q1

1 Introduction

The main application for FBARs is in telecommunications, especially in mobile phones. There is an ever-ongoing development of making smaller and smarter mobile phones than before. One phone should be able to work around the world on different frequencies, which of course increases the number of filters needed in a given phone. The number of RF filters in a mobile phone ranges from three to seven, which results in world market of about 2 billion pieces per year [1]. Because of the big size of the telecommunications market also the research activity around the world on the subject of FBAR has recently been high [1–6]. There are two ways to make phones smaller; shrinking the size of individual devices and increasing integration. FBAR in the current form achieves the first goal by its capability to produce very small, thin, and light filters. Comparison with the current market leaders of surface acoustic wave filters shows that FBAR filters have steeper filter skirts, smaller temperature coefficient of frequency (TCF), smaller chip size and better power handling capability [1, 6]. All these differences are significant, and furthermore the comparison is between mature SAW technology and the first generation of commercial FBAR devices: SMR type (solidly mounted resonator, see below) or bridge type. FBAR also gives good promise for future integration with RF circuits as materials, processing, and thermal budget can easily be designed to be compatible with CMOS processing, for example. The FBAR structure lends itself also to other applications (gas- and pressure-sensors have been suggested). The performance of these sensors using ZnO as piezolayer and SMR type structure with mirrors has been calculated and found to be excellent [7].

There are two basic FBAR structures; namely bridge (also called membrane) resonators or solidly mounted (also called mirror) resonators. The piezoelectric layer is vibrating between two electrodes and in bridge type device the substrate and the resonator are decoupled by an air gap. The air gap, in principle, provides almost ideal isolation, but in practice the lower electrode as well as the supporting structure cause losses. The bridge structure has been utilized to make filters using the resonators in a ladder configuration [5]. Bridges or membranes are

The Nano–Micro Interface: Bringing the Micro and Nano Wolds Together.
Edited by Hans-Jörg Fecht and Matthias Werner
Copyright © 2004 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim
ISBN: 3-527-30978-0

© WILEY-VCH

usually made by surface (or bulk) micromachining, which is often considered limiting the yield and productivity. Nevertheless there is a commercial producer for bridge-type FBAR passband filters for frequencies around 2 GHz [6].

Mirrors for isolating the resonator from the substrate was first proposed by Newell [8] in 1965 and then 30 years later developed to modern SMR structure by Lakin [9]. Here the resonator is isolated from the substrate by an acoustical mirror, build from alternating layers of high and low acoustical impedance materials, whose thicknesses are a quarter of the acoustic wavelength at the operation frequency. Depending of the choice of materials typically two to four layer pairs are needed. If molybdenum is used as the high impedance material and SiO_2 as the low impedance material three layer pairs are needed, but substituting Mo with W, two pairs are sufficient for adequate resonator substrate isolation. Mirrors can also be made of completely insulating materials such as AlN and SiO_2, which would give the benefit of easier processing as the mirror would not need any patterning. Metals in the mirror layers need patterning otherwise the parasitic capacitances associated with the conductive metal layers would cause problems in the device operation. Heavy metals have a high acoustic impedance and a high acoustic reflectivity, but a mirror made of AlN/SiO_2 requires four reflective pairs.

For making devices using bulk acoustic waves the quality of the piezolayer is paramountly important. In this chapter we are concentrating on ZnO, but same is true to other piezoelectric materials such as AlN or PZT {$Pb(ZrTi)O_3$}. Zinc oxide is chosen because of its high acoustic coupling coefficient (k_{mat}=0.282, k^2=7.95%) [5]. Lead zirconate titanate PZT promises the highest coupling coefficient at 0.28–0.5, after annealing, but very low Q-values (only 18 at 2.3 GHz) [3]. Aluminum nitride AlN on the other hand has a smaller temperature coefficient of frequency (TFE) (~25 ppm) than zinc oxide (~50 ppm). The smaller TFE of AlN in some FBAR filter applications can nullify the benefit of the higher acoustic coupling coefficient of ZnO. The longitudinal sound velocity in AlN is 10 400 m/s, which is over 60% higher than in ZnO, 6400 m/s. As the thickness of the piezolayer largely determines the frequency of the device, it is advantageous, at low frequencies, to have low sound velocity as the films will be thinner and therefore faster to deposit resulting in increased productivity. At high frequencies, the effective coupling becomes low with a piezomaterial with a low sound velocity because of the small thickness of the layer. This would indicate that ZnO is better at low frequencies and AlN at high frequencies.

The most important parameter determining the quality of piezoelectric layer (AlN or ZnO) is a strong preferred orientation of the film. For FBAR devices operating in the longitudinal wave mode this is (0001). As the crystal is thus growing c-axis perpendicular to the substrate the hexagonal basal plane is interacting with the seed layer. ZnO films can and have been deposited by several different ways, such as CVD (chemical vapor deposition), laser ablation, and PVD methods (physical vapor deposition). In the PVD methods magnetron sputtering, either by rf-sputtering from ZnO-target or by dc or pulsed dc in reactive mode from zinc target in oxygen containing atmosphere, have been extensively used as the temperatures remain low during deposition and there is good compatibility with standard semiconductor device

processing. Beside the sputtering parameters themselves, other issues affecting the piezoelectric film quality are the seed layer and the sputtering environment (affecting contamination). If the seed layer is used as the bottom electrode of the device, it has to be highly conducting to keep the electrical losses to a minimum. Therefore it is advantageous to separate these functions to a highly conducting bottom electrode and to a separate seed layer, which can be optimized to promote piezolayer growth and acoustical properties of the FBAR stack. Device quality ZnO can be grown on several metals, at VTT this has been realized on gold and molybdenum [4, 5, 10, 11]. It has been shown that good quality AlN, which has the same wurtzite-type crystal structure as ZnO, can be grown on different seed materials [12]. Löbl [13] and S.-H. Lee [14] for AlN and J. B. Lee [15] for ZnO identified the surface roughness of the seed layer as the decisive factor on piezoelectric film quality; the smoother the seed layer, the better the piezoelectric film quality. The film quality was measured by X-ray rocking curve of ZnO film and the FWHM (full width half maximum) of the (0002) peak was shown to correlate with the effective acoustic coupling coefficient, k_{eff} [3]. K_{eff} on the other hand determines the bandwidth and insertion loss of a filter [16]. Quality factors, Q, are determined at both series and parallel resonance. They are calculated according to the IEEE standard [17]. The reason for the correlation between surface roughness and film quality is quite simple. Since the deposition takes place at low temperature and with low particle energy, adatoms on the surface have low mobility and they do not reach the energetically favored positions for the growth in the preferred orientation. On a smooth substrate the movement of the adatoms is easier and this results in improved piezolayer quality. Control of the surface roughness of a given metal can only be achieved to a certain degree with adjustment of the sputtering parameters, as other film properties, especially stresses in the film, will also be strongly affected. Therefore a better approach is needed.

CMP is usually used to planarize device structures, as seen in the diagram in Fig. 1. The wafer is held on a carrier and pressed with a defined force against a micro-porous polyurethane polishing cloth, which is glued on the rigid polishing

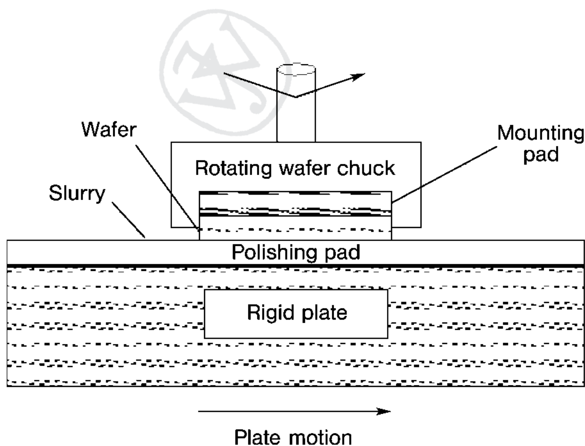


Fig. 1 Diagram of chemomechanical polishing (CMP).

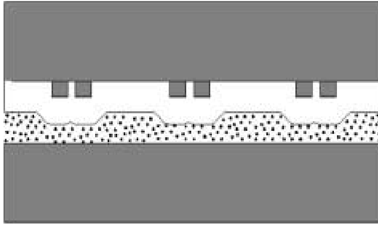


Fig. 2 Principle of CMP removal.

platen of the tool. While the platen and the chuck are rotating a suspension with Q3 adjusted pH-value of DIW and abrasive particles (slurry) is dispensed on the platen. The abrasive particles are made from silica or ceria with diameters in the 50 nm range. During polishing the particles are accelerated by the micro-pattern of the polishing pad and impinge on the surface of the wafer, thus weakening the strength of the atomic network. The pH-adjusted liquid can penetrate into the weakened network and dissolve atomic clusters from it. Owing to the height variation of the patterned surface a different local pressure is applied to elevated and lower areas of the wafer leading to increased removal on the higher regions. This leads to a planarization of the pattern on a large scale. In Fig. 2 the principle of the removal is presented in detail. In this chapter the emphasis is on surface smoothing by CMP, which can be achieved with a modified CMP planarization process.

Any kind of CMP, however, will lead to a heavy contamination of the polished substrates with particles left on the surface. Since these particles have strong adhesion a special cleaning is an important issue after polishing. Beside soft etching methods and standard cleaning with megasonic agitation we are currently qualifying a special post-CMP cleaner, which scrubs the surface with a soft PVA-brush (polyvinyl alcohol) and remove particles also by mechanical means. Beside the particles a slurry often contains metallic contamination. Thus by including chemistry to the post-CMP cleaning process care has to be taken for lowering the metal contamination down to the stringent levels for CMOS compatible production. It is the aim of this chapter to develop the CMP smoothing and apply it to FBAR to achieve high quality ZnO for resonators and filters.

2 Experimental

We have used 100 mm (100)-oriented silicon wafers as substrates. Wafers with 1–10 Ω cm resistivity were used for structural characterization of the deposited zinc oxide films. High resistivity wafers (>500 Ω cm) were chosen as substrates for processing resonators and filters to eliminate the parasitic effects associated with the semiconducting silicon [4]. Films were sputtered in a cluster tool (Von Ardenne CS 730 S) from 200 mm diameter round targets. In this system metal films are deposited in a multitarget chamber with dc-magnetrons, but to minimize

cross-contamination, ZnO is sputtered in a dedicated single target chamber. Reactive dc-magnetron sputtering from zinc target (purity of 99.995%) in argon/oxygen atmosphere is utilized in all experiments. Both gases have purity of 99.9999%. The flow rates of the gases were rationed with massflow controllers and the oxygen content was always set to 41 vol.-%. The loadlocked cluster type sputtering system was pumped with oil free turbodrag and diaphragm pumps to below 5×10^{-5} Pa before sample processing.

Resonators were SMR-type fabricated on quarter wavelength acoustical mirrors, consisting of alternating layers of high (W) and low (SiO_2) acoustic impedance materials. We used a simplified resonator process, where only the top electrode is patterned leaving all other layers (mirror, bottom electrode and ZnO) to cover the whole wafer. Contact to the bottom electrode is done capacitively. The film thicknesses for the resonator stack were calculated by an in-house developed one-dimensional modeling program. Tungsten has the highest known acoustic impedance and the impedance ratio $Z_{high}:Z_{low}$ for W–SiO_2 pair is 7.7 : 1. This ensures good acoustic isolation with only two layer pairs. In case of Mo-SiO_2 the ratio is 4.8 : 1 and consequently one needs an extra pair. Metals were sputter deposited by dc-magnetron and PECVD (plasma enhanced chemical vapor deposition) was used for SiO_2. Our resonator and filter fabrication is explained in more detail elsewhere [4].

Smoothing was done on a Strasbaugh 6 DS-SP planarizer. Standard processing consumables such as pads and slurries were varied in the experiments to achieve the best surface smoothing. Polishing times were varied in the range 30–90 s. Cleaning was done in a batch cleaning in a quartz sink using megasonic agitation for 10 min with pure DIW at 55 °C and subsequent spin-drying for particle removal. Additionally in some cases a SC-1 bath was used for enhanced particle removal.

The film morphology was studied using a digital scanning electron microscope (SEM, Leo 1560). Surface roughness and topology were measured by atomic force microscopy (AFM, Digital Instruments Dimension 3100). FilmTek 4000 spectrophotometry tool was used for optical characterization of ZnO. For electrical characterization of the completed devices Agilent Technologies 8753 network analyzer was utilized.

3
Results and Discussion

Schematic cross sections of the film stacks for both bridge and solidly mounted resonator are shown in Fig. 3. In surface micromachining the air gap is formed by dissolving a sacrificial layer from underneath the bridge, such as copper below silicon nitride bridge [5]. SMR schematic in Fig. 3 has the designed layer thicknesses, whereas the lowest high-Z layer in the actual scanning electron microscopy (SEM) cross section micrograph of a FBAR is too thick. Fortunately it does not affect the mirror performance substantially. This can be deciphered from Fig. 4, which shows the relative calculated displacement amplitude in a resonator

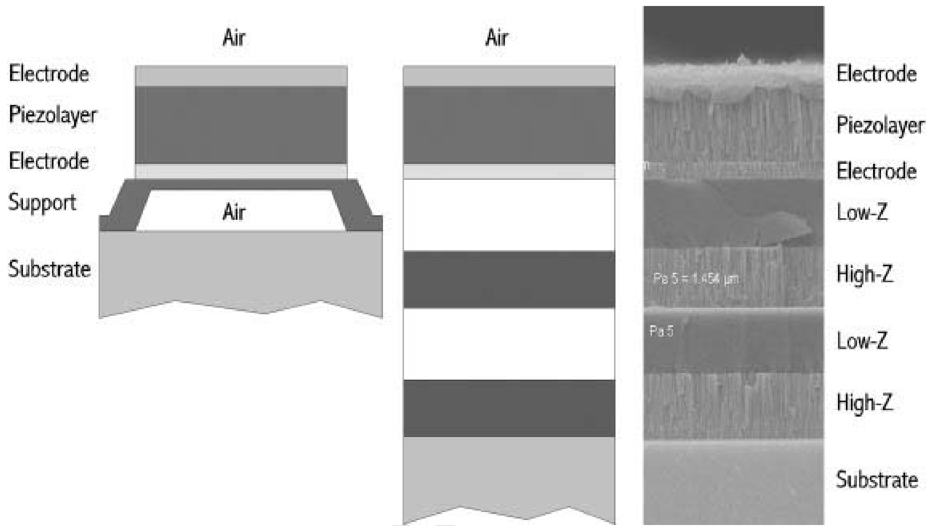


Fig. 3 Bridge and mirror resonator film stacks with cross section SEM of the mirror FBAR.

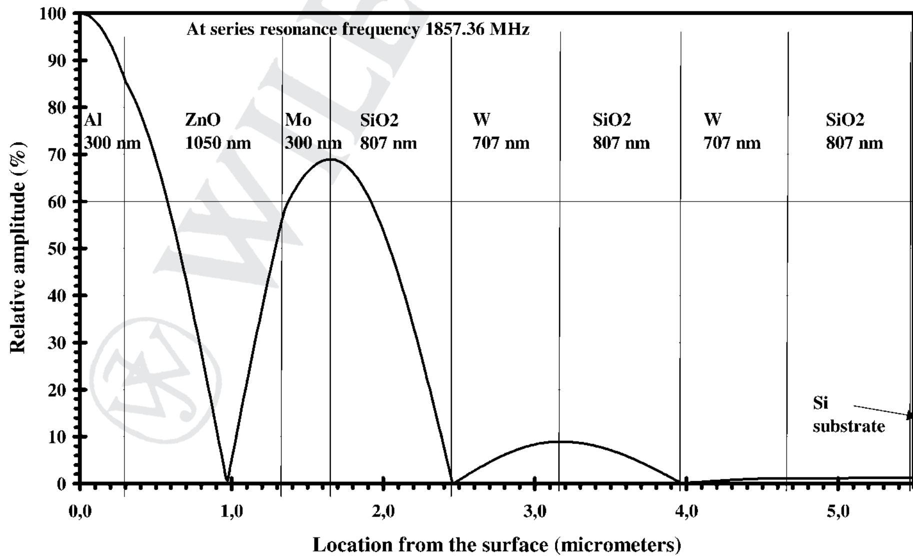


Fig. 4 Relative displacement in a resonator stack at 1857 MHz. Free surface is on the left.

stack with silicon dioxide/tungsten mirror. The relative displacement at the substrate is <2% of the maximum at the series resonance frequency of 1857 MHz; therefore it is not necessary to increase the number of mirror layers in this stack. The highly columnar structure of the metals in the mirror and bottom electrode

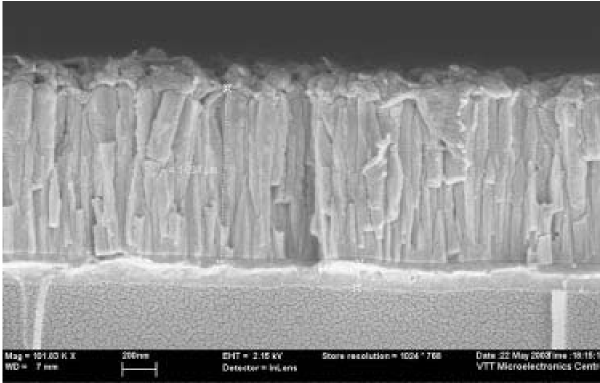


Fig. 5 Cross section SEM micrograph with non-CMP ZnO piezoelectric film on resonator.

is clearly depicted in Fig. 3, as well as the amorphous nature of silicon dioxide. Top electrode is sputtered aluminum and it has been deformed during sample cleaving. The ZnO piezolayer is also highly columnar as desired for strongly preferred orientation. But as can be seen in Fig. 5 the ZnO film on a wafer, which is not CMP, smoothed is porous and the ZnO surface appears to be very rough.

ZnO is transparent, therefore we have measured the samples optically with Filmtek 4000 from ultraviolet to infrared wavelengths (450–1650 nm) [18]. A typical index of refraction (n) and extinction coefficient (k) as function of the wavelength are shown in Fig. 6. Index of refraction at 633 nm varies on different films from 1.910 to 1.921, which is quite close to the bulk value of 1.997 [19]. In optical respect our ZnO films seem to be of fairly good quality even without CMP smoothing.

It is not feasible to smooth the top electrode metal layer by CMP, due to contamination issues. Gold, one of our electrode materials, is the most feared yield killer in microelectronics. Therefore we decided to smooth the top mirror layer SiO_2 as this is compatible with other work done on our CMP tool. A CMP smoothing process for the silicon dioxide was developed and the topological properties of the films were measured with AFM. As one can see in AFM nanographs in Fig. 7, the surface appearance of PECVD deposited SiO_2 film changes completely in CMP. During the removal of 70–80 nm of oxide by CMP the rms roughness is dramatically reduced from 4–5 nm to <0.3 nm. After the first trials with actual FBAR samples a smooth surface was achieved, but lots of particles were detected on the surface even after post-CMP cleaning. This was resolved by adding a SC-1 cleaning step at 55 °C in the post-CMP cleaning procedure. In the actual FBAR samples we found holes in the oxide. In the overall view the large number of holes can be seen in the optical micrograph (Fig. 8 a), a close up reveals that the holes go through the oxide (Fig. 8 b). This was further confirmed with stylus measurements. It seems that holes originate from defects on the thick tungsten high Z film. These defects in turn cause flaws on the growing SiO_2 and the SC-1 cleaning solution (ammonium and hydrogen peroxide) attacks these resulting in holes.

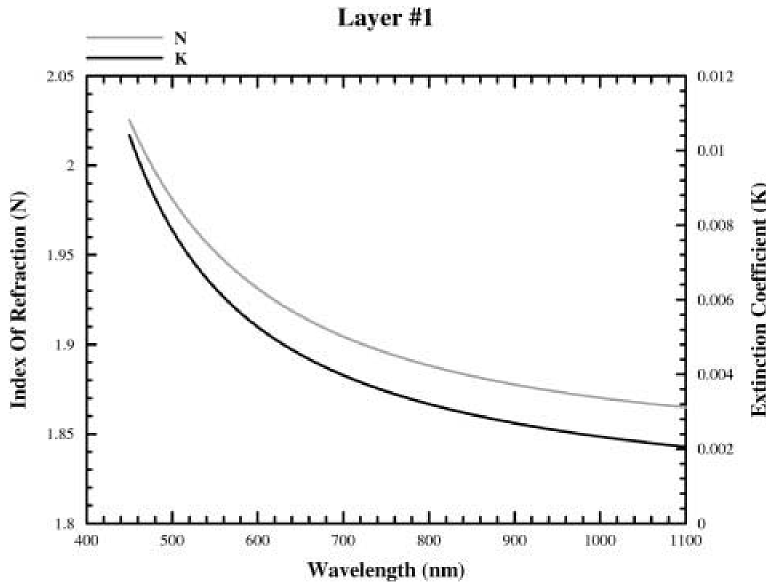


Fig. 6 Filmtek spectrophotometry results of the index of refraction and extinction coefficient as function of wavelength.

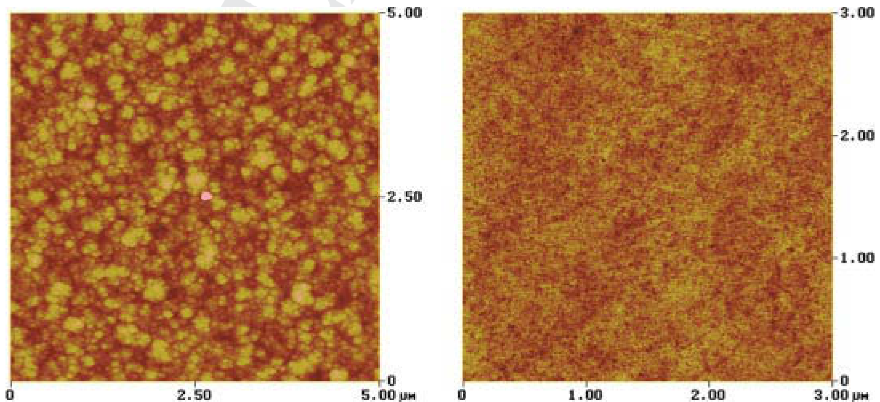


Fig. 7 AFM nanographs of SiO_2: (a) before and (b) after CMP smoothing.

Another issue with CMP smoothing is how our resonator stacks survive through the CMP. This is illustrated in Fig. 9, where a stylus trace (in fact a cross section, compare Fig. 3) of the resonator stack is shown before and after the CMP smoothing. The corners are rounded during CMP, but a large center area of the mirror stack remains flat and uniform. It does seem to be possible to reduce the rounded area further by CMP process development. When including CMP into the FBAR process flow, one has to take into account not only the removal of the

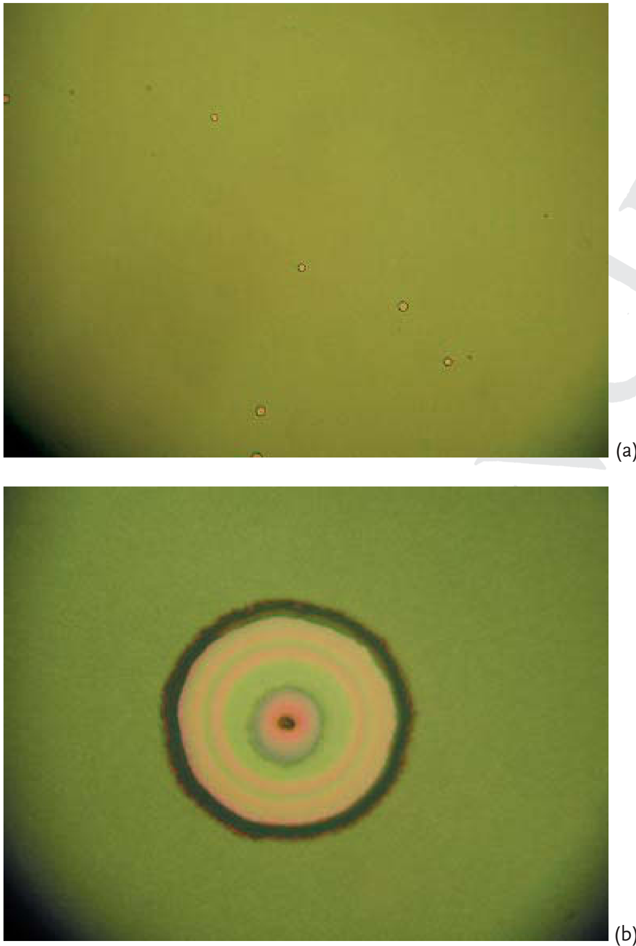


Fig. 8 Optical micrograph of SiO_2 surface after post CMP cleaning: (a) overall view, (b) close up of a hole.

oxide by CMP, but also the rounding of the corners by allocating some extra area on the resonator mirrors. Although we loose some chip "real estate" future integration of CMP smoothing into the filter processing seems feasible.

In Fig. 10 AFM nanographs of zinc oxide surface in the old process without CMP smoothing of the silicon oxide and with CMP are shown. Surface roughness has been reduced from 23 to 4.4 nm. The ZnO film (non-CMP) in cross section SEM micrograph in Fig. 5 is from the same sample as in Fig. 10a. The cross section microstructure and surface roughness are also closely related in case of the CMP smoothed ZnO film, where smooth surface also results in dense and featureless SEM cross section (not shown here).

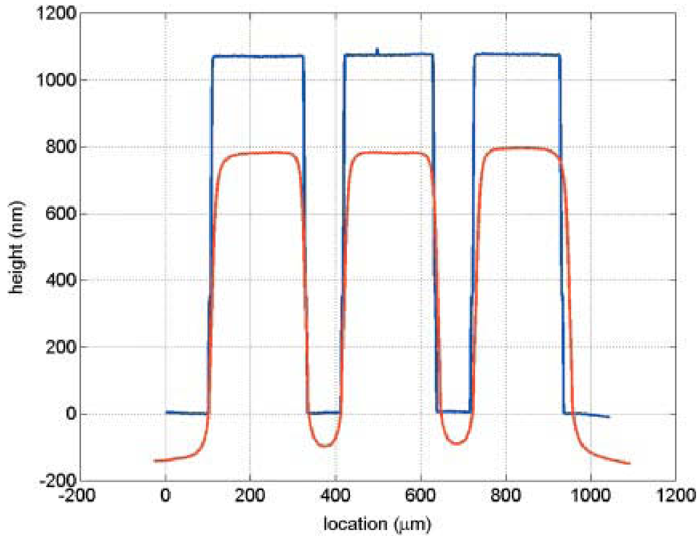


Fig. 9 Dektak stylus trace of the FBAR stack: (a) before and (b) after CMP smoothing.

WILEY

Smoothing seems to result in better ZnO smoothness as expected and has been reported before [16]. In smoothest ZnO the rms roughness we have achieved with CMP is 4.4 nm, which compares favorably with the best achieved smoothness of non-CMP ZnO, where rms roughness is 13 nm. In a recent work [20] very smooth, rms roughness 1.06 nm ZnO film is reported on an actual SMR FBAR with gold electrodes. ZnO roughness was measured by AFM on the as-deposited samples and it is plotted as function of the deposition run in Fig. 11. Data show that the smoothest ZnO is achieved on those wafers where the top SiO_2 has been smoothed by CMP and the worst roughness was on non-CMP wafers. Another trend is that the ZnO on the non-CMP resonators is getting better with time (more runs). Owing to the instabilities in the ZnO sputter deposition and small number of samples, evidence however is not unambiguous.

The quality of the piezolayer (and the whole resonator) is measured by the effective coupling coefficient and the Q-values at series and parallel resonances. In Fig. 12 the coupling coefficient as function of surface roughness is presented. Two lowest points can be explained by the dc-bias on the substrate during sputtering, which is obviously detrimental to the piezolayer quality. Unfortunately only one CMP-smoothed; wafer survived through the processing (the smoothest one). At the parallel resonance (Qp) Q-values range from 70 to 307, and at the series resonance (Qs) from 69 to 446 without showing any correlation to the ZnO surface roughness. the CMP-smoothed resonator had Qp of 108 and Qs of 339. Due to our simplified resonator process this structure is not optimal for Q-value determination, but nevertheless our Q-values are comparable to the one (201) reported recently [20].

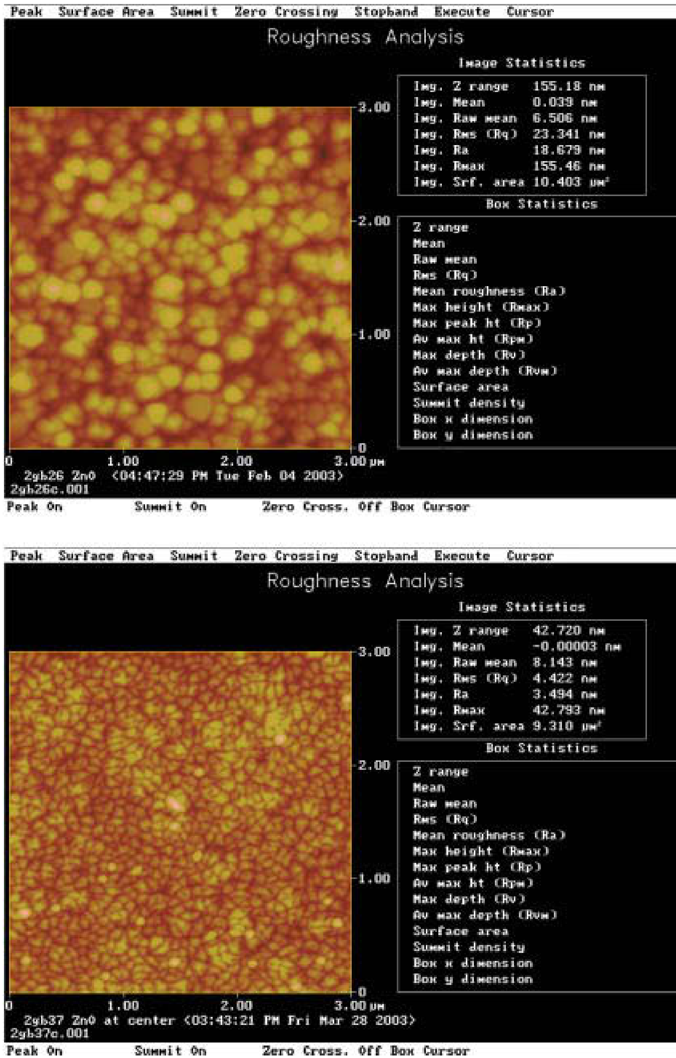


Fig. 10 AFM nanographs of ZnO surface after sputter deposition: (a) non-CMP (b) CMP smoothing applied to SiO_2.

One has to keep in mind that the wavelength of the acoustical waves in ZnO in these resonators is 3 µm, but the scale of the surface roughness is in (tens of) nanometers. Therefore strong physical coupling between the acoustical waves and the surface roughness was not expected. One can speculate that a smoother surface would result in smoother and denser ZnO, because of the effect on film growth during sputtering. This has not been completely verified, as the evidence is inconclusive at this stage.

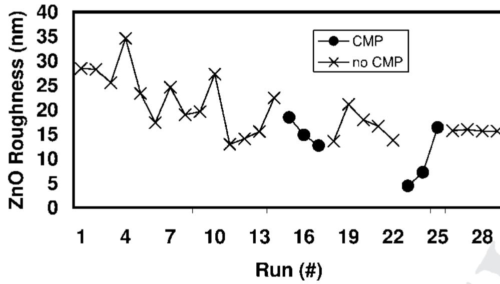


Fig. 11 ZnO surface roughness as measured by AFM after sputtering runs.

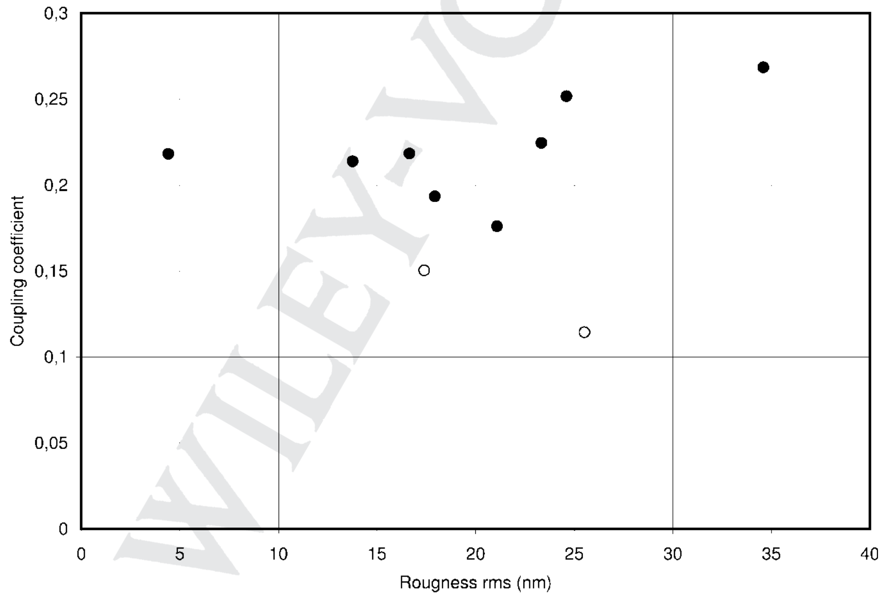


Fig. 12 Acoustic coupling coefficient correlation to ZnO surface roughness. Open circles denote DC-bias on the substrate during sputtering.

4 Conclusions

CMP smoothing was introduced to FBAR (thin film bulk acoustic wave resonator) technology and it was used in fabrication of SMR-type resonators. The ZnO film morphology and microstructure were studied with AFM and SEM, respectively. Optical properties were sampled with spectrophotometry. It was shown that the smoothing of the top mirror SiO_2 improves the surface roughness of the zinc oxide. The roughness achieved with CMP smoothing was 4.4 nm (rms), which compares favorably with 13 nm without CMP. The quality of the ZnO piezolayer was evaluated by measuring the acoustic coupling coefficient and Q-values at parallel

and series resonance. ZnO was piezoelectrically good and the CMP smoothing shows good prospects for future integration in FBAR process flow.

Acknowledgments

Special thanks are due to Ms. Meeri Partanen for sample processing and Kimmo Solehmainen for Filmtek measurements.

References

1. Aigner R., Ellä J., Timme H.-J., Elbrecht L., Nessler W., Marksteiner S., in: *Proc. IEEE International Electron Devices Meeting (IEDM)*, San Francisco, 9–11 December **2002**.
2. Lakin K., *IEEE Ultrasonics Symp.* **2002**.
3. Löbl H.P., Klee M., Metzmacher C., Brand W., Milsom R., Dekker R., Lok P., *Mater. Chem. Phys.* **2003**, *79*, 143–146 and *Mater. Sci. Eng. B* **2002**, 1–4.
4. Kaitila J., Ylilammi M., Molarius J., Ellä J., Makkonen T., *IEEE Ultrasonics Symp.* **2001**, 223.
5. Ylilammi M., Ellä J., Partanen M., Kaitila J., *IEEE Trans. Ultrasonics, Ferroelectrics, Frequency Control* **2002**, *49*, 535.
6. Larson III J.D., Ruby R.C., Bradley P.D., Wen J., Kok S.-L., Chien A., *IEEE Ultrasonics Symp.* **2000**, 869.
7. Mansfeld G.D., Kotelyansky I.M., *IEEE Ultrasonics Symp.* **2002**.
8. Newell W.E., *Proc. IEEE* **1965**, *53*, 575–581.
9. Lakin K., Kline G., and McGarron K., *IEEE Trans. Microwave Theory and Techniques* **1995**, *43*, 2933.
10. Molarius J., Kaitila J., Pensala T., Ylilammi M., *J. Mater. Sci.: Mater. Electron.* **2003**, in press. Q4
11. Molarius J., Ylilammi M., US Patent 6,521,100, **2003**.
12. Iriarte G.F., Bjurström J., Westlinder J., Engelmark F., Katardjiev I.V., *IEEE Ultrasonics Symp.* **2002**.
13. Löbl H.P., Klee M., Milsom R., Dekker R., Metzmacher C., Brand W., Lok P., *J. Eur. Ceram. Soc.* **2001**, *21*, 2633–2640.
14. Lee S.-H., Lee J.K., Yoon K.H., *J. Vac. Sci. Technol. A* **2003**, *21*, 1.
15. Lee J.B., Kwak S.H., Kim H.J., *Thin Solid Films* **2003**, *423*, 262–266.
16. Lakin K., Kline G., and McGarron K., *IEEE Ultrasonics Symp.* **1992**, 471–476.
17. *IEEE Standard on Piezoelectricity*, ANSI/IEEE Standard 176, **1987**.
18. US Patent 5 999 267, **1999**.
19. Jellison Jr. G.E., Boatner L.A., *Phys. Rev. B* **1998**, *58*, 3586–3589.
20. Lee J.B., Kim H.J., Soo Gil Kim, Hwang C.S., Hong S.-H., Shin Y.H., Lee N.H., *Thin Solid Films* **2003**, in press. Q5

© WILEY-VCH

PAPER F

Low-temperature Bonding of Thick-film Polysilicon for MEMS

In: Journal of Microsystems Technology 2006.
Vol. 12, No. 5, pp. 401–405.
Reprinted with kind permission of Springer Science and Business Media.

Low-temperature bonding of thick-film polysilicon for MEMS

H. LUOTO, T. SUNI, M. KULAWSKI, K. HENTTINEN, H. KATTELUS

VTT Information Technology, Tietotie 3, 02150 Espoo, Finland

hannu.luoto@vtt.fi

Fax. +358-9-4567012

Tel. +358-9-4567279

Abstract

Polysilicon thick films have been found to be an irreplaceable option in various sensors and other microelectromechanical system (MEMS)-designs. Polysilicon is also a prospective option for replacing single-crystal silicon in customized silicon-on-insulator-substrates. Due to the nature of polysilicon, bonding for MEMS-purposes has so far concentrated on anodic bonding, which has drawbacks for instance in terms of process duration and thermal load. The objective of this work is to develop low-temperature direct bonding for various polysilicon films. Polysilicon films were grown at varying temperatures and pressures with and without boron doping. The films were polished by chemical-mechanical polishing and cleaned. Surface qualities were studied by atomic-force-microscope before bonding. Wafers were then activated with argon plasma and bonded to oxidized silicon, quartz and glass. Bonding quality was evaluated with scanning-acoustic-microscope, the crack-opening-method and HF-etching. Scanning-electron-microscopy was used to investigate film and interface quality. This development has led to a new kind of polishing process, where several microns of polysilicon are removed still leaving surface direct bondable. This is accomplished by a dedicated and effectively planarizing polishing process. Spontaneous bonding took place and good bonding quality was achieved after annealing at 200°C.

Introduction

Low-temperature (LT-) direct wafer bonding is known as a potential technology for fabricating silicon-on-insulator (SOI) structures for advanced microsystems and optical devices. It has not, however, been extensively used for wafer-scale-packaging so far, despite of its inherent advantages. As a capping wafer for a silicon-based wafer the thermal match is, of course, ideal over a wide temperature range. The seal is hermetic and outgassing minimal. Alkaline ions, being essential constituents in anodically bondable glasses, are totally avoided [1]. The high applied voltage during bonding which may cause deleterious electrostatic force for devices is not used. The bonding temperature as low as 200°C in direct bonding allows encapsulation of temperature-sensitive devices or use of capping wafers with imperfect thermal match. Furthermore, the process time is shorter than in anodic bonding. The need to encapsulate in high vacuum is common in RF-microelectromechanical systems (RF-MEMS), where the quality factor for oscillating actuators or speed of mechanical switches are improved at reduced pressure. The high vacuum eliminates fluidic friction decreasing the power consumption of the device and at the same time increases the sensitivity to external stimulus. These facts have promoted the present investigation of LT-direct wafer bonding technology.

One of the most important drawbacks in direct bonding is that it requires very good surface finish and total absence of particles in the bonded interface. That is why it is very important to study process cycles resulting in perfect surface polish for bonding. Polycrystalline silicon is a commonly used material in micromachining. Its surface is typically rough due to the microcrystalline structure posing major challenges for the polishing cycle.

We have investigated chemical-mechanical polishing (CMP) processes to efficiently remove the surface roughness that is met after thick film polysilicon growth. Grain boundaries in the polycrystalline structure were found to exhibit preferential etching when processing was

performed with conventional chemicals or processes. This phenomenon was not acceptable during polishing in order to maintain a sufficient level of surface smoothness required by LT-direct bonding [2]. Additionally, the functioning of polysilicon plasma-activation had to be confirmed. The bonding was performed in air or in vacuum. The films were deposited by both with low-pressure chemical-vapour-deposition (LPCVD) and atmospheric-pressure chemical-vapour-deposition (APCVD) growth process. Surface quality was investigated with atomic-force-microscope (AFM), the bonded interface strength was measured with the crack-opening-method and HF-etching test and voids at the bonded interface were studied with scanning-acoustic-microscopy (SAM) [2, 3].

Experimental

In the experiments, <100> oriented p-type Czochralski grown silicon wafers with a diameter of 100 mm were used. The resistivity of the wafers was 1-50 ohmcm. A thermal wet oxide layer with a thickness of 500 nm was grown at 1050°C on part of the wafers. Polysilicon films were grown with two fundamentally different processes, LPCVD and APCVD. LPCVD-films were grown at 620°C and 680°C followed by an annealing step performed at 1050°C for 1h. The doping level of films was varied from intrinsic to highly boron-doped. APCVD-films were grown at 1100°C with ~$6,5*10^{17}$ of in-situ boron doping. Prior to APCVD-process, seed layer of 100nm was grown on all the wafers in 600°C with the LPCVD-process. APCVD-grown films were also annealed subsequently at 1050°C for 15min.

After the film depositions wafers went through a CMP-process carried out with Strasbaugh 6DS-SP two-table polishing system. Polishing was performed as a two-step process where the first step was dedicated for removing most of the high surface roughness and bigger surface defects, and the second one for finishing the surface. Surface quality after the polishing process was then confirmed with AFM in tapping mode (Digital Instruments D3100). After

the polishing and an RCA-1 (NH_3:H_2O_2:H_2O, 70°C) cleaning, the wafers were activated in a reactive ion etcher (Electrotech RIE) using argon plasma. During the plasma exposure the chamber pressure was 150 mTorr with the gas flow set at 30 sccm. The RF power was 150 W. With these parameters the bias voltage of the substrate electrode was 200 V. The duration of the plasma exposure in this study was 30s. After the plasma treatment the wafers were cleaned in deionised water. After cleaning, the wafers were dried in a spin dryer. The wafers were subsequently bonded in a commercially available wafer bonder (Electronic Visions EV801). The bonding was carried out either in air or in vacuum at room temperature. The bonded wafer pairs were annealed for 2 hours at 200°C. After this first annealing step some of the wafers were cut into rectangular slices using a dicing saw. The diced samples were annealed for 2h at 300-400°C. The surface energy of the diced samples was measured in air using the crack-opening-method. The bonded wafer pairs were inspected for interfacial voids using IR transmission imaging and scanning acoustic microscopy (Sonix UHR2000). The surface roughness of the plasma-activated surface was measured with an atomic-force microscope using silicon tips in the tapping mode. As a parallel test for the crack-opening-method an HF-etching test was executed, where samples were first dipped in a 50% HF solution for 10 minutes and subsequently cleaned in deionised water and dried. The etched distance was measured from cross-section samples by using LEO 1560 scanning-electron microscope (SEM) manufactured by Oxford Instruments. Concomitantly, information of the general interface quality was obtained.

Results and Discussion

Both the LPCVD- and APCVD-films showed maximum film roughness up to 10-15% of the total film thickness. As-deposited film surface topography contained spikes, where sharp tips emerged from surrounding area. This could be seen with both LPCVD- and APCVD-films.

This kind of formation is understandable particularly in case of APCVD-polysilicon due to its strongly columnar structure (see Figure 1). The growth temperatures of the LPCVD-films were kept relatively high (620°C and 680°C) to enable high growth rates. Hence, grains grow preferentially in coarse columnar structure [4]. After the deposition the films were in a relatively high compressive stress which was needed to be relaxed or converted into tensile in order to maintain film stress controllability. The LPCVD-films were annealed after deposition to enlarge crystal size, to improve film quality and to relief stress. Annealing as well as boron-doping were confirmed to slow down the removal rate in CMP. The required removal for smoothening the surface was, however, found to be affected by neither boron-doping nor annealing. This implies that the surface roughness is not affected by doping or annealing. Furthermore, we observed that the retardation effect was significant in very heavily doped LPCVD-poly where boron concentration exceeded $5*10^{18}cm^{-3}$ and was close to its solubility limit at room temperature. We assume that a polishing process is prolonged due to slowed down silicon hydrolytic reaction, where boron in boranes (B-Si) is preferably attacked by hydroxide ions, and the activity of Si-Si hydrolysis is reduced as it has been suggested by *Yang et al.* in the case of single crystal silicon [5]. High decline of the removal rate as a function of annealing temperature and time could be explained by a grain structure consisting of larger grains, in which case the amount of grain boundaries prone to chemical attack by the polishing slurry is reduced. Alternatively, mechanical shear force needed to propagate a crack through a grain could be higher.

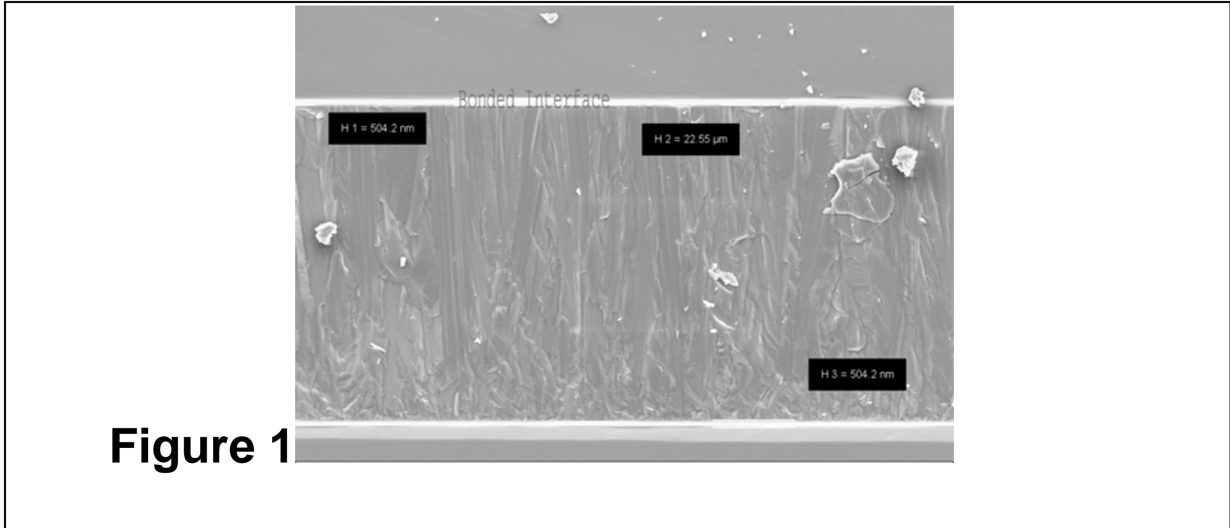


Figure 1

The developed CMP-process has been confirmed to be close to an ideal planarization process, where the roughness or tops of patterns are first abraded. This was noted to be exceptionally practical in high-roughness polysilicon polishing, where extreme topographies are commonly found. Hence, the level of necessary material removal is much lower than in a typical polishing process. Figure 2 illustrates the surface smoothening sequence in our polishing process. The development of a suitable CMP-process has achieved a state where local roughness is lowered to a level required for direct bonding as presented in Figure 3. The process uses consumables dedicated for polysilicon smoothening. An initial process removes the major roughness and potential surface defects, and is followed by a finishing step to further enhance the atomic level roughness performance. Typically, removal was kept close to the lowest possible.

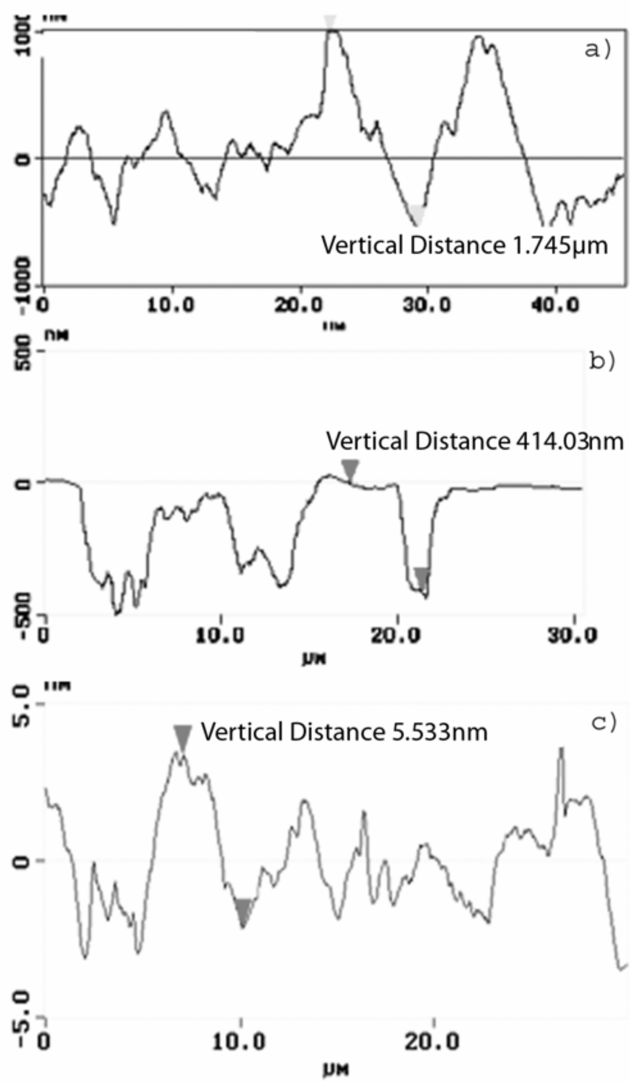


Figure 2

Figure 3

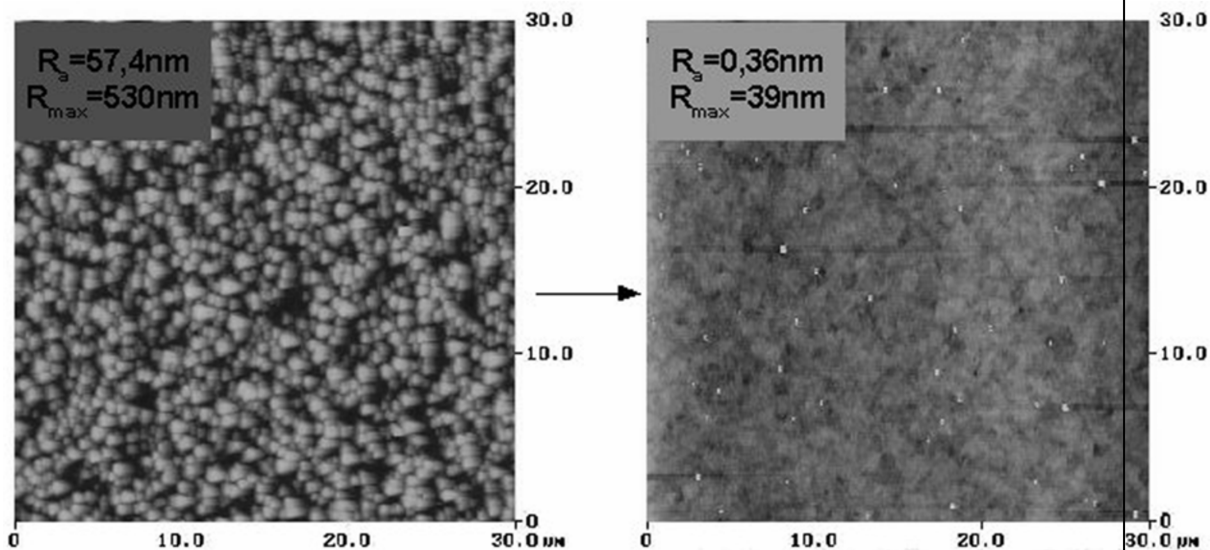


Figure 4 presents a SAM-image taken from a wafer couple where an oxidized silicon wafer with 23µm thick APCVD-grown polysilicon film is bonded to a silicon wafer with 500nm of thermal oxide. The wafer was bonded in vacuum. The visible voids suggest failure in wafer handling in otherwise successful bonding. In general, bonding in air was found to result in slightly higher surface energies than vacuum bonding. This has been also witnessed in case of hydrophilic bonding of Si and SiO_2 [6]. According to the results obtained from crack-opening-method measurements, the APCVD-grown films yield bonding strengths higher than those of the LPCVD-films. The HF-etching trials showed systematically higher surface energies corresponding to etch length than crack-opening-method. Figure 5 presents etch lengths of samples annealed at different temperatures. Results for plasma-assisted bonding are published by *Suni et al*. [3].

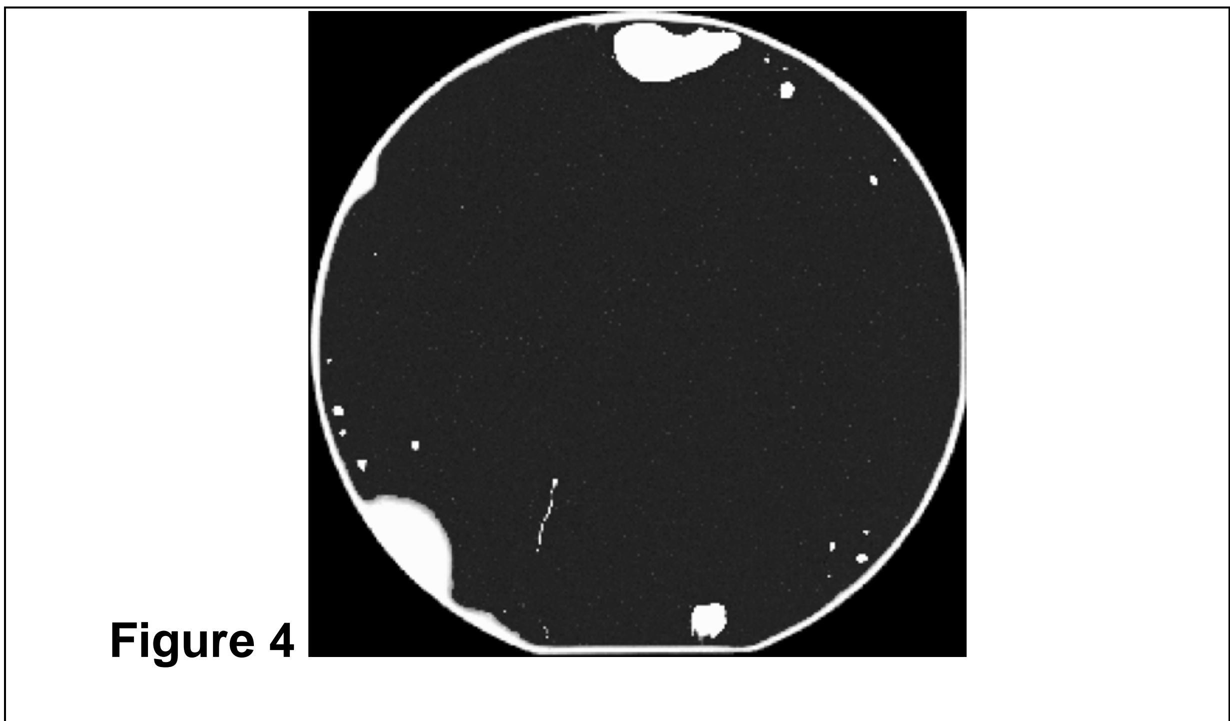


Figure 4

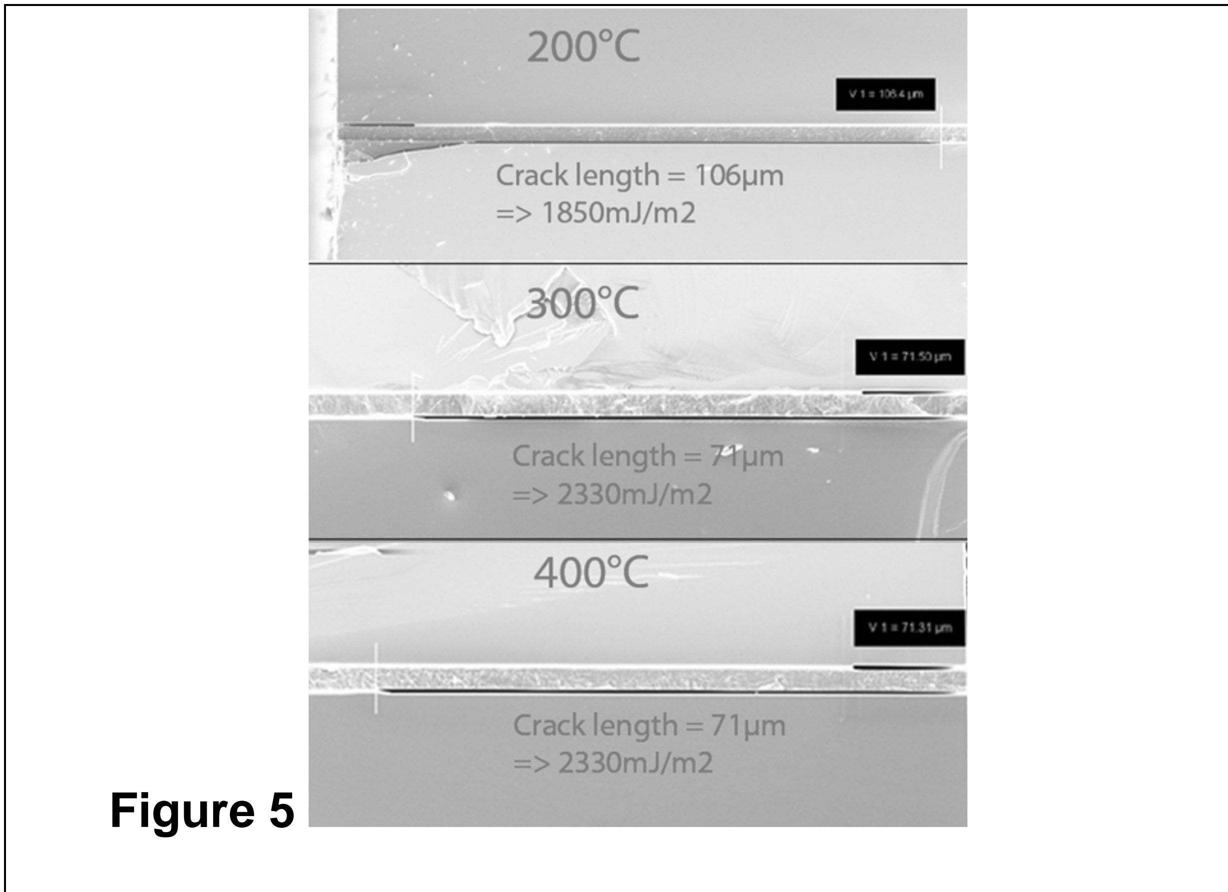


Figure 5

The surface energy and bonding quality were measured from argon activated and deionised water rinsed samples bonded to thermally oxidized silicon wafers. These samples included both LPCVD- and APCVD-films. The measurement results in Figure 6 show already moderate bond strength after annealing the wafer couples at 200°C for 2 hours.

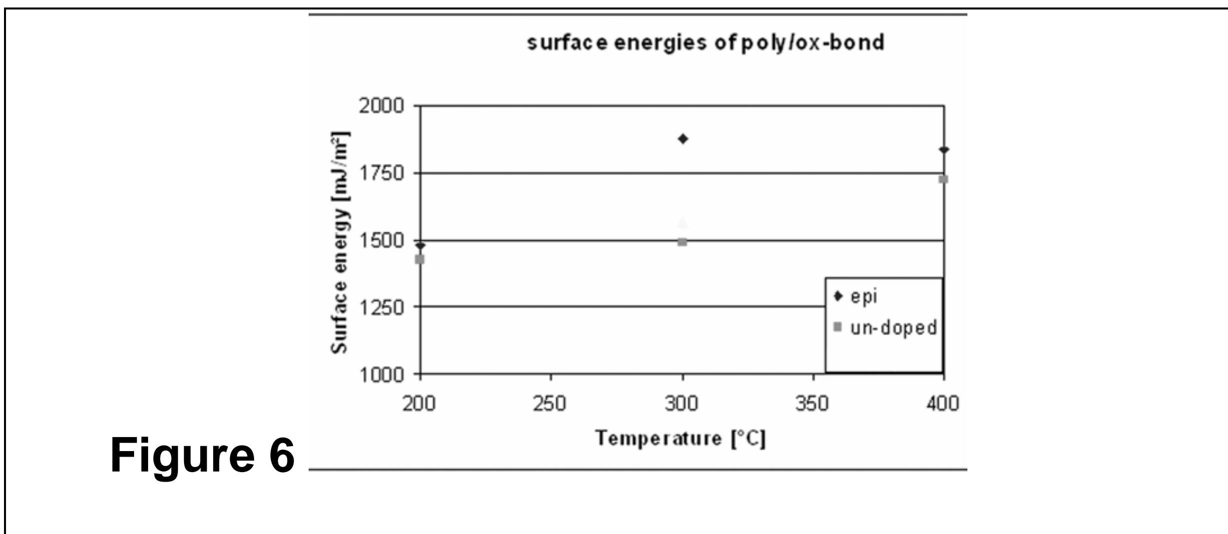


Figure 6

Additional experiments were made with bonding varying materials to polysilicon. These studies included quartz (fused silica) and Pyrex glass. Both quartz and Pyrex were treated

with conventional oxide polishing process followed by RCA-1 cleaning and argon plasma-activation with rinsing step. Quartz/APCVD-polysilicon bonding quality was confirmed visually and identified to be uniform with very few visible voids as can be seen in Figure 7.

Figure 7

Conclusions

Polysilicon LT-direct bonding as a method for wafer-scale-packaging and vacuum encapsulation has been demonstrated. We have developed a new kind of polishing process, where several microns of polysilicon is removed still leaving the surface direct bondable. This is enabled by a dedicated and effectively planarizing polishing process which allows polishing and LT-direct bonding of patterned wafers as well. The required amount of removal is dictated by the surface roughness of deposited and annealed material. Due to the ideally planarizing process, material removal is close to the roughness amplitude of the deposited and annealed films. Understanding of the polysilicon and the grain boundary behavior under CMP has been greatly improved.

Bonding strengths of around 2000 mJ/m^2 and almost void-free interfaces are verifiably achievable. Demonstration of the LT-direct bonding of polysilicon to glass has been done.

References

[1] Liwei Lin, Presentation: “Packaging Schemes for MEMS”, University of California at Berkeley, pp. 38-42, 17.6.2004

[2] Q. Y. Tong, U. Gösele, “Semiconductor Wafer Bonding, Science and Technology”, New York, USA, John Wiley & Sons Inc., 1999

[3] T. Suni, J. Kiihamäki, K. Henttinen, I. Suni, J. Mäkinen, ”Characterization of Bonded Interface by HF Etching Method”, Semiconductor Wafer Bonding VII: Science, Technology and Applications, Electrochemical Society, pp. 70-75, 2003

[4] P. A. Krulevitch, “Micromechanical Investigations of Silicon and Ni-Ti-Cu Thin Films”, Ph.D. thesis, University of California, Berkeley, 1994

[5] Retardation in the Chemical-Mechanical Polish of the Boron-Doped Polysilicon and Silicon, W. L. Yang, C-Y Cheng, M-S Tsai, IEEE Electron Device Letters. Vol. 21, No.5, May 2000

[6] T. Suni, K. Henttinen, I. Suni, J. Mäkinen, ”Effects of Plasma Activation on Hydrophilic Bonding of Si and SiO_2”, J. Electrochem. Soc., 149 (6), G348, 2002

Figure 1. Cross sectional SEM-image of bonded wafer couple Si/LPCVD-polysilicon seed layer/APCVD-polysilicon/Ox/Si.

Figure 2. Line section analysis from an AFM-image taken from a) as-deposited APCVD-polysilicon surface, b)APCVD-polysilicon surface after 100 s polishing and c) the surface after first polishing step when only atomic scale roughness is remaining. Here, no other material loss than peak reduction (ideal planarization) is expected to take place.

Figure 3. LPCVD-polysilicon (thk. 4µm) before and after two-step CMP-process. White dots on the image after CMP are residual abrasive particles.

Figure 4. SAM image of bonded APCVD-grown polysilicon/ox. White areas are voids.

Figure 5. SEM-images of bonded interfaces etched with 50% HF-solution for 10 minutes. Surface energies corresponding to etch propagation lengths are shown with each annealing temperature. The equivalence is taken from [3].

Figure 6. Surface energies of vacuum bonded polysilicon/ox-couples.

Figure 7. A photograph of quartz wafer bonded to a silicon wafer with a polished APCVD-polysilicon film (thickness 23µm).

Published by

VTT

Series title, number and report code of publication

VTT Publications 611
VTT–PUBS–611

Author(s)
Kulawski, Martin

Title

Advanced CMP Processes for Special Substrates and for Device Manufacturing in MEMS Applications

Abstract

The present work reports on studies and process developments to utilize the chemical mechanical planarization (CMP) technology in the field of micro electrical mechanical systems (MEMS). Approaches have been undertaken to enable the manufacturing of thick film SOI (silicon-on-insulator) substrates with a high degree of flatness as well as utilizing CMP for the formation of several novel MEMS devices. Thick film SOI wafers are of high interest in MEMS manufacturing as they offer obvious benefits as a starting material or foundation for more complex structures. Precise control of the SOI layer thickness as well as the removal uniformity is of critical importance to fully utilize the benefits of this technology. By combining fixed abrasive (FA) pads for polishing and novel grinding techniques it is shown that major improvements can be achieved over the standard manufacturing sequence. Analysis of the material removal rate (MRR) dependency on several process parameters is made. Together with the FA pad vendor a suitable consumable set for SOI is generated, which shows long term stability in the generated process. A comparison with standard methods is undertaken to prove the surface and crystalline quality of the material is equivalent. Analysis is done to understand the microscopic mechanism of removal. The CMP process is applied to several MEMS structures to smooth deposited oxide films and to enable direct wafer bonding (DWB) at low temperatures. This allows the design of bonded multiple stack layers including heat sensitive materials such as metals. FA CMP is applied to large pattern MEMS for total planarization but also for smoothing of the surface of single protruding structures while minimizing edge rounding and preserving the original intended pattern shape. With dedicated CMP steps thick film polysilicon smoothing is demonstrated enabling DWB. The mechanical particularities of the FA pad are investigated in detail.

Keywords
CMP, micro electro mechanical systems, polishing, fixed abrasive, MEMS, SOI, silicon-on-insulator, direct wafer bonding, DWB, low temperature bonding, FA

ISBN
951–38–6855–9 (soft back ed.)
951–38–6856–7 (URL: http://www.vtt.fi/publications/index.jsp)

Series title and ISSN
VTT Publications
1235–0621 (soft back ed.)
1455–0849 (URL: http://www.vtt.fi/publications/index.jsp)

Project number

Date	Language	Pages	Price
September 2006	English	80 p. + app. 60 p.	C

Contact
VTT Technical Research Centre of Finland
Tietotie 3, P.O. Box 1000, FI-02044 VTT, Finland
Phone internat. +358 20 722 111
Fax +358 20 722 7012

Sold by
VTT Technical Research Centre of Finland
P.O.Box 1000, FI-02044 VTT, Finland
Phone internat. +358 20 722 4404
Fax +358 20 722 4374

Chemical mechanical planarization (CMP) is a comparably new technology, being introduced in the eighties to overcome problems with increasing topography on the ever shrinking integrated circuits (IC) and the demand of multilayer metallization. The topography is removed by polishing the extent amount of material using an elastic polishing pad and chemically active polishing agent with added abrasive particles. Since then the process has seen a rapid evolution and was introduced into several areas of the IC production.

The present work reports on studies to utilize CMP in the field of micro-electro-mechanical systems (MEMS) to create a new technology platform for the future demands of the growing micromechanical world.

Approaches have been undertaken to enable the manufacturing of thick film SOI (silicon-on-insulator) substrates with a high degree of flatness. These wafers are of high interest in MEMS manufacturing as they offer obvious benefits as a starting material or foundation for complex structures. Precise control of the SOI layer thickness and uniformity is achieved by using novel fixed abrasive (FA) pads.

Standard and FA CMP is applied to several MEMS structures for smoothing of deposited oxide and thick polysilicon films to enable direct wafer bonding (DWB) at low temperatures. This allows the formation of 3-D structures including heat sensitive materials such as metals. FA CMP is further applied to large pattern MEMS for total planarization while avoiding degradation of the pattern shape. The FA pad is investigated in detail, compared with standard CMP and the mechanism of removal is discussed.

This book summarizes about 3 years of exciting research and development to contribute to the success story of one of the youngest and most widely growing processes in the semiconductor industry.

Tätä julkaisua myy	Denna publikation säljs av	This publication is available from
VTT	VTT	VTT
PL 1000	PB 1000	P.O. Box 1000
02044 VTT	02044 VTT	FI-02044 VTT, Finland
Puh. 020 722 4404	Tel. 020 722 4404	Phone internat. +358 20 722 4404
Faksi 020 722 4374	Fax 020 722 4374	Fax +358 20 722 4374

ISBN 951-38-6855-9 (soft back ed.)
ISSN 1235-0621 (soft back ed.)

ISBN 951-38-6856-7 (URL: http://www.vtt.fi/inf/pdf/)
ISSN 1455-0849 (URL: http://www.vtt.fi/inf/pdf/)

Martin Kulawski