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Kimmo Solehmainen

Fabrication of microphotonic waveguide components on silicon

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VTT, Bergsmansvägen 3, PB 1000, 02044 VTT
tel. växel 020 722 111, fax 020 722 4374

VTT Technical Research Centre of Finland, Vuorimiehentie 3, P.O.Box 1000, FI-02044 VTT, Finland
phone internat. +358 20 722 111, fax + 358 20 722 4374

VTT, Tietotie 3, PL 1000, 02044 VTT
puh. vaihde 020 722 111, faksi 020 722 7012

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VTT Technical Research Centre of Finland, Tietotie 3, P.O. Box 1000, FI-02044 VTT, Finland
phone internat. +358 20 722 111, fax +358 20 722 7012

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Keywords inductively coupled plasma etching, integrated optics, microphotonics, optical device fabrication, optical losses, silicon-on-insulator (SOI) waveguides, waveguide bends

Abstract

This thesis reports on the development of silicon-based microphotonic waveguide components, which are targeted in future optical telecommunication networks. The aim of the work was to develop the fabrication of silicon microphotonics using standard clean room processes which enable high volume production. The waveguide processing was done using photolithography and etching. The default waveguide structure was the rib-type, with the waveguide thickness varying from 2 to 10 μm. Most of the work was done with silicon-on-insulator (SOI) wafers, in which the waveguide core was formed of silicon. However, the erbium-doped waveguides were realised using aluminium oxide grown with atomic layer deposition. In the multi-step processing, the basic SOI rib waveguide structure was provided with additional trenches and steps, which offers more flexibility to the realisation of photonic integrated circuits.

The experimental results included the low propagation loss of 0.13 and 0.35 dB/cm for SOI waveguides with 9 and 4 μm thicknesses, respectively. The first demonstration of adiabatic couplers in SOI resulted in optical loss of 0.5 dB/coupler and a broad spectral range. An arrayed waveguide grating showed a total loss of 5.5 dB. The work with SOI waveguides resulted also in a significant reduction of bending loss when using multi-step processing. In addition, a SOI waveguide mirror exhibited optical loss below 1 dB/90° and a vertical taper component between 10 and 4 μm thick waveguides had a loss of 0.7 dB. A converter between a rib and a strip SOI waveguides showed a negligible loss of 0.07 dB. In the Er-doped Al_2O_3 waveguides a strong Er-induced absorption was measured. This indicates potential for amplification applications, once a more uniform Er doping profile is achieved.

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Avainsanat inductively coupled plasma etching, integrated optics, microphotonics, optical device fabrication, optical losses, silicon-on-insulator (SOI) waveguides, waveguide bends

Tiivistelmä

Tässä väitöskirjatyössä kehitettiin piipohjaisia mikrofotoniikan valokanavakomponentteja, jotka on tarkoitettu käytettäväksi tulevaisuuden optisissa tietoliikenneverkoissa. Työn tavoite oli kehittää piipohjaisen mikrofotoniikan valmistusta käyttäen yleisesti käytössä olevia puhdastilaprosesseja, jotka mahdollistavat suuret valmistusmäärät. Valokanavien valmistuksessa käytettiin fotolitografiaa ja syövytystä. Valokanavat olivat perusrakenteeltaan harjannetyyppiä, ja niiden paksuus vaihteli kahdesta kymmeneen mikrometriin. Suurin osa työstä tehtiin välioksidoiduilla piikiekoilla (silicon-on-insulator, SOI), jolloin valokanava muodostui piistä. Erbiumilla seostetut valokanavat tehtiin sen sijaan alumiinioksidiin, joka oli valmistettu atomikerroskasvatuksella. Moniporrasprosessoinnissa SOI-harjannevalokanavan perusrakenteeseen lisättiin ylimääräisiä uria, joiden ansiosta valosignaalin ohjaukseen perustuvien integroitujen piirien toteutus muuttuu joustavammaksi.

Kokeellisiin tuloksiin kuuluivat alhainen etenemishäviö 9 ja 4 µm:n paksuisilla SOI-valokanavilla, joiden häviöiksi mitattiin 0,13 ja 0,35 dB/cm. Ensimmäisillä SOI-valokanaviin valmistetuilla adiabaattisilla optisilla tehonjakajilla saavutettiin 0,5 dB:n optinen häviö komponenttia kohden sekä laaja aallonpituusalue. Optiselle aallonpituusjaotinkomponentille mitattiin 5,5 dB:n häviö. SOI-valokanavilla saavutettiin myös merkittävä kaarroshäviön pieneneminen käyttäen moniporrasprosessointia. SOI-rakenteeseen perustuvan valokanavapeilin optinen häviö oli alle 1 dB/90°. 10 ja 4 µm:n paksuisten valokanavien välille tehdylle liitoskomponentille mitattiin puolestaan 0,7 dB:n häviö. Komponentti, joka muunsi harjannetyypin SOI-valokanavan suorakulmaiseksi valokanavaksi, aiheutti vähäpätöisen, 0,07 dB:n suuruisen häviön. Erbiumilla seostetuista Al_2O_3-valokanavista mitattiin voimakas erbiumin aiheuttama absorptio. Tämä viittaa mahdollisuuksiin valokanavavahvistimien tuottamisessa, kunhan saavutetaan tasaisempi erbiumin seostusprofiili.

Preface

The work presented in this thesis was carried out during the period 2001–2006 at the VTT Technical Research Centre of Finland in Espoo, Finland. The current name of the research group is the Microphotonics team at the VTT MEMS and micropackaging centre. The results presented in this thesis were obtained as part of the VTT projects OWALE, SOIWAVE, and MEPHISTO. I wish to thank Planar Systems Inc., the European Space Agency, the European Community (the Sixth Framework Programme), and VTT for their financial support of these projects. I am also grateful to the Academy of Finland for providing me with a position at the Graduate School of Electronics Manufacturing at Helsinki University of Technology during 2002–2005, which greatly supported my postgraduate studies.

Of the many people I am grateful to, I would like first to thank my advisor, Dr. Timo Aalto, for his invaluable support during these years. Prof. Harri Lipsanen is acknowledged for supervising this thesis. Many thanks to Päivi Heimala for her cooperation and guidance in clean room processing and in the scientific writing. The enormous support from my dear colleagues Markku Kapulainen, Mikko Harjanne, and Dr. James Dekker is highly appreciated. Furthermore, I would like to thank Dr. Georges Przyrembel and Prof. Berndt Kuhlow at the Fraunhofer Institute for Telecommunications, the Heinrich-Hertz-Institute in Germany, Dr. Kaupo Kukli and Prof. Markku Leskelä at the Department of Chemistry, University of Helsinki, as well as Kirsi Polamo and Dr. Runar Törnqvist for contributing to the publications and research projects which form the basis of this thesis.

Several people have helped me through a range of challenging problems in the clean room. Among them I especially would like to thank Teija Häkkinen, Kirsi Järvi, Taru Lehtikuusi, Riitta Lindman, Merja Markkanen, Meeri Partanen, Kristiina Rutanen and Tuula Virolainen for conducting the projects or otherwise supporting my work. Mrs. Adelaide Lönnberg I thank for checking the language.

Finally, I would like to thank my wife Tiina, my relatives and my friends for their support and encouragement. And last but not least, my dear daughter Heta, thank you for providing the necessary motivation to finalise this project! On the front page you can find a small picture of Sipolansaari, an island in the North Karelia, where we will spend many of our future holidays, I dare to hope. The pattern of Sipolansaari (with your name and birthday) was actually processed in the clean room on a silicon wafer. The picture which you see is a scanning electron microscope image of the real processed silicon structure.

Kimmo Solehmainen, Espoo, October 2006.

Contents

List of publications

This thesis is based on the following original publications, which are referred to in the text by their Roman numerals:

I K. Solehmainen, T. Aalto, J. Dekker, M. Kapulainen, M. Harjanne, K. Kukli, P. Heimala, K. Kolari, and M. Leskelä, "Dry-etched silicon-on-insulator waveguides with low propagation and fiber-coupling losses", Journal of Lightwave Technology, Vol. 23, No. 11, pp. 3875–3880, 2005.

II K. Solehmainen, T. Aalto, J. Dekker, M. Kapulainen, M. Harjanne, and P. Heimala, "Development of multi-step processing in silicon-on-insulator for optical waveguide applications", Journal of Optics A: Pure and Applied Optics, Vol. 8, No. 7, pp. S455–S460, 2006.

III K. Solehmainen, M. Kapulainen, M. Harjanne, and T. Aalto, "Adiabatic and multimode interference couplers on silicon-on-insulator", IEEE Photonics Technology Letters, Vol. 18, No. 21, pp. 2287–2289, 2006.

IV G. Przyrembel, B. Kuhlow, K. Solehmainen, T. Aalto, P. Heimala, and L. Moerl, "AWG based DWDM multiplexers combined with attenuators on SOI", Proc. 32nd European Conference on Optical Communication (ECOC 2006), paper We3.P.40, 2 p., September 2006, Cannes, France.

V T. Aalto, K. Solehmainen, M. Harjanne, M. Kapulainen, and P. Heimala, "Low-loss converters between optical silicon waveguides of different sizes and types", IEEE Photonics Technology Letters, Vol. 18, No. 5, pp. 709–711, 2006.

VI K. Solehmainen, M. Kapulainen, P. Heimala, and K. Polamo, "Erbium-doped waveguides fabricated with atomic layer deposition method", IEEE Photonics Technology Letters, Vol. 16, No. 1, pp. 194–196, 2004.

Publication I describes the basis of the fabrication used in this thesis. It presents the fabrication and measurements of silicon-on-insulator (SOI) optical waveguides with low propagation losses. The feasibility of atomic layer deposition in the preparation of antireflection coatings is also studied.

Publication II reports on the development of multi-step fabrication processing which allows the incorporation of additional grooves and steps into the basic optical waveguide structure. Two different multi-step fabrication processes are proposed. They are based on simple fabrication methods on a SOI platform. The processes are studied in the fabrication of different waveguide structures.

Publication III presents the design, fabrication, and characterisation of SOI-based adiabatic couplers. In the paper, the performance of the adiabatic couplers is compared with that of multi-mode interference couplers. The fabrication of the devices is based on the basic waveguide processing described in Publication I.

Publication IV utilises also basic SOI waveguide processing described in Publication I in the fabrication of arrayed waveguide gratings. The paper briefly covers the simulation, design, fabrication, and characterisation of these components.

Publication V reports on the design, simulation, fabrication, and characterisation of waveguide converters which are based on the multi-step processes described in Publication II. The converters are designed to couple light between SOI waveguides with different cross-sections.

Publication VI presents the fabrication and characterisation of erbium-doped optical waveguides on silicon. Unlike in the previous publications, the waveguide core itself is not made of silicon. Here, the waveguide material is aluminium oxide, which is deposited on the silicon dioxide coated silicon wafers using atomic layer deposition.

Author's contribution

The results presented in this thesis are based on teamwork within the research group and with the co-authors.

For Publication I, the author designed the fabrication process, supervised the clean room processing, and carried out some of the processing steps. He also carried out most of the measurements and analysed the experimental results. The manuscript was prepared by him.

For Publication II, the author designed the fabrication process and was solely responsible for the clean room processing. He actively participated in the measurements of the devices and prepared the manuscript.

For Publication III, the author designed and carried out the fabrication process. He participated in the measurements and performed the analysis of the experimental results. He also prepared the manuscript.

For Publication IV, the author was responsible for the design of the fabrication process and carried out the processing. He also participated actively in the preparation of the manuscript.

For Publication V, the author designed and carried out the fabrication process. He also participated in all the measurements and actively contributed to the preparation of the manuscript.

For Publication VI, the author participated in designing the fabrication process. He participated in the clean room fabrication and in designing the measurement setup. He conducted a significant part of the measurements and analysis of the experimental data. He also prepared the manuscript.

List of abbreviations and symbols

ALD	Atomic layer deposition
AR	Antireflection
ASE	Advanced silicon etch
AWG	Arrayed waveguide grating
BESOI	Bond and etch-back silicon-on-insulator
BOX	Buried oxide
CVD	Chemical vapour deposition
ER	Extinction ratio
FWHM	Full width at half maximum
HF	Hydrofluoric acid
ICP	Inductively coupled plasma
LPCVD	Low-pressure chemical vapour deposition
LTO	Low-temperature oxide
MM	Multi-moded
MMI	Multi-mode interference
MZI	Mach-Zehnder interferometer
PECVD	Plasma enhanced chemical vapour deposition
PIC	Photonic integrated circuit
PM	Polarisation maintaining
RIE	Reactive ion etcher
sccm	Standard cubic centimetres per minute
SEM	Scanning electron microscope
SM	Single-moded
SOI	Silicon-on-insulator
TE	Transverse electric (horizontal orientation of the electric field)
TEOS	Tetra-ethyl-ortho-silicate
TM	Transverse magnetic (vertical orientation of the electric field)
UV	Ultraviolet
VOA	Variable optical attenuator
WDM	Wavelength division multiplexer
g	Depth of an additional etch step in multi-step processing
H	Thickness of a waveguide
h	Thickness of the slab surrounding a rib waveguide
n	Refractive index of a material
t	Thickness of a thin film
W	Width of a waveguide
λ	Wavelength in a vacuum (default 1550 nm)

1 Introduction

1.1 Background

The rapid development of microelectronic circuits over the past fifty years has had a significant impact on modern society. Computers or cellular phones are but the tip of an iceberg of devices that depend on the existence of microelectronics. The most important material in the field of microelectronics has, beyond dispute, been silicon. Its combination of low raw material cost, relatively simple processing, and a useful temperature range make it currently the best compromise among the various competing materials. Intense development work has resulted in the maturity and cost-efficiency of silicon-based fabrication technology. The importance of microelectronics in our every-day lives, and the main role of silicon in it, has inspired what we call the "silicon age"—succeeding the stone, bronze, and iron ages as the material eras of mankind [1–2].

Thus far, silicon has been associated primarily with electronic devices. In optical applications it is known in its oxidised form, silicon dioxide, as the ingredient of the optical fiber. However, optics can also be realised on a silicon chip [3]. Microphotonics is the related technology involving the manipulation of light on a microscopic scale. It can be viewed as the equivalent to microelectronics, the electrical signal being replaced by an optical one. The analogy may become clearer when we consider the propagation of a signal. Whereas an electrical signal resides in the region of high electrical conductivity, an optical signal propagates along the region of high refractive index. The equivalent to an electrical wire in microphotonics is an optical waveguide, which has the refractive index higher than that of the surrounding material. Similarly, photonic integrated circuits (PICs) correspond to electrical integrated circuits. The basic functions in PICs are the generation [4–5], guiding [6], splitting [7], multiplexing [8], amplification [9], switching [10], and detection of the light signal [11–12].

All these basic functions have already been demonstrated on silicon. However, in many cases the performance of the device has not been sufficient, or the fabrication technology has been too costly to enable successful

commercialisation. Thus, silicon microphotonics is still in its infancy and many technical challenges are yet to be solved. Perhaps the biggest challenge of Si based microphotonics has been the realisation of efficient and low-cost light sources and modulators. Only in the last few years has there been significant progress in this area [13–17]. Examples of other challenges are the optical coupling of the waveguide chips to the standard optical fibers, the miniaturisation of the PICs, optical loss reduction, and wavelength dependency. Most of these aspects are discussed in this work. The technological approach of silicon microphotonics is to take advantage of the mature and widespread state of silicon based microelectronics. This is possible because the same tools and, in many cases, similar process steps can be used both in microelectronics and microphotonics. An excellent book on processes belonging to the field of microfabrication has been written by Franssila [18].

There are several different waveguide structures that can be used to realise a waveguide on silicon, as shown in Fig. 1. The simplest is the slab waveguide (Fig. 1.a), which has a uniform high-index layer on a low-index cladding layer. Although the slab waveguide offers only lateral confinement, and cannot therefore confine light horizontally, parts of some photonic components are based on the slab structure. From the waveguide types offering full confinement, a strip waveguide (Fig. 1.b) can be formed from the slab structure with photolithography and etching techniques. In photolithography, the pattern of a laser-drawn photomask is transferred to a resist layer. The patterned resist protects the top of the waveguide core when the excess high-index core layer is etched away. The etching can be done with a wet or dry etching process. In wet etching, the solid material changes into soluble products in the presence of a liquid etchant. In dry etching, the etching element is gaseous. After etching of the waveguide structure, a top cladding layer is typically deposited to provide a uniform low-index surrounding for the core.

A variation of the strip waveguide is a rib waveguide (Fig. 1.c), in which the high-index core layer is not fully etched. However, the difference between the effective indices of the partially etched slab and the rib is sufficient to confine the light within the rib section. A modest but sometimes sufficient optical confinement can be obtained by realising a strip of cladding material on top of a slab waveguide, resulting in a strip-loaded waveguide (Fig. 1.d). The final example of different waveguide structures is a diffused waveguide (Fig. 1.e). In

the diffused waveguide the refractive index difference is achieved by local doping with an element which changes the refractive index.

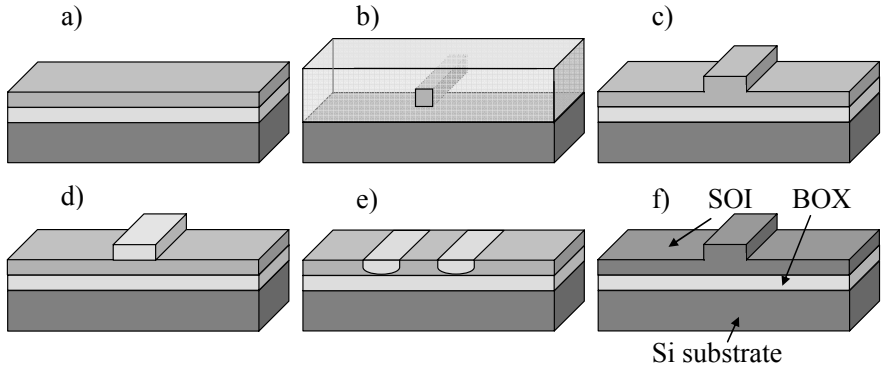

Fig. 1. Schematic presentation of different waveguide structures. The waveguide core layer is shown in dark grey. The cladding layers are shaded in light grey. The waveguide structure rests on a silicon substrate (very dark grey). a) Slab waveguide, b) strip waveguide, c) rib waveguide, d) strip-loaded waveguide, e) diffused waveguide, and f) rib-type SOI waveguide.

As there are several different waveguide structures available, there are also many materials that can be used to realise a waveguide on silicon. These include e.g. silicon dioxide [19], silicon oxynitride [20], polymers [21], germanium [22], and silicon itself. Also III–V semiconductors have been structured on silicon [23]. From the different material systems available, silicon-on-insulator (SOI) is becoming an important platform for realising PICs and for integrating them monolithically with control electronics. SOI technology takes advantage of commercially available SOI wafers that have a single-crystal Si layer (SOI layer) on top of a buried oxide (BOX) layer made of SiO_2. This structure readily acts as a slab waveguide. From this, the realisation of strip and rib waveguides is straightforward. Due to the ultra-high refractive index contrast between Si (n = 3.48) and SiO_2 (n = 1.47), SOI technology allows large-scale integration of optical circuits. Extreme device miniaturisation can be achieved with sub-micron nanowires [24–25]. In this work, the most often-used waveguide structure was the rib-type SOI waveguide shown in Fig. 1.f). Compared with nanowires, rib waveguides with a larger cross-section offer lower coupling losses to optical fibers and lasers, while maintaining single-mode (SM) operation [26].

There are a number of techniques that can be used to grow the core and cladding materials for a waveguide on a silicon wafer. In principle, any of the deposition techniques known in microfabrication can be applied. These include thermal oxidation, sputtering, chemical vapour deposition, flame hydrolysis deposition, ion-assisted deposition, spin-coating, sol-gel technique etc. The given application and chosen material system determine the requirements for the deposited thin film. However, there are some common requirements that the deposition technique must fulfil. First of all, the thin film should enable low optical losses. This means that the surface roughness should be low and the material should have a negligible amount of impurities that can absorb light in the operating wavelength. For example, a high hydrogen content in a glass film grown with plasma enhanced chemical vapour deposition results in strong absorption at telecommunication wavelengths [27]. It is important to be able to control the film thickness accurately, since the waveguide thickness is one of the main design parameters. Especially in the case of phase-sensitive components, film thickness uniformity is of significant importance. Furthermore, the deposited film should exhibit low stress. In addition to the above requirements, the film deposition technique should have a sufficiently high growth rate and it should be low-cost, reproducible, versatile, and scalable to mass production.

One of the deposition techniques fulfilling most of these requirements is atomic layer deposition (ALD) [28], which was applied in this work in the realisation of antireflection coatings on waveguide facets and also in the deposition of the waveguide core layer in erbium-doped waveguides. The aim of Er-doping is to achieve an optical amplification similar to that attained with erbium-doped fiber amplifiers [29]. Erbium is used because it is capable of amplifying optical signals at wavelengths around 1550 nm by stimulated emission, if sufficient population inversion of the metastable energy state is obtained. Several different techniques and materials have been used to produce Er-doped waveguides on Si [9, 30–33]. Silicon itself would be the ideal host for an integrated optical amplifier in Si based microphotonics. Indeed, Er-doping in Si has been demonstrated using ion implantation and molecular-beam-epitaxy techniques [34–35]. However, there are some drawbacks with this. First, the maximum concentration of optically active Er ions that can be achieved in single-crystal Si is rather limited [36]. Second, the non-radiative de-excitation of the metastable energy state is relatively high in Er-doped Si. Compared to silicon, there are

materials that allow a higher Er concentration as host material, such as Al_2O_3 [37], which was used in this work.

1.2 Objectives of the thesis

The relatively high scattering loss at the sidewalls of SOI waveguides is seen as a drawback of SOI against competing technologies. This is due to the high refractive index difference between the core and cladding layers, which also induces unwanted reflections at the input and output facets of the SOI waveguides. Thus, the first aim of this work was development of the SOI waveguide fabrication technology to achieve low propagation and fiber-coupling losses. The fabrication process was based on dry etching of silicon, which ensures good control of critical dimensions in waveguide formation.

Another important objective of the thesis was the development of multi-step processing. Here, the target was to demonstrate simple, cost-effective and scalable fabrication steps for the realisation of photonic structures using more than one etch mask. This was seen to enable advanced waveguide structures, which would result in e.g. bend loss reduction and conversion between different waveguide sizes and types. The demonstrations were chosen to be done with two masks using SOI technology, although the concept was aimed to be viable also for more mask levels and other material systems.

Couplers and arrayed waveguide gratings (AWGs) belong to the basic building blocks of photonic integrated circuits. Optical couplers are used to couple light between different waveguides, whereas AWGs are used for spatial combining or separation of different wavelengths. One of the aims of this thesis was to test the developed fabrication technology in the realisation of these devices.

The final specific target was to apply atomic layer deposition in the fabrication of microphotonic waveguide components. In particular, the aim was to prove the feasibility of ALD in the realisation of antireflection coatings and Er-doped waveguides.

2 Fabrication and characterisation methods

2.1 Basic waveguide fabrication in SOI

During this work, the most often-used waveguide type was the SOI rib waveguide. The main steps involved in the fabrication process of such waveguides are illustrated in Fig. 2. These steps can be divided into mask patterning (steps 1–6), Si etching (steps 7–8) and cladding oxide deposition (step 9), which are described in detail here.

The most commonly used starting wafer was a bond and etch-back SOI (BESOI) wafer with ~10 µm thick SOI layer [38]. Epitaxially thickened Smart Cut™ wafers were used for the fabrication of SOI waveguides with thickness below 5 µm [39]. All SOI wafers had resistivity above 10 Ωcm. Such a high resistivity ensured that material absorption had a negligible effect on the propagation loss of the optical signal. The buried oxide layer was typically 1 µm thick, which was sufficient for optical isolation of the SOI layer from the Si substrate.

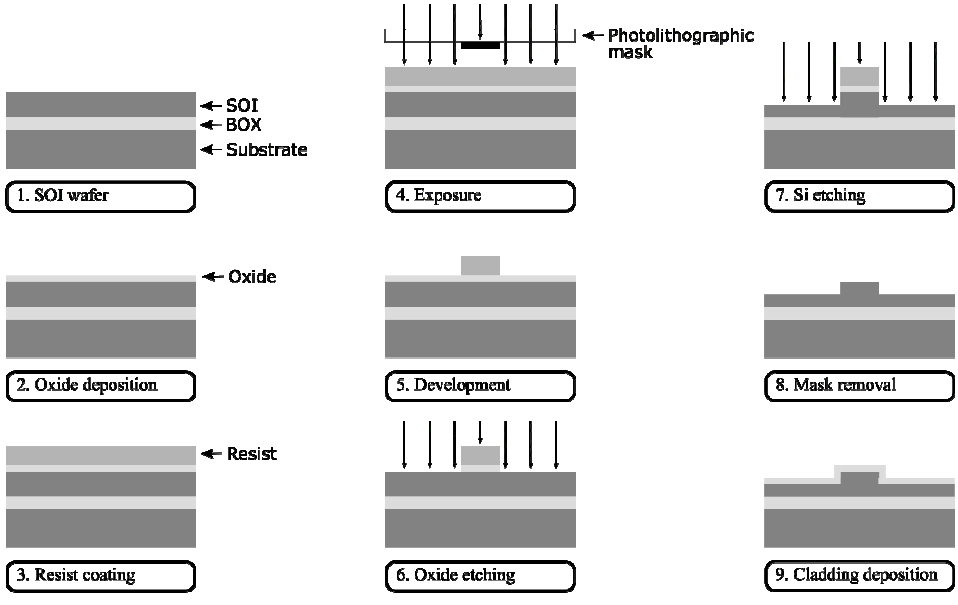

Fig. 2. Process steps for the fabrication of a rib SOI waveguide.

Although a resist layer was sufficient as the mask for Si waveguide etching, it was customary to use an additional hard mask layer beneath the resist. Its purpose was to ensure the protection of the waveguide top surface during Si etching. It was also used as the second mask layer in multi-step processing. A wide range of materials can be used as a hard mask, such as silicon dioxide, aluminium oxide, silicon nitride, or various metals. Silicon dioxide was chosen because it is widely used and well-known mask material and the SiO_2 deposition processes were readily available. The deposition was done in a low-pressure chemical vapour deposition (LPCVD) furnace, either with a low temperature oxide (LTO) or with a tetra-ethyl-ortho-silicate (TEOS) process. A thermal oxide layer was also used as the oxide mask. In that case, however, the silicon consumption (45% of the resulting oxide thickness) changed the SOI layer thickness. This had to be taken into account in designing the waveguide dimensions.

The pattern of the photomask, which included the waveguide structures, was transferred to the oxide mask using standard photolithography (steps 3–5 in Fig. 2) and oxide dry etching. The main steps of the photolithography included resist coating, exposure, and development, but several intermediate phases were associated with these. The lithography started with baking the wafer at 140 °C, which removed the moisture attached to the wafer surface. Then the wafer was coated in the primer oven with a monomolecular layer of hexamethyl disilazane (HMDS). Priming (or adhesion promotion) makes the wafer surface hydrophobic, which prevents moisture condensation. It also ensures known surface conditions, which improves the repeatability of the lithography process.

During spin coating a few millilitres of resist were poured onto the slowly rotating wafer. The wafer was then accelerated to a high speed of rotation, ensuring a uniform resist layer. The speed of rotation is inversely proportional to the resulting resist thickness, which can therefore be controlled. In this work the speed of rotation varied between 2000 and 5550 rpm, giving a resist thickness between 1.4 and 2.1 μm (SPRT515 resist). Following spin coating, the solvent was evaporated from the resist during a soft bake at 90 °C. A hot plate system was used for baking, and duration of 1–2 minutes was sufficient for solvent evaporation.

Exposure was done using a contact mask aligner which is the simplest and fastest system for resist patterning of a large area. The tool brings the resist-covered wafer and the photomask close to each other. During contact exposure the wafer and the mask are pressed into intimate contact. In the proximity exposure a gap of typically 5–10 μm is left to ensure that the resist does not leave any traces on the mask. After mask alignment, the resist was exposed to UV light through the photomask. UV radiation changes the solubility of the resist in exposed areas, but actual resist patterning takes place during the development step.

In this work a positive type resist was used. With such resists UV light increases the solubility of the resist when it is immersed in an alkaline-based developer. Thus the exposed areas corroded during development, and an exact replica of the photomask was formed in the resist. Another bake step, called hard bake, was applied after exposure. It was used to improve the resistance of the resist against the developer and etchants. In waveguide processing, the most important aspects of lithography are the resist profile and resolution. Thus the lithography parameters were varied to achieve as rectangular a resist cross-section as possible. The maximum resolution of the lithography was 1–2 μm, depending on the resist and the exposure parameters.

The pattern of the resist was transferred to the oxide hard mask during oxide etching, shown in step 6 of Fig. 2, using a reactive ion etcher. In reactive ion etching (RIE), the etching is caused by ions and reactive molecules produced by creating plasma from the source gases. The plasma is generated using a radio frequency electric field. In the chamber the ion bombardment is accelerated towards the wafer surface. This enables anisotropic (vertical) etch profiles, which is the main advantage of RIE compared to wet etching in hydrofluoric acid (HF), which can also be used in oxide etching. The anisotropic nature of RIE was beneficial for patterning of the hard mask, since it was desirable to transfer the dimensions of the photomask to the final waveguide structures as accurately as possible.

The gases used to build up the plasma in the RIE process were CF_4, CHF_3 and He. The operating pressure in the oxide etch recipe was 2.5 Torr and the power was 600 W. The SiO_2 etch rate was approximately 350 nm/min. Although the etching process is chosen so that the mask material is not etched, this is seldom

achieved perfectly. Selectivity is a measure of this feature. It is the ratio of the etch rates between the material to be etched and the mask material. In the case of RIE it is the physical nature of etching that results in unwanted removal of the mask material. The resist etch rate in the oxide etch process used in this work was measured to be around 250 nm/min. This results in rather low selectivity of 1.4. In practice this is not a major problem, since the resist thickness can be chosen accordingly so that the resist layer does not wear out.

Silicon etching was done using an inductively coupled plasma (ICP) etcher provided by Surface Technology Systems (STS). A photograph of the ICP etcher used in the experiments is shown in Fig. 3. The ICP etcher is basically an RIE system in which the plasma is produced by electromagnetic induction. Compared to other RIE systems the main advantage of ICP etcher is the improved confinement of the plasma, enabling high plasma densities at low operating pressures. This leads to an increase in etch rates while sustaining low etching damage. ICP etchers are known for their ability to etch very deep structures with almost vertical sidewalls. It can be used, for example, to etch completely through a silicon substrate [40].

In waveguide etching the etch depth is relatively low, typically below 10 µm. However, nearly 90° verticality and low etching damage are very important requirements for waveguide fabrication. Furthermore, a wide operating window of ICP etching enables further optimisation of the basic processes. This is important, since the waveguide process requires extremely low surface roughness on the etched sidewalls, a property which is not optimised in the default processes. Especially in SOI waveguides, where the high refractive index difference between the Si core and oxide cladding enhances the roughness-induced optical losses, the etched waveguide sidewall should be very smooth [41].

Fig. 3. Photograph of ICP etcher used in Si etching. (Picture courtesy of Gao Feng.)

The Si etching process used in this work was a modification of the STS advanced silicon etch (ASE), which is a pulsed (Bosch) type process [42]. In the ASE process the etching and passivation cycles are alternated subsequently. The etching and passivating gases are SF_6 and C_4H_8, respectively. During the etch cycle SF_6 gas supplies fluorine radicals, which etch silicon isotropically. The verticality is ensured in the subsequent passivation cycle, in which a thin polymer film is deposited on the etched silicon sidewalls to prevent lateral etching under the mask. A scanning electron microscope (SEM) picture of a sidewall etched with the ASE process is shown in Fig. 4(a). The subsequent etching and passivating cycles result in an undulated structure. If the undulation were perfectly regular along the direction of the propagation of light, it would not cause excess optical losses. However, the pulsed etching also increases random surface roughness, which is a source of optical propagation losses. Thus, the default ASE process is not ideal for waveguide fabrication.

It is important to note the very smooth upper part of the etched sidewall in Fig. 4(a). This is a result of the first etch cycle of the ASE process. It is obtained by etching the first 0.5 μm with continuous passivation, so that the etching and passivation gases are applied simultaneously. In the default ASE process its purpose is to prevent significant under-etching when no passivation is yet present. However, in this work it was extended over the whole etching step to avoid the pulsed structure and additional surface roughness. The result was an extremely smooth etched sidewall shown in Fig. 4(b).

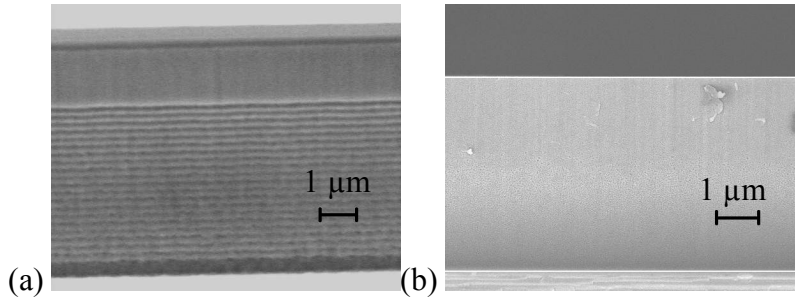

Fig. 4. SEM images of a Si waveguide sidewall etched with (a) ASE and (b) continuous passivation ICP etch process. [Publication I.]

In the continuous passivation etch recipe, the flow rate of the passivating gas was linearly increased from its initial value as the etching reached deeper. The C_4F_8 flow rate was initially 120 sccm (standard cubic centimetres per minute) and was increased at a rate of 2 sccm/min, while the SF_6 flow rate was kept constant at 40 sccm. The chamber pressure was 12 mTorr. The radio frequency generator was operated at 13.56 MHz frequency. The power connected to the coil was constant at 600 W, while the power connected to the platen was initially 30 W and was then decreased at a rate of 1 W/min. The disadvantage of continuous passivation etching is the limited etching depth, which was around 6 µm for the process used. However, for all of the waveguide structures realised in this work this maximum etch depth was sufficient. Another weakness of this process is the lower selectivity compared to the ASE process (Publication I). This was taken into account by increasing the mask thickness accordingly.

In order to estimate the quality of the etch processes, the continuous passivation and ASE etch recipes were compared in terms of residual surface roughness. The etched surfaces were measured using a Dektak profilometer. For the measurement the samples were cleaved and placed in a special sample holder, which enabled measurement from the vertical surfaces. The measured r.m.s. (root-mean-square) values of the surface roughness were 4 and 10 nm for the continuous passivation and ASE processes, respectively. It should be kept in mind that most of the roughness of the ASE process is parallel to the direction of light propagation and hence does not contribute to the optical propagation loss. However, the measurement shows the low surface roughness of the continuous passivation process. It is worth mentioning that in addition to the amount of surface roughness, the scattering losses in a waveguide also depend on the correlation length (period) of the roughness [43].

Si ICP etching was followed by the removal of the resist and oxide masks with oxide plasma and HF etching, respectively. After these steps the waveguide structure was complete. However, it is customary to deposit a cladding layer on top of the waveguide structure. Its purpose is to protect the sensitive waveguide surfaces from contamination and mechanical hazards. It can also serve as an insulating layer when an additional layer is realised on top of the waveguides. A typical example of this is a metal heater in a waveguide switch. The refractive index of the cladding layer has to be lower than that of the waveguide core material. Since the mode field of the propagating light in the waveguide extends to the cladding layer, the cladding material needs to sustain low optical absorption at the operating wavelength. In waveguides with a Si core, the cladding can be made of silicon dioxide. During this work, most of the cladding oxide depositions were done with the TEOS oxide process. TEOS oxide was chosen because it imposes the lowest stress on the waveguide structures [44]. The default cladding oxide thickness was 1 µm.

A variation of the default SOI waveguide process was a thermal oxidation step before deposition of the cladding oxide. This was done to reduce surface roughness of the waveguide sidewalls after Si etching [45]. It was also used to introduce a controlled linewidth change when fabricating vertical tapers (see Section 3.5), where it was necessary to narrow the finite width of the taper's tip. The thickness of the thermal oxide was 0.5–1.0 µm and it was removed with HF etching before the cladding oxide deposition.

For many basic waveguide structures, the cladding oxide deposition was the final clean-room process, after which the component chips were diced and characterised. However, for variable optical attenuators (see Section 3.4 or Publication IV), metal heaters were formed on top of the waveguide structure. One of the most commonly used metals in microelectronics fabrication is aluminium, which has also been used in waveguide applications [46]. However, the use of Al on top of narrow waveguides limits the applied heating power due to the well-known vulnerability of Al to electromigration [47]. To broaden the electrical power range of the heaters, a metallization process was developed. The process was based on molybdenum, which endures higher current densities than Al. To prevent the defects presented by corrosion, a silicon nitride passivation layer was formed on top of the heaters. The contact pads and wires, which were not as vulnerable to electromigration as the waveguide heaters, were realised using Al.

The metallization process started with sputter deposition of a 0.5 µm layer of Mo on top of the TEOS cladding. Then, a 7 µm thick resist layer was spun on top of the Mo film and patterned with standard photolithography. The Mo patterning was done with a wet etch in a room-temperature phosphorus acid bath. After etching the resist was removed. Mo was passivated with a 50 nm Si_3N_4 layer grown with plasma enhanced chemical vapour deposition (PECVD). The openings for the contact wires and pads were patterned into the Si_3N_4 layer. For this, another lithography step was carried out. After the dry-etching of the Si_3N_4 with RIE the resist was not removed, but a 1µm layer of Al was sputtered on top of the patterned resist for contact metallization. Using a lift-off process, the patterned resist and the unwanted Al on top of the resist were removed in acetone. Finally, a protection resist for dicing and polishing was spun on the wafer.

The final steps of the fabrication process were dicing the wafer and polishing the chip facets to optical quality. These were carried out with commercial tools available at VTT's facilities in Micronova. Chip dicing was performed with a Loadpoint Micro Ace 3 (Series 2). The spindle speed was 40 000 rpm and the feed rate was usually 0.5 mm/s. Waveguide facet polishing was carried out with a South Bay Technology Model 920 lapping machine with diamond lapping films. The minimum diamond grit size used in the polishing was 0.1 µm.

2.2 Multi-step processing in SOI

There are various targets and requirements for different microphotonic components. Usually SM operation is needed, which sets certain limits on waveguide dimensions. Low-cost components should also have a small footprint of the wafer. Furthermore, low insertion loss of the devices requires a low-loss connection to the optical fibers that couple the light into and out of the chip. Unfortunately, these targets often conflict. For example, thick Si rib waveguides with a large cross-section offer SM operation and a low-loss connection to standard optical fibers. However, they usually require very long bending radii, which results in large components. On the other hand, designing SM waveguide structures with a small footprint requires small waveguide cross-sections, which usually result in high fiber-coupling losses. Thus it would be useful to combine different waveguide cross-sections, each optimised for a given purpose, within a

single silicon waveguide device. This cannot be achieved using traditional waveguide fabrication with a single mask and etch step.

More flexibility can be brought to the component design by using a process with more than one etch depth. The principle is called multi-step processing. It allows the incorporation of additional steps and grooves into the basic waveguide structures, as shown in Fig. 5. The additional etch steps enable the integration of waveguides with different dimensions. The coupling of light between different cross-sections can be done adiabatically. This means that the occupation of the optical modes is preserved as the cross-section of the waveguide changes along its length. For example, if the fundamental mode is initially excited, all the power is still in the fundamental mode after a change in the cross-section. The concept of multi-step processing has been proposed before [48], but during this work the fabrication processes were developed and the principle was applied to different optical components as described in Section 3.5.

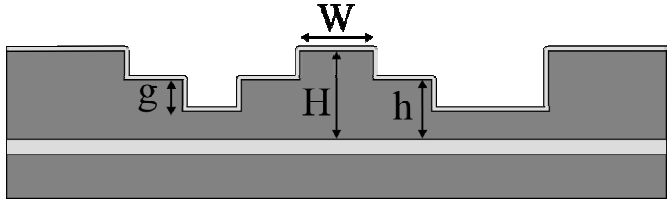

Fig. 5. Cross-sectional schematic figure of a multi-step waveguide structure. *W* is the width of the waveguide, *H* is the thickness of the basic rib waveguide structure, *h* is the thickness of the slab surrounding the rib, and *g* is the depth of an additional etch step.

The multi-step processing developed here was developed from the basic waveguide process presented in Section 2.1, with an extension to include another Si etch step. Thus, two Si etch steps and two photomasks were applied. Two different options for the fabrication sequence were tested, both having one etch step with an oxide mask and another etch step with a resist mask. The first option was to use the double-masking process shown in Fig. 6. The essence of this process was to first pattern both mask layers and then etch the structures into silicon.

In the double-masking process, the upper etch step *H-h* (basic waveguide structure) was defined first for the oxide mask. This was done by patterning a 1 µm TEOS oxide layer with standard photolithography and RIE. The Si etching

was not done at this point. Instead, the resist was removed and a new photoresist layer was applied using a different photomask. This resist layer defined the lower step (*g*) and was used in the first Si etching step (step 2 in Fig. 6). Silicon etching was done using the ICP etcher. After the etching, the resist was removed and the second Si etching step used the oxide layer as the etch mask, defining the dimension *H-h* (step 4 in Fig. 6). After oxide mask removal, a TEOS cladding oxide layer was deposited.

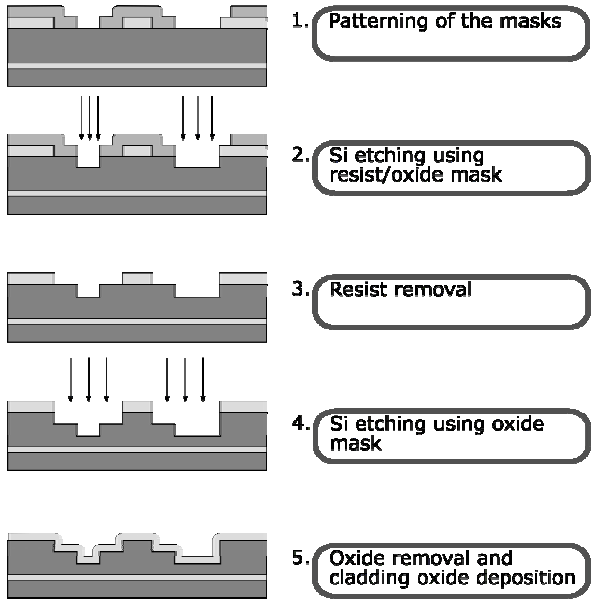

Fig. 6. Process flow for the developed double-masking version of the multi-step process. [Publication II.]

The double-masking process is capable of achieving accurate mask patterning for both etch steps, since the lithography is always done on a flat silicon surface. The only challenging part of the process is the second Si etching (step 4 in Fig. 6). After the first etch there is a topography in the Si structure, and etching this topography deeper into the silicon results in localised surface roughness. The roughness can be seen in the SEM image shown in Fig. 7. The roughness is generated at the upper edge of the lower etch step in the form of a spiky structure along the edges. It can be reduced by subsequent thermal oxidation or Si wet etching, but it is difficult to remove the residuals completely. However, the excess Si roughness might be avoided by slightly compromising the smooth waveguide sidewalls and verticality of the etch. This should be studied more,

since the double-masking process is preferred when accurate lithography and deep etching is required.

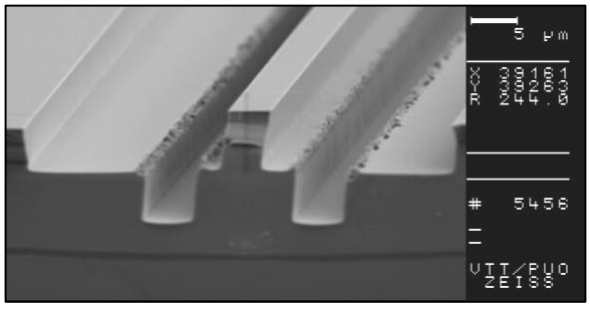

Fig. 7. Residual Si roughness formed at the corners of etched trenches.

The other process option was the sequential process, in which the basic waveguide structure and the additional grooves were fabricated sequentially as shown in Fig. 8. The upper Si etch step (*H-h*) was defined first by patterning the oxide layer with photolithography and dry oxide etching. After the Si etch the resist was removed, while the patterned oxide was left on the unetched areas. The second lithography was then done, defining the lower etch (*g*). After the second Si etch the resist and oxide masks were removed. Finally, TEOS cladding oxide was deposited.

In the sequential process, the residual Si roughness is avoided, since there are no topographical edges in Si during etching. However, the lithography in the etched trench (step 3 in Fig. 8) is an extremely demanding task with standard contact lithography. The spin-coating results in an uneven resist profile, as shown in Fig. 9. On top of the wafer surface there may be areas, where the resist does not cover the surface (point *A* in Fig. 9). Furthermore, in the bottom corner of the trench the resist is significantly thicker than elsewhere (point *B*). These defects depend strongly on the lithography parameters and the shape of the mask patterns. To circumvent these limitations, significant efforts were devoted to development of the lithography. A sufficient quality was achieved by changing the resist dispensing parameters and optimising the exposure time. The dispensing dose was set to the maximum in order to cover the whole wafer surface with resist. The exposure time was doubled from the default value to ensure a sufficient exposure dose for the resist with varying thickness.

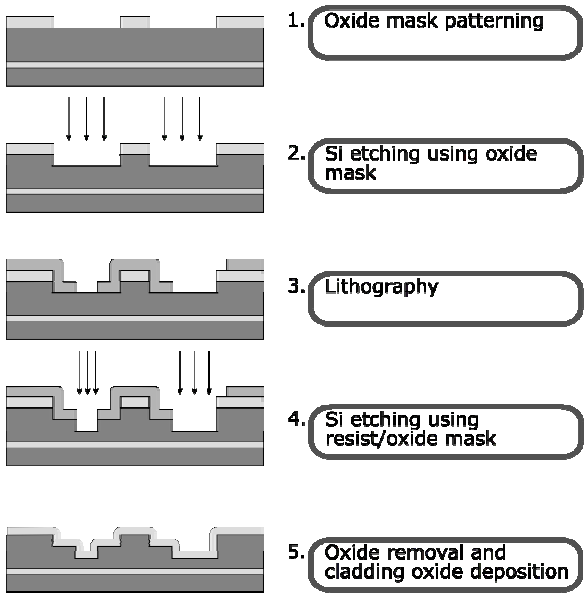

Fig. 8. Process flow for sequential multi-step process. [Publication II.]

Because of the difficulties with the second lithography step, there were limitations in the etch depth achievable with the process. The maximum depth of the first etch step depended strongly on the mask patterns and the lithography process used. With the lithography process used here the maximum depth of the first etch was approximately 6 µm. However, by using resists designed for a higher aspect ratio, it would be possible to realise structures with small features and deep etches. In general, the sequential process is advisable when the first etch is shallow, or when sharp corners must be achieved in the multi-step structure.

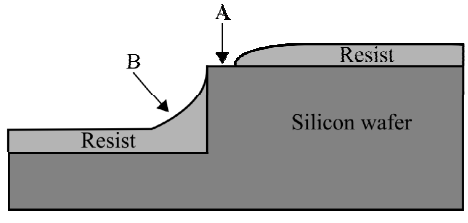

Fig. 9. Resist profile after spin-coating on an uneven silicon surface.

2.3 Atomic layer deposition in waveguide applications

Atomic layer deposition, also known as atomic layer epitaxy or ALE, was developed from chemical vapour deposition (CVD) technology in 1970s. The aim was to develop a deposition technique that could produce thin films with low defect density, high step-coverage and accurate thickness control. One of the first applications of ALD was the growth of large-area electroluminescence-based thin-film displays [49]. Since then, it has proven to be a convenient method for depositing thin films of high quality for a variety of applications and today ALD has also been adopted by large semiconductor manufacturers. In recent years a wide range of materials has been grown with ALD [50].

The ALD process is based on surface reactions of precursor gases. The method differs from many other deposition processes in that only one reactant gas is introduced in the deposition chamber at a time. Through a process called chemisorption the gas reacts with the substrate and a monolayer of the precursor is adsorbed on the surface. Under proper conditions the growth is self-limited and no more than one monolayer is deposited. After the chemisorption phase the residual gas is purged and the second gas is introduced in the chamber. This is typically water vapour, which reacts with the precursor forming a monolayer of solid material. One process cycle is completed when the second gas is purged. After this a new, identical cycle can be performed. The final film thickness depends precisely on the amount of cycles and can therefore be controlled at nanometre level. Generally, the film is deposited conformably, i.e. regardless of the surface shape.

The temperature is kept relatively low during ALD growth, typically below 400 °C. Low processing temperature ensures that the thermally induced stress in the deposited film remains reasonably low. This is particularly beneficial in waveguide applications, where stress-induced birefringence is a detrimental phenomenon. The main disadvantage of the ALD is that the film grows slowly, typically 50–300 nm/h. This drawback can be alleviated by processing a lot of components simultaneously, so that reasonably high productivity is achieved. This is possible since very large areas can be grown uniformly using ALD.

In optical applications, ALD has been used for the preparation of dielectric multilayer structures for some basic optical components such as antireflection

and high-reflection coatings, and Fabry-Perot filters [51]. However, it has not been widely used in the fabrication of photonic integrated circuits. One of the objectives of this work was to apply ALD in microphotonics. Two different applications were tested. First, it was used in the deposition of Ta_2O_5 and ZrO_2 antireflection coatings, as described in Section 3.2. The other application was the waveguide core layer deposition of Er-doped Al_2O_3 waveguides. The fabrication of the waveguides is briefly described below, and the results are given in Section 3.6.

The base for the fabrication of the Er-doped waveguides was a standard Si wafer with 100 mm diameter. The refractive index of Si is higher than that of Al_2O_3 (n = 1.64). Therefore, a lower cladding layer was needed between the Al_2O_3 core and the substrate to ensure that light could not couple between them. It was formed by depositing a 5 µm thick SiO_2 film with PECVD on the Si wafer. After the lower cladding deposition, ALD was applied for the growth of 2 µm thick Al_2O_3 core. Er-doping was done by adding Er cycles between Al_2O_3 cycles in the ALD process. The doping level was measured with X-ray fluorescence resulting in an average Er concentration of 2.3 wt-%. The measurement method did not take into account the layered doping structure. The measured doping level corresponds to an Er ion concentration of 3.2×10^{20} cm^{-3} (assuming density of 4.0 g/cm^3). This was a relatively high doping level compared with other Er-doped waveguide studies [52].

For the rib waveguide formation, a thin molybdenum film was sputter-deposited as a hard mask for the Al_2O_3 etching. The Mo film was patterned with standard photolithography and wet etching in a commercial metal etchant (PS 70/10). The Al_2O_3 wet etching in 50% phosphoric acid at 75 °C for 7.5 min was followed in order to define the waveguide structure. This resulted in an etch depth of 0.4 µm as measured with a profilometer. After resist removal the samples were immersed in NH_4OH-H_2O_2-H_2O solution to remove the Mo mask. No upper cladding was used on top of the waveguides. Finally, the wafer was cleaved into waveguide chips for optical characterisation.

2.4 Characterisation methods

The development of microphotonic devices requires the use of many different measurement methods both for process optimisation and device characterisation. During fabrication, the most important parameter to be measured is the film thickness. The main tool for thin film characterisation was a FilmTek 4000 spectrophotometer from Scientific Computing International. The tool is a computerised film thickness measurement and material characterisation system. It combines fiber-optic spectrophotometry with material modelling software to provide a tool for the simultaneous measurement of film thickness, refractive index and extinction coefficient [53]. In the measurement the spectrophotometer is used to scan the sample over a predefined range of wavelengths to obtain a reflectance spectra from both normal and 70° angles of incidence. Absolute reflectance data is obtained by comparing sample data with the measured reflectance of a known sample, which is typically a silicon wafer. This data is used to calculate the thickness and optical constants of the thin film. According to the manufacturer, the film thickness precision of the tool is better than 1 nm. During this work, spectrophotometric film thickness measurements were performed routinely. For example, the measurement system enabled accurate measurement of the SOI layer thickness, which was very important in optimising the fabrication processes. It was also used in the determination of the thickness and refractive index of antireflection coatings (see Section 2.3).

In the characterisation of the processed waveguide devices, the insertion loss measurement was the most often used. The measurement setup is shown in Fig. 10. In the setup, the input and output fibers are aligned to the waveguide chip using a computerised alignment system or manually controlled precision positioners. One end of the input fiber is connected to a light source and the other to an optical detector. The measurement starts with measuring the intensity at the output fiber using this arrangement. Then the reference intensity is determined by coupling the input fiber directly to the output fiber. The insertion loss is the difference between these intensities.

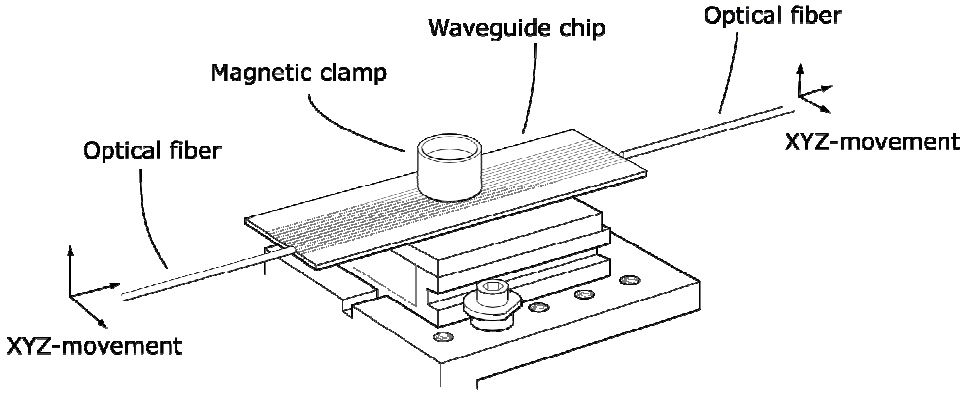

Fig. 10. Insertion loss measurement of a waveguide chip.

Depending on the particular requirements for the measurement, a broadband diode emitter or a narrowband laser was used as the light source. When using a narrowband source, the wavelength target was exclusively 1550 nm, which was the default wavelength in this work. From the light source, the input signal was guided to the waveguide using a SM or polarisation-maintaining (PM) fiber. The use of the PM fiber enabled separate insertion loss measurements for both TE and TM polarisations, which represent the two orthogonal orientations of the propagating light. In TE polarisation the electric field is aligned horizontally with respect to the Si chip. Correspondingly, TM polarisation represents the vertical alignment of the electric field. In the case of the PM input fiber, light was coupled to only one of the fiber's polarisation modes at a time. A polariser was used to align the polarisation axes of the PM fiber to those of the waveguide. This ensured that the two polarisation modes of the waveguide could be excited separately with minimum cross-talk (below −25 dB).

In the insertion loss measurement, the transmitted light from the waveguide output was coupled to a single-mode or multi-mode fiber and guided to a detector. Depending on the application, an optical power meter or a spectrum analyser was used as the detector. When using a broadband light source and a spectrum analyser, the transmission spectrum of the sample could be measured. Transmission spectrum measurement is used when measuring the spectral characteristics of an optical device, or, when studying absorption caused by impurities present in an optical layer. The overall accuracy of the insertion loss measurement was estimated as ±0.5 dB.

The measured insertion loss of a waveguide chip consists of the coupling losses, the propagation loss, and the functionality loss, which can result from e.g. bends, crossings, or dimensional changes. One of these loss components can be directly determined from the insertion loss if all the others are known. It is common to determine the coupling loss with a simulation tool if the waveguide and fiber dimensions are known. However, it is often more accurate to eliminate the effect of the coupling losses by comparing different waveguide devices with identical input and output coupling. For the determination of propagation loss, the functional losses are minimised. If, however, a functional loss is to be measured from a certain waveguide section or structure, the coupling and propagation losses can be eliminated using a suitable reference waveguide. All these options were used in the course of this work.

A typical difficulty in determining waveguide propagation loss from the insertion loss measurement is the effect of fiber-coupling losses. Although there are excellent simulation tools that can calculate modal losses accurately, dimensional uncertainties and misalignment make the coupling losses uncertain. The contribution of the fiber-coupling uncertainty has been typically minimised by measuring identical waveguides of different length. In this cut-back method the same waveguide is repeatedly measured and shortened to extract the propagation loss. However, these approaches still give rather limited measurement accuracy. A significant improvement in the accuracy of propagation loss determination is to use a very long waveguide as described in Section 3.1.

Another approach, which was also applied in this work, is the use of Fabry-Perot resonances created in the waveguide to determine the propagation loss [54]. The resonance is created by changing the phase in the waveguide, for example by tuning the wavelength of the laser or by heating the sample. The former requires a narrow band laser with bandwidth well below 10 pm, assuming that the waveguide to be measured is a few centimetres in length. This was the method used in this work (see Section 3.1). The latter option requires some additional arrangements to the typical measurement setup, so that the temperature of the sample can be controlled. The propagation loss can be calculated from the resonance fringes, provided that the reflectivity of the waveguide end facets is known. For accurate determination, the reflectivity should be calculated using simulations or models of the waveguide modal reflectivity [55–56].

Active waveguides have a number of properties to be measured in addition to those of the passive waveguides. The results from the measured Er-doped waveguide samples are given in Section 3.6. The measurement methods are described briefly here. One of the setups was emission spectrum measurement (Fig. 11), which gives information about the wavelength range and Er activity of the sample. For the emission spectrum measurements, the Er ions in the waveguide were excited by coupling light from a 980 nm pump laser to the waveguide with an SM fiber. The same fiber was also used to gather the spontaneous emission that was created in the waveguide. A 1550/980-nm wavelength division multiplexer (WDM) was used to couple the pump light to the input fiber. In this setup there was also another WDM to ensure that the residual intensity of the 980 nm light would be filtered before reaching the spectrum analyser.

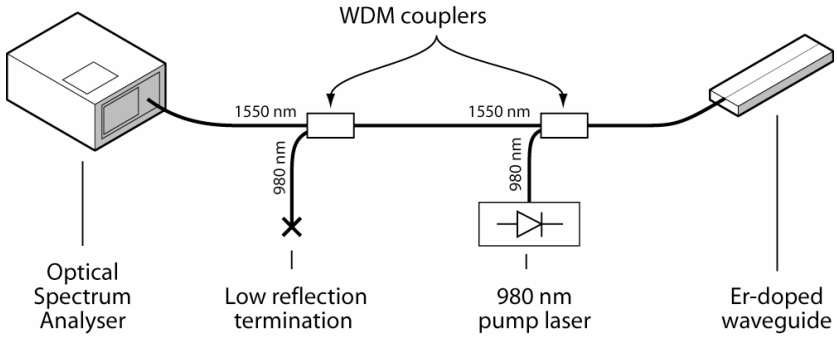

Fig. 11. Setup for emission spectrum measurement of the Er-doped waveguides.

The fluorescence lifetime is a good measure of the optical activity of Er ions. It refers to the statistical time an Er ion stays in the metastable excitation state before dropping back to the ground energy state. A short fluorescence lifetime indicates that there are not enough excited Er ions to contribute to the stimulated emission, and optical amplification may be hindered. Several physical mechanisms can reduce the lifetime. They can be divided into radiative (spontaneous emission) and non-radiative (phonon related) transitions. The fluorescence lifetime was measured with the same setup as the emission spectrum. The only differences were that instead of the spectrum analyser, the backward directed emission light was fed into an InGaAs photodetector and the pump laser was modulated with a pulse generator. The electrical output signal from the photodetector was measured with a digitising oscilloscope. The

fluorescence lifetime was defined as the time during which the emitted intensity from the waveguide dropped to 1/e of the initial intensity after the pump was switched off.

As the Er-doped waveguides are intended to be used in amplification applications, their figure of merit is gain/length expressed in dB/cm. In the gain measurement the waveguide was pumped with a 980 nm laser and the signal was provided by a tuneable narrowband laser. The signal and the pump light were combined with a 1550/980-nm WDM to a single-mode fiber, which was coupled to the waveguide input. Light from the waveguide output was coupled to a multi-mode fiber and measured with an optical spectrum analyser.

3 Device fabrication results

3.1 Low-loss rib waveguides in SOI

The fabrication of single-mode SOI waveguides with propagation losses as low as ~0.1 dB/cm has been demonstrated by others using a wet silicon etching process [57]. However, the production of functional integrated optical components using wet etching is difficult due to the modest critical dimension control. Dry etching offers the required anisotropic etch profile and is therefore preferred in practical applications. The challenge in dry etching is the surface roughness produced on the exposed sidewalls, which increases the scattering of light and thereby the optical losses. This has a pronounced effect in the SOI waveguides, because the high refractive index contrast increases the scattering losses [41]. The etching-induced surface roughness has limited the propagation losses of dry-etched SOI waveguides to 0.3–0.5 dB/cm [58–60].

In this work, the waveguide fabrication process described in Section 2.1 was used to produce SOI waveguides with record-low losses. The continuously passivated ICP process was applied in the realisation of 4 and 9 µm thick rib waveguides. Although the processing was in principle similar for these samples, details of the fabrication process differ. For example, the realisation of the mask and the cladding oxide layers were different. Thus, the fabrication parameters are given in conjunction with the following measurement results.

In the fabrication of 4 µm thick waveguides the starting wafer was an epitaxially thickened Smart Cut SOI wafer with a 4.5 µm thick SOI layer and a 1 µm thick BOX. The oxide hard mask was not used in this process. Instead, the mask patterns including simple straight test waveguides were transferred to the resist, which was used as the mask in the ICP Si etching. The etch depth of the rib-type waveguides was 2.2 µm. After the etch and resist removal, a 0.46 µm thick thermal oxide was grown to reduce the roughness of the waveguide sidewalls. The thermal oxide was removed with wet etching in HF acid before growing a cladding oxide layer. The 1 µm thick cladding oxide was deposited with the TEOS process. The lithography and the thermal oxidation changed the waveguide dimensions, so that the final waveguide thickness was 4.3 µm. Before the measurements, the test chips were diced and polished to optical quality.

The 4.5 cm long straight waveguides were measured using the Fabry-Perot method at the Fraunhofer Institute for Telecommunications, Heinrich-Hertz-Institute. During measurement the resonance effect was created by tuning the wavelength of a narrow band laser. The transmission spectrum of a measured waveguide is shown in Fig. 12. The propagation loss was determined by fitting it to the measured transmission spectrum. As a result, propagation loss of 0.35 dB/cm gave the best fit. Measurements from other waveguides with similar dimensions resulted in propagation loss of 0.25–0.35 dB/cm.

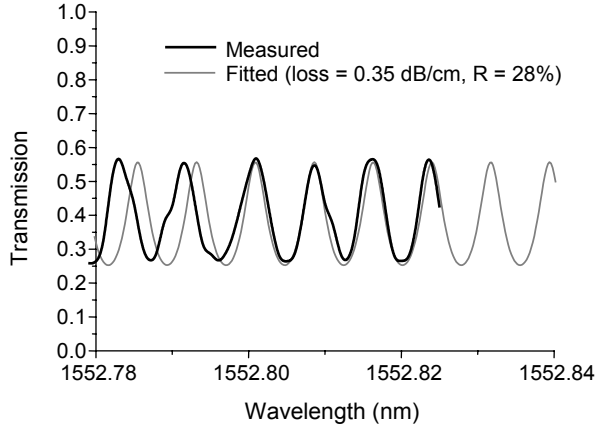

Fig. 12. Fabry-Perot propagation loss measurement of a 4.3 µm thick SOI waveguide.

In the fabrication of the 9 µm thick waveguides, a special test mask was used enabling accurate measurement of propagation loss using the simple insertion loss method (see Publication I). The test mask included 114 cm long waveguides of width 2–11 µm. Due to the extensive length of the waveguides, they were fitted to the 10 cm wafer by constructing them in a spiral form, as seen in Fig. 13. The construction, in which there were several waveguides travelling in parallel in the spiral, caused each waveguide to pass through 100 waveguide crossings. The bending radius of these waveguides was not fixed, but varied from 2.5 to 4.2 cm along the length of the waveguide. The waveguides were fabricated on a BESOI wafer with a 9 µm thick SOI and a 1 µm thick buried oxide layer. A 300 nm SiO_2 film was used beneath the resist as an additional hard mask. After mask patterning using lithography and dry oxide etching, ICP etching was applied to etch the rib waveguide structure in SOI. The etch depth was 5 µm, resulting in $h/H = 4/9$. After the Si etch, the resist residuals and the

oxide mask were removed. The final step in the waveguide fabrication was deposition of a 1 μm top cladding layer by wet thermal oxidation at 1050 °C. Before the measurements, the test chips were diced and polished to optical quality.

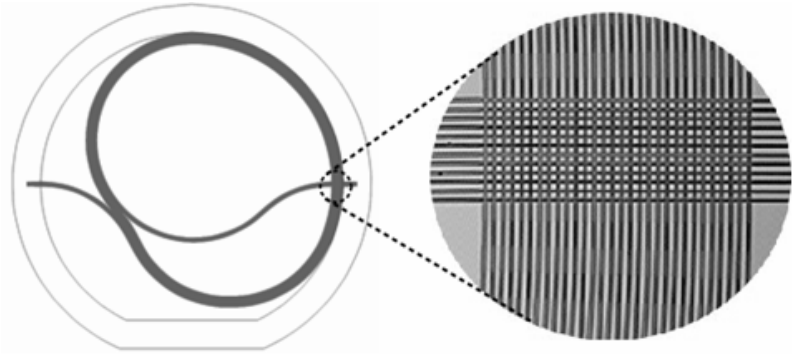

Fig. 13. Layout of spiral waveguide mask. The spiral includes several parallel waveguides. The microscope image shows the mask section where the waveguides cross. [Publication I.]

During measurement of the 9 μm thick SOI waveguides the propagation loss of the fundamental mode was determined. To avoid the influence of higher order modes, it had to be ensured that the waveguide under study had a single-moded behaviour. In rib-type straight waveguides the formula proposed by Soref et al. [26] can be used, which gives the waveguide dimensions that lead to single-moded operation:

$$\frac{W}{H} \leq 0.3 + \frac{h/H}{\sqrt{1-(h/H)^2}}. \tag{1}$$

The formula is applicable when $h/H \geq 0.5$. For the bent waveguides presented here, the Soref's formula cannot be directly applied. An immediate contradiction arises from the fact that h/H was made slightly less than 0.5 to minimise bending losses. With a slight deviation from Soref's condition, however, presumably the approximate single-mode limit could be estimated using Eq. 1. This assumption has also been verified with simulations [2, 44]. Another discrepancy arises from the fact that with a bent waveguide, the fundamental mode can be measured with dimensions that would cause the corresponding straight waveguide to be multi-

moded. With an appropriate bending radius, the bending losses in a curved waveguide can be very high for the weakly guided higher-order modes, while still very small for the fundamental mode. In that case the bent waveguide is in practice single-moded and the loss of the fundamental mode can be measured. All the results given below are for the fundamental mode.

The propagation loss was determined from the insertion loss measurement. In the measurement, index matching oil was used between the fiber and the waveguide to eliminate the effect of the air gap. The propagation loss was calculated by subtracting simulated reflection and modal coupling losses of the fiber-waveguide connections from the insertion loss, and dividing the remainder with the waveguide length. The minimum insertion loss of 18.6 dB including propagation, bending, crossing and fiber-coupling losses was measured at 1550 nm through a 6.7 μm wide SOI waveguide. The reflection loss due to the two fiber-waveguide facets was calculated as 1.4 dB. The modal coupling loss was defined by simulations with the TempSelene software. For the fiber a Gaussian field distribution with $1/e^2$ intensity radius of 5 μm was assumed. For the waveguide corresponding to the 18.6 dB insertion loss (H = 9 μm, h = 4 μm, W = 6.7 μm) the modal coupling loss due to two fiber couplings was simulated as 2.5 dB. The resulting propagation loss was 0.13 dB/cm.

The propagation loss results for one of the waveguide chips containing 114 cm long SOI waveguides are shown in Fig. 14 as a function of the waveguide width. After measuring several spiral waveguide chips and examining the propagation losses as a function of waveguide width, a pit-shaped behaviour similar to that of Fig. 14 was repeatedly observed. This behaviour is consistent with previous SOI waveguide loss studies [58–60]. With the narrowest waveguides the intensity distribution is closer to the waveguide walls, increasing the scattering losses. At the other end where the width increases, power leakage from the fundamental mode into the lossy higher-order modes is expected to increase.

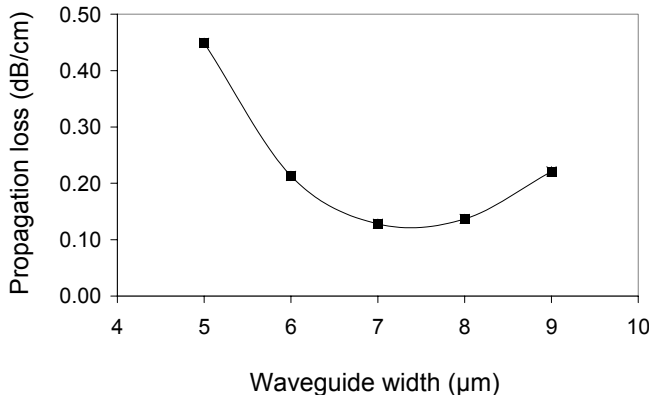

Fig. 14. Propagation loss measurement results for a bent 114 cm long rib waveguide on SOI. [Publication I.]

When Soref's formula is applied to the bent waveguides in Fig. 14, the width limit for single-mode operation is $W \leq 7.2$ μm. This limit was confirmed also with simulations for both straight and bent waveguides. The results suggest that propagation losses around 0.1 dB/cm can be achieved in single-mode straight waveguides with the current processing technology. This is the lowest propagation loss published so far in the literature for a dry etched SOI waveguide.

3.2 Antireflection coatings

The microphotonic chips are usually connected to the surrounding system (optical network, measurement setup etc.) using optical fibers. Due to the high refractive index difference between a silica fiber core (n = 1.47) and a silicon waveguide (n = 3.48), a total of 16% of the incoming light is reflected at each fiber-waveguide junction. If there is an air gap between the fiber and the waveguide, the reflectance is even higher. Two waveguide connections (without air gaps) produce reflection losses of 28% (1.4 dB), which has the same order of magnitude as the sum of all the other loss components present in a typical waveguide chip.

The reflection (or Fresnel) losses can be reduced or even eliminated by using an antireflection (AR) coating. The AR coating can be fabricated either at the end of the fiber or on the waveguide end facets. It can consist of one or several

layers. A multilayer AR coating can have a very low reflectance with relative broad thickness and material tolerances, over a wide spectral range. However, zero reflectance is also possible with a single layer at the desired wavelength, if the following conditions are fulfilled:

$$n_{AR} = \sqrt{n_1 n_2}\ , \tag{2}$$

$$t = \frac{\lambda}{4 n_{AR}}\ . \tag{3}$$

Here, n_{AR} is the refractive index of the antireflection coating, n_1 and n_2 are the refractive indices of the surrounding materials, t is the thickness of the antireflection coating, and λ is the target wavelength. In practice, it may be difficult to find suitable material that exactly fulfils Eq. 2. Furthermore, thickness control in layer deposition may be inaccurate, giving thickness away from Eq. 3. Fortunately, the reflections are suppressed satisfactorily for most applications, even if the properties of the actual coating differ from the above conditions. For the Si and SiO_2 interface, n_{AR} = 2.26 and t = 171 nm are the optimum refractive index and thickness of the single antireflection coating at 1550 nm wavelength.

In order to eliminate the reflection losses, several diced and polished waveguide chips were coated using atomic layer deposition. The ALD depositions were done in cooperation with the University of Helsinki and Helsinki University of Technology. Three materials were tested. At the University of Helsinki Ta_2O_5 and HfO_2 layers were prepared with ALD. At Helsinki University of Technology ZrO_2 layers were grown. The spectrophotometer described in Section 2.4 was used to measure the film thickness and refractive index of these layers. The setup did not allow for direct measurement of the waveguide end facets, therefore the measurements were carried out on ALD coated reference surfaces. Fig. 15 shows the measured reflectance spectra of a bare Si wafer and a Si wafer coated with Ta_2O_5. At 1550 nm, the reflectance is decreased from 30.5% of the bare Si to 2.4% for the Ta_2O_5 coated Si surface. From the Ta_2O_5 spectrum, a refractive index of 2.10 and film thickness of 170 nm can be determined. Being away from the ideal thickness of 185 nm given by Eq. 3, the wavelength of the minimum reflectance is shifted from the targeted 1550 nm to 1430 nm. The

deviation from the targeted value was not due to poor thickness control accuracy, but to lack of calibration in the deposition process. This can easily be fixed in future work. Among the investigated AR coating materials, the refractive index of ZrO_2 (n = 2.13) was closest to ideal. Unfortunately, the ALD process for ZrO_2 was unstable, giving a non-uniform and rough layer on the vertical sidewalls.

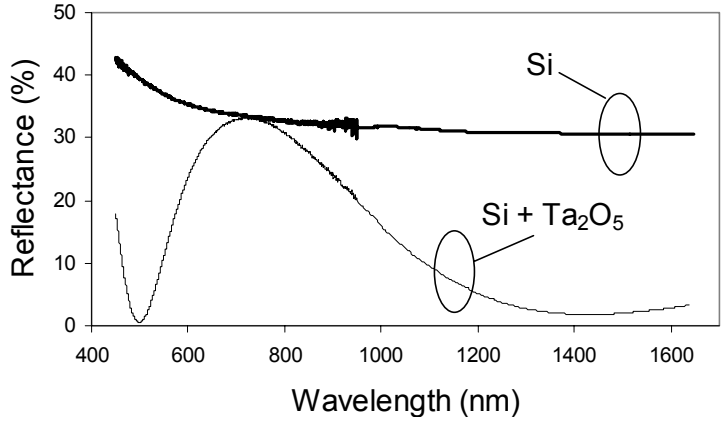

Fig. 15. Measured reflectance spectra of a silicon surface coated with 170 nm of Ta_2O_5. Measured reflectance of a bare Si surface is shown as a thick curve.

The impact of the antireflection coating on coupling losses was determined in insertion loss measurements, where the insertion loss of straight 4 cm long waveguides was measured before and after the antireflection coating deposition. The waveguides were 9 μm thick rib-type SOI waveguides with h/H = 4/9 and varying width. In the measurement, light was coupled to the waveguide with a SM fiber. The transmitted light was gathered with a multi-mode (MM) fiber. Index-matching oil (n ~1.5) was used to fill the air gaps between the fibers and the waveguide. As a result, the Ta_2O_5 coating decreased the losses significantly. On average, the loss reduction after the Ta_2O_5 AR coating deposition was measured as 1.6±0.3 dB. This value is close to the calculated value of 1.4 dB, which assumes a Ta_2O_5 antireflection coating 170 nm in thickness. The difference between the simulated and measured value is within the accuracy of the insertion loss measurement.

3.3 Adiabatic couplers

Optical couplers are used in microphotonic circuits when it is necessary to couple light between different waveguides. The first approach to realise these was the directional coupler. Unfortunately, this component was found to be sensitive to wavelength, fabrication tolerances, and the polarisation state of light. Over the past 10 years they have mostly been replaced with multi-mode interference (MMI) couplers, which have relaxed fabrication tolerances and sufficiently low polarisation dependency. However, MMI couplers still have a rather large wavelength dependency. To circumvent these limitations, adiabatic couplers have been developed and tested on $LiNbO_3$ [61], SiO_2 [8], and more recently on polymeric [62] waveguide materials. In adiabatic operation there is no energy change between different modes in the coupler structure. This principle distinguishes the adiabatic coupler from directional and MMI couplers, where the excitation of higher order modes is the main requirement for the operation. Unlike simple Y-junctions, adiabatic couplers can be used as passive 2×2 couplers and, thus, to construct e.g. active 2×2 switches. The main drawback of previous adiabatic coupler demonstrations has been that in order to avoid the excitation of higher order modes, the adiabatic couplers have been significantly longer than the equivalent directional couplers or MMI couplers. For that reason adiabatic couplers have not been widely used in integrated optics. In this study adiabatic couplers were, for the first time, fabricated and characterised in SOI.

The design of the adiabatic coupler was based on a simple waveguide cross-section analysis carried out with the TempSelene software. The principal outcome of the analysis was confirmation of the principle and some guidelines for the component dimensions. The performance of the designed component was then tested experimentally. To that end, adiabatic couplers with slightly different design parameters were fabricated and characterised. The layout of the best adiabatic coupler is shown in Fig. 16(a). In the component there are two waveguides (numbered as 1 and 2), which are gradually brought very close to each other and then separated. There are many different sections in the device (see Publication III for details), but the one in which the two waveguides are brought from a (edge-to-edge) distance of 3 μm to the minimum distance of 1 μm is the most critical. In this section the waveguides form a coupled waveguide system that enables the optical power splitting of the coupler.

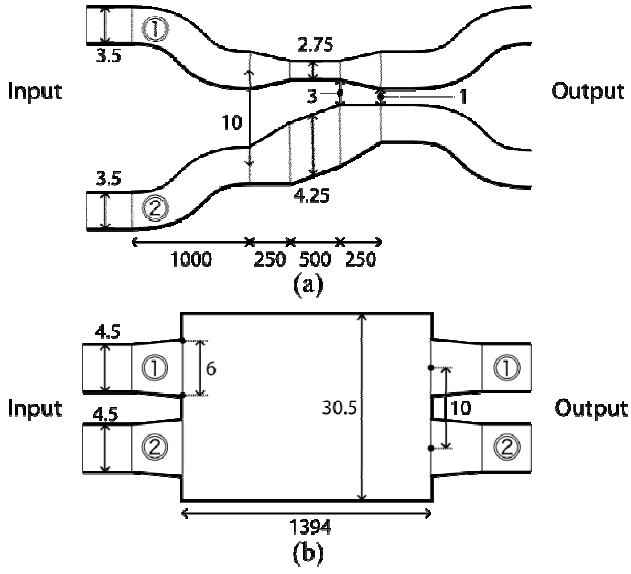

Fig. 16. Schematic view of (a) adiabatic coupler and (b) MMI coupler. The dimensions are in micrometres (not drawn to scale). [Publication III.]

In fully adiabatic operation the optical power from the input port of waveguide 2 excites the even system mode of the coupler and splits evenly into two output waveguides (with the same phase). Similarly, optical power from the input port of waveguide 1 excites the odd system mode and splits evenly into the output waveguides (with opposite phases). The splitting ratio is thus 50/50, which has led to the device being called as a 3 dB coupler. In order to enable easy and accurate characterisation of the couplers, a pair of these 3 dB couplers was cascaded to form a 2×2 Mach-Zehnder interferometer (MZI) device. The couplers were otherwise identical, but the latter was point-mirrored from the first one. Thus waveguide 1 was made thicker and waveguide 2 thinner in the latter coupling section. The MZI test device did not include any phase modulation structures, so that light coupled to input 1 was always transmitted to output 2, and vice versa. The high extinction ratio (ER) between the output powers of the two MZI outputs indicated that each coupler acted as a 3 dB coupler. Lower ER was an indication of unbalanced coupling caused by the residual excitation of higher order modes.

The performance of the adiabatic coupler was compared with the MMI coupler shown in Fig. 16(b). Both coupler types were optimised by characterising a set of devices with slightly varied layouts and by choosing the device that had the

best coupling characteristics. As with the adiabatic coupler, a pair of identical MMI couplers was used to form a 2×2 MZI structure, which made comparison of the devices easier. When comparing the two design layouts it can be seen that the MMI coupler design is actually somewhat longer than the equivalent adiabatic coupler.

Both coupler test structures were processed on the same wafer, which had 4 μm SOI thickness and a 1 μm BOX layer. The basic SOI waveguide fabrication described in Section 2.1 was used for the processing (see Publication III for details). The waveguide structure was rib-type with 2 μm etch depth. In the measurements, the excess optical losses, polarisation sensitivity, and spectral characteristics of the couplers were studied. To improve the measurement accuracy, the total insertion loss measured for a test device was compared with an equally long and wide reference waveguide. Thus the excess loss resulting from the MZI structures could be extracted without knowing the somewhat imprecise coupling losses.

For the adiabatic couplers the measured excess loss was about 0.2–0.6 dB per coupler for both polarisations. The ER of the MZI device based on the adiabatic couplers was about 15 dB for TE and almost 20 dB for TM. The excess loss per MMI coupler was measured as 0.2–1.0 dB for both polarisations. As with the adiabatic couplers, the variation in the results was due to the finite accuracy of the measurement setup. The ER of the MMI-based MZI was over 20 dB for TE and almost 30 dB for TM. This was clearly better than the adiabatic coupler based MZI. In order to improve the ER of the adiabatic coupler based device, the device geometry should be optimised to further suppress the residual excitation of the higher order modes.

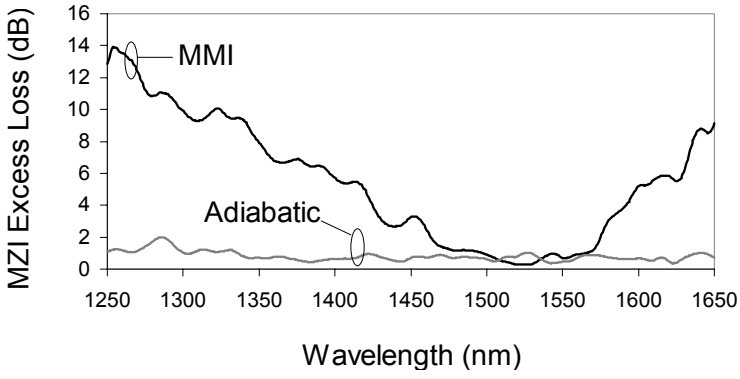

Fig. 17. Excess loss of 2×2 MZI devices based on adiabatic and MMI couplers. The spectra are measured from input port 1 to output port 2. [Publication III.]

The results of the spectral loss measurement are shown in Fig. 17. The MZI based on adiabatic couplers shows a very flat response with excess loss around 1 dB throughout the measured spectral range. The exception is the peak around 1290 nm, where the maximum loss of 2 dB was measured. The MMI-based MZI shows losses of about 1 dB in a spectral range of 1480–1570 nm. However, outside this low-loss region the losses increase rapidly. It was therefore shown that when a broad wavelength range is required, i.e. from 1300 to 1600 nm, low loss adiabatic couplers with acceptable extinction ratio can be realised on SOI. Furthermore, it was shown that using adiabatic couplers does not necessarily require a larger component size than MMI couplers with comparable characteristics.

3.4 Arrayed waveguide gratings

In optical telecommunications, multiple wavelength channels are often used to increase the capacity of an optical data transmission link. This is called wavelength division multiplexing (WDM) technology. Arrayed waveguide grating (AWG) is an important building block in a microphotonic WDM circuit, enabling the spatial combining (multiplexing) or separation (demultiplexing) of different wavelengths [63–65]. The device consists of two star couplers connected by an array of waveguides with a constant incremental path length difference. AWGs have previously been demonstrated using SOI, which was also the device platform used in this work [66–68].

In this work SOI-based AWGs were designed, fabricated, and characterised (see Publication IV). They were developed to merge wavelengths from several lasers into a common waveguide in a multi-wavelength transmitter unit. The design target was eight channels in the C-band (1530–1560 nm), which is the main operation wavelength window in optical telecommunications. The channel spacing was chosen to be 1.6 nm (~200 GHz) around the 1550 nm centre wavelength. For amplitude stabilisation the AWGs were integrated with variable optical attenuators. The VOAs were based on symmetrical Mach-Zehnder interferometer structures with 2 mm long and 15 μm wide heaters on top of the waveguides. For the MZI-VOAs 3 dB couplers are required and they were realised by 1x2 MMI couplers. The design of the component layout including both the AWGs and VOAs was carried out by the Fraunhofer Institute for Telecommunications, Heinrich-Hertz-Institute.

When considering the fabrication of AWGs, one of the main parameters influencing the performance of the device is the etch depth (H-h). This parameter is discussed here, while keeping the waveguide thickness H constant. When the etch depth in the rib-type SOI waveguide is increased and thereby the slab height h is decreased, the effective index contrast between the waveguide core and the slab increases. This enables a decrease in the bending loss. At the same time the cross-talk between adjacent waveguides is decreased.

The simulated effect of rib waveguide slab height on laser coupling loss is shown in Fig. 18. The simulation was carried out by Fraunhofer Institute for Telecommunications, Heinrich-Hertz-Institute, with the commercial beam propagation software "BeamPROP" from RSoft Design Group. In the simulation, the coupling loss between the laser output and a rib-type SOI waveguide was calculated while varying the slab height and laser far-field angle. The full width at half maximum (FWHM) of the far-field angle is one of the basic specifications of the laser chips. As can be seen from the figure, the variation of the slab height has no significant effect on the coupling loss at small laser far-field angles. However, at far-field angles higher than 20° the decrease in the slab height results in lower laser coupling loss.

These aspects encourage minimising the slab height. However, in order to maintain the SM operation it should not be decreased below Soref's limit $h/H = 0.5$. When decreasing the slab height, another limitation arises from the

increased propagation loss, which adds to the overall loss of the device. Based on these considerations the etch depth of the AWG test devices was targeted as close as possible to the condition $h/H = 0.5$.

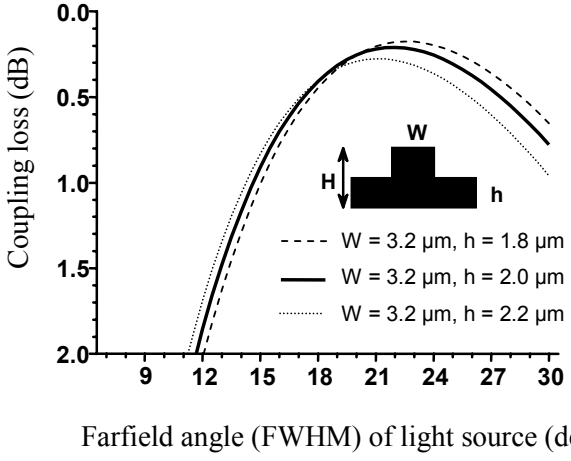

Fig. 18. Simulated laser-to-waveguide coupling loss for different values of slab height (h). The waveguide thickness was 4 µm.

The device structures were fabricated on an epitaxially thickened smart-cut SOI wafer with a 4.5 µm thick SOI layer and a 1 µm thick BOX layer. The waveguides were defined by standard photolithography and ICP Si etching with the continuous passivation process. No oxide hard mask was used in the fabrication. The etch depth was 2.2 µm. After etching, a 0.46 µm thick thermal oxide was grown to reduce the roughness of the waveguide sidewalls. During oxidation the thickness of the SOI layer decreased to 4.3 µm. The thermal oxide was removed with wet etching in buffered HF before growing a cladding oxide layer. The 1 µm thick cladding oxide was deposited with the TEOS process in the LPCVD furnace. For the VOA structures metal heaters based on molybdenum were realised on top of the waveguide structure. The Mo metallization process was described in detail in Section 2.1. After metallization, the fabricated test wafers were diced and the AWG chip facets were polished.

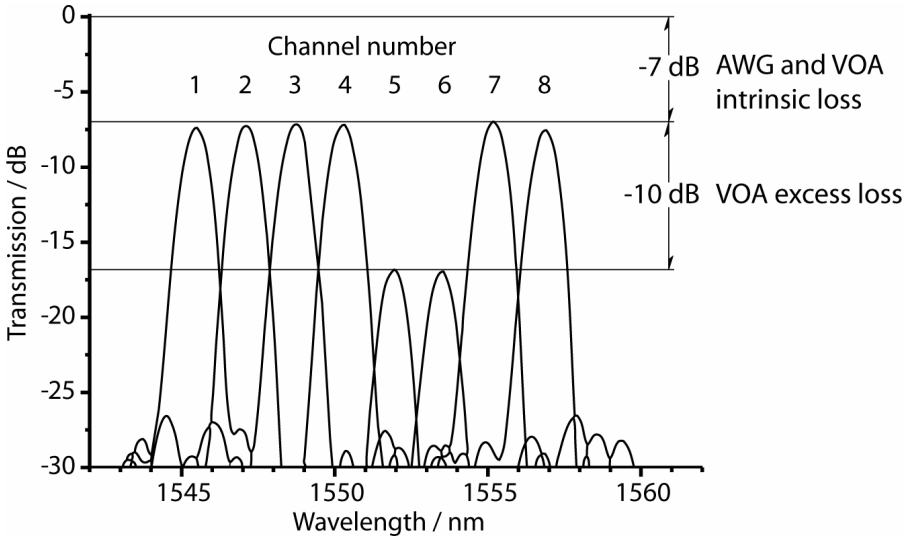

Fig. 19. Measured characteristics of an 8-channel 200 GHz AWG, each channel integrated with MZI-VOA. The VOAs for channels 5 and 6 are active.

The measured transmission spectrum of an 8-channel AWG with directly connected VOAs is shown in Fig. 19. The measurement was done by the Fraunhofer Institute for Telecommunications, Heinrich-Hertz-Institute. The optical loss of the combined device was 7 dB. A loss of 5.5 dB was measured for an identical AWG without the VOA. Thus the loss due to the VOA can be specified as 1.5 dB. In the figure, two channels are suppressed with the VOAs, resulting in attenuation of 10 dB for these channels.

3.5 Waveguide structures based on multi-step processing

The multi-step processing described in Section 2.2 was applied to different microphotonic waveguide components. It was used in the development of waveguide bends, mirrors, and converters (Publications II and V). These structures enable the miniaturisation of rib SOI waveguides. In addition, the converters can be used to connect waveguides of different sizes and types, enabling more flexibility in the design of microphotonic chips. The basic principles and theory of these components and structures are not new. However, few details about their fabrication and characterisation are found in the literature,

especially for SOI-based devices. Unlike in the fabrication processes proposed by others, no costly or complicated process steps such as epitaxial growth [69], grey-scale lithography [70], or e-beam lithography [71] were used here.

The first application example of multi-step processing is a waveguide bend. This is related to the main disadvantage of the rib waveguide structure, i.e. the required large bending radius. This was confirmed in the simulations carried out with the TempSelene software for SOI rib waveguides with various thicknesses. For example, if the acceptable loss is set to a relatively high value of 1 dB/90°, a bending radius above 20 mm has to be used for 10 μm thick waveguides. However, such a large bending radius may result in component size too large for practical applications. A bend size reduction can be achieved by reducing the waveguide dimensions, but at the same time the advantages of low fiber-coupling loss is lost. The multi-step processing principle can provide an elegant and a radical solution for reducing the size of a waveguide bend. By etching an additional groove on the outer edge of a bent rib waveguide, as seen in Fig. 20, one can increase its horizontal effective index contrast, which enables tighter bends [72–74].

In order to test the groove bend, a double-masking multi-step process (see Section 2.2) was applied to realise a rib waveguide structure with an additional etch step. The waveguide thickness was 10 μm and the etch defining the basic rib waveguide structure was 5.1 μm deep. The additional grooves in the measured test chip were through-etched to the BOX layer (unlike the partially etched groove in Fig. 20(b)). The additional grooves were designed to approach the bent waveguide from a distance, as seen in Fig. 20(c), so that the coupling losses between the straight and bent waveguide sections were minimised. The width of the groove was of the same order as the rib of the bent waveguide. Each bend test structure was composed of four successive 45° bends.

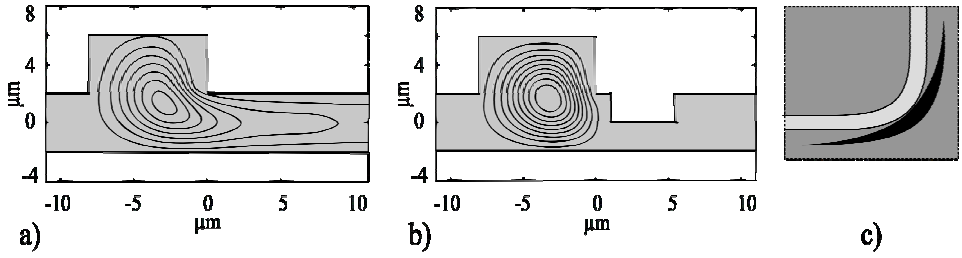

Fig. 20. Cross-sections and calculated intensity distributions of SOI waveguides with a bending radius of 10 mm (a) without and (b) with an additional groove. (c) Top view showing the positioning of the groove in a bent waveguide. [Publication II.]

Optical losses were measured from groove bend test structures with bending radii of 5 mm and 10 mm. For the 5 mm radius, the losses created in the bend were determined as 0.9 dB/90° and 0.7 dB/90° for the TE and TM polarisations, respectively. Thus, the groove enabled a significant decrease of the bending radius from over 20 mm to 5 mm with 10 µm thick SOI waveguides, if the 1 dB/90° bending loss limit is used. For comparison, a similar waveguide with 5 mm bending radius without the groove resulted in losses over 10 dB/90° for both polarisations. It is worth mentioning that similar results were achieved for the 5 and 10 mm bending radii. This suggests that the losses measured here for the groove bends were not dominated by the bending loss and that there was some other loss mechanism present. Since the double-masking process was used, the spiky Si residuals along the corner of the additional groove (see Fig. 7) probably caused excess scattering losses along the bend. It is expected that by fabricating the grooves with the sequential multi-step process, which enables smoother grooves, the bending losses and the bending radii can be further decreased.

Another application where the proposed multi-step process can be beneficial is a waveguide mirror, which changes the direction of the waveguide abruptly [75–76]. In this work the mirror facet was monolithically integrated with 10 µm thick SM rib waveguides. The main advantage of the rib-type waveguide mirror is that it occupies a very small footprint when added to a SM rib waveguide circuit. The waveguide mirror test structure fabricated and characterised in this study is illustrated in Fig. 21. The angle between the input and output waveguides was 90°. The multi-step processing enabled passive alignment of the lower etch step with the mirror facet. This was because the openings of the second mask were effective only when overlapping with the

openings of the first mask. Thus the alignment of the mirror with the input and output waveguides was not affected by the limited alignment resolution. Since the mirror facet was not formed during a single etch step, but two successive steps were used, it was crucial to avoid a discontinuity at the junction of the etch steps. This kind of discontinuity is typical to the sequential multi-step process due to the limited resolution of the second lithography. Thus the fabrication of the waveguide mirror was done with the double-masking process, achieving a uniform and smooth mirror facet. The upper Si etch step was 4.9 μm deep, while the lower etch step was performed through the remaining SOI layer. Each mirror test structure involved eight 90° mirrors. The best loss results for the 90° rib waveguide mirrors were measured as 0.6 dB/90° and 0.7 dB/90° for the TE and TM polarisation at 1550 nm, respectively. These results were of the same level as in the previous SOI waveguide mirror study, which was based on wet etching [76].

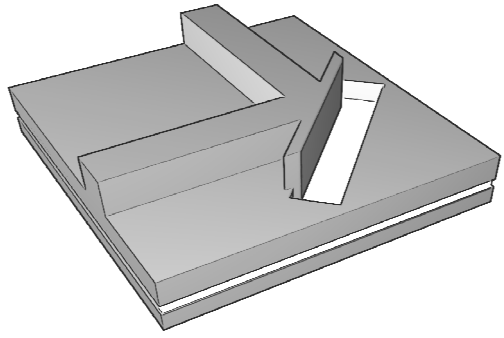

Fig. 21. SOI waveguide mirror with rib-type input and output waveguides.

The third application of multi-step processing is the adiabatic conversion between waveguides with cross-sections of different sizes and types. For example, a rib waveguide can be converted into a strip waveguide with the same or a different thickness. This can be used e.g. to realise compact waveguide arrays, tight bends, waveguide mirrors, or short multi-mode interference couplers [48]. Another useful element for microphotonics is a vertical taper, which adiabatically changes the thickness of a SM rib waveguide. It can be used e.g. in efficient light coupling between an optical fiber and a small-size microphotonic circuit.

Rib-strip converters and vertical tapers are schematically illustrated in Fig. 22. In the rib-strip converter shown in Fig. 22(a), the additional grooves beside the rib waveguide are spread until a strip waveguide is formed. In the vertical taper shown in Fig. 22(b), the thick rib waveguide is narrowed down until it vanishes. By then, the light is coupled from the thicker rib waveguide to the thinner rib waveguide. It should be noted that the converters and vertical tapers can be modified by tuning the depths of the two etch steps (without modifying mask layouts). In Fig. 22 the etch depths relative to the SOI layer thickness are approximately 50%+50% for the converter and 60%+20% for the vertical taper. However, by using e.g. 50%+25% etch steps for the converter, the conversion would appear between two rib waveguides with clearly different slab thicknesses and *h/H* ratios. Thus the converter can be considered as a structure for changing the horizontal confinement of a waveguide. Similarly, using e.g. 60%+40% etch steps for the vertical taper would provide a transformation between a thick rib waveguide and a thinner strip waveguide (instead of a thinner rib waveguide). Thus the vertical taper essentially changes the waveguide thickness.

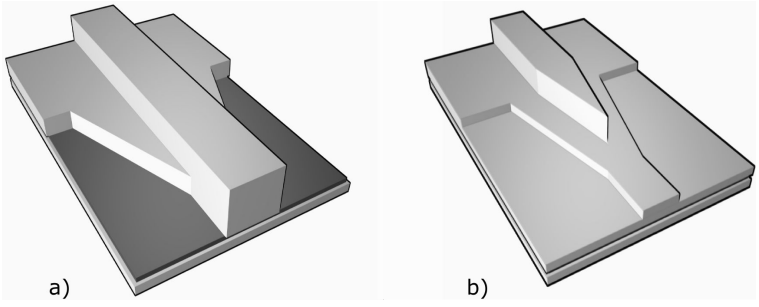

Fig. 22. Schematic illustration of (a) a rib-strip converter and (b) a vertical taper. [Publication II.]

The double-masking multi-step process was used for the fabrication of the rib-strip converters into 10 μm thick SOI waveguides. The upper etch step was 5 μm deep. This formed the basic rib structure for the input waveguides. The lower etch step reached through the remaining ~5 μm of the SOI layer, which defined the strip waveguide. To enable a high measurement accuracy, optical losses were measured through 22 successive converter elements. This means that a rib-strip conversion was followed by a strip-rib conversion, which was repeated in total of 11 times. The measurement accuracy for a single converter element was estimated as ±0.02 dB. The resulting excess losses for a single rib-strip converter

were 0.05±0.02 dB for TE and −0.01±0.02 dB for TM. The apparently negative loss for TM is due to the finite measurement accuracy. In conclusion, the excess loss and the polarisation dependent loss are both below 0.07 dB for a single rib-strip converter.

The vertical taper was fabricated with the sequential process, which ensured a low top surface roughness of the thinner waveguide. The upper etch was about 6 μm deep, defining a 10 μm thick rib waveguide. The thickness of the thinner waveguide was also defined by this etch step as 4 μm. The depth of the lower etch step was 2 μm. The taper section is illustrated in Fig. 23, where the width of the 10 μm thick waveguide is narrowed well below 1 μm. The tests mask had six successive vertical taper elements adjoined, so that the light was coupled from the 10 μm thick waveguide to the 4 μm waveguide and vice versa three times. The measurement accuracy for a single vertical taper was estimated to be better than ±0.1 dB. Based on the results, the excess loss of a single vertical taper was 0.7±0.1 dB, including the impact of the polarisation dependent loss.

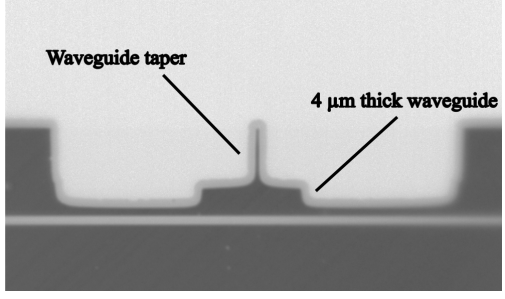

Fig. 23. Microscope image of a cross-section of a vertical taper. Both 4 μm and tapered 10 μm rib waveguides are visible. [Publication II.]

3.6 Er-doped Al_2O_3 waveguides on silicon

The fabrication of Er-doped Al_2O_3 waveguides based on atomic layer deposition was already described in Section 2.3 and the related characterisation methods in Section 2.4. Here, the main measurement results from one of the test chips with 3.9 cm long straight Er-doped waveguides are summarised (see Publication VI). These measurements include optical transmission, emission, fluorescence lifetime, and signal gain characteristics. The thickness of the rib-type Al_2O_3

waveguides was 2.0 μm, while the etch depth was 0.4 μm. The waveguide width was 6.0 μm in the transmission and gain measurements, and 2.8 μm in the fluorescence lifetime measurement.

Measured transmission spectra for both TE and TM polarisations of an Er-doped waveguide are shown in Fig. 24. The spectra show clearly the absorption due to the Er ions, the maximum being 6.1 dB/cm for TE and 6.4 dB/cm for TM at 1530 nm. The maximum absorption measured using non-polarised light (and a slightly different setup) was 6.2 dB/cm, which shows consistency with the previous results. The total waveguide losses resulting from the fiber coupling and scattering can be estimated from the transmission values around 1300 nm, where no Er-induced absorption occurs. In Fig. 24 the total waveguide losses are about 11 dB. According to the simulations, the fiber coupling losses due to the modal mismatch were 4.5 dB, which results in a propagation loss over 1.5 dB/cm. However, the total fiber coupling losses were probably higher than this. This assumption is supported by the fact that the waveguide end facets were cleaved, but not polished. Since wet etching does not increase the surface roughness of the waveguides considerably, another explanation for high propagation losses is scattering in the material.

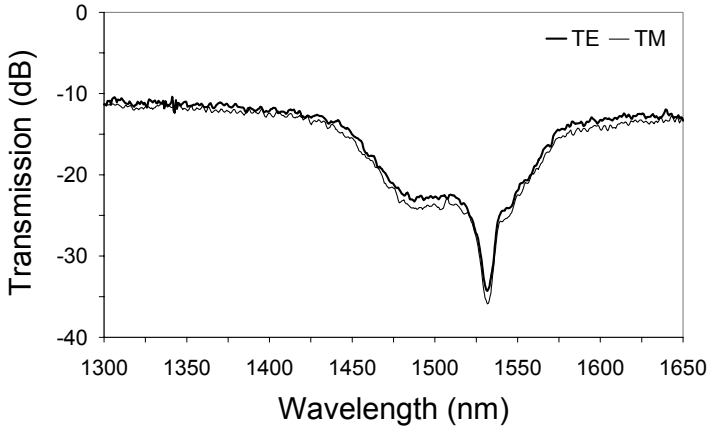

Fig. 24. Transmission spectrum of a 3.9 cm long Er-doped Al_2O_3 waveguide for TE and TM polarisations. [Publication VI.]

In the emission spectrum measured from the Er-doped Al_2O_3 waveguide, the highest peak was located at 1530 nm, followed by a broad emission shoulder from 1540 nm to 1560 nm. The full width at half maximum (FWHM) of the

emission spectrum was 52 nm. A broad emission spectrum is typical for Er-doped Al_2O_3 material, being broader than e.g. in Er-doped silica [77].

In the gain measurement the absorption of the signal light competed with the stimulated emission, and a net optical gain was not obtained. This indicated that the inversion of the Er ions was not sufficient. The poor inversion was verified in the fluorescence lifetime measurements, where a lifetime as low as 0.9 ms was measured. The short lifetime was most probably due to the inhomogeneous doping profile generated during ALD core deposition. The pure Er layers between the Al_2O_3 layers with a locally high volume density of the Er ions cause the doping profile to be inhomogeneous. This is expected to increase the cooperative upconversion, in which Er ions are spontaneously de-excited from the metastable energy state. This detrimental interaction is expected especially at high Er concentrations or when Er ions are clustered [78].

Despite the poor fluorescence lifetime of the Er ions, the signal at the output was clearly amplified in the gain measurement when the 980 nm pump light source was switched on. The ratio of the output signal with and without the pump power is commonly referred to as the signal enhancement. The signal enhancement at 1550 nm as a function of pump power is shown in Fig. 25. The pump power given in the figure indicates the optical power in the input fiber. The actual power in the waveguide was estimated to be 65% lower. As seen in the figure, the signal enhancement was saturated to a level of about 6 dB when the pump power was increased.

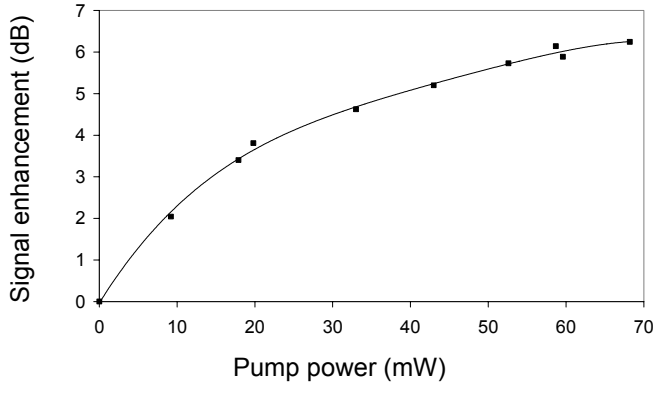

Fig. 25. Signal enhancement of an Er-doped waveguide as a function of the pump power at 1550 nm signal wavelength. [Publication VI.]

To achieve a net optical gain in these waveguides it is necessary to increase the fluorescence lifetime of the metastable state. This implies finding means to spread the Er doping profile from the current abrupt and periodic density caused by the ALD based fabrication method. Furthermore, the high total losses of the waveguide need to be decreased significantly. This can be done by optimising the waveguide dimensions to better match those of the optical fiber, and finding the origin of the high losses.

4 Conclusions

The aim of this study was to develop the fabrication processes of microphotonic waveguide components. More specific targets were e.g. propagation loss reduction in straight and bent silicon-on-insulator (SOI) waveguides, applying processing with more than one etch step, and applying atomic layer deposition in the waveguide fabrication. Therefore, the significance of the work lies more in the development of novel and improved fabrication concepts, and less in the invention of novel components. The main achievements were related to simplified processing or improved performance of previously known waveguide components.

The first part of the work was the development of the basic waveguide processing. A propagation loss as low as 0.13 dB/cm was measured at 1550 nm for a 114 cm long rib-type waveguide with a thickness of 9 μm. This is the lowest propagation loss of a dry-etched and single-mode SOI waveguide reported in the literature. The measured propagation loss of 0.25–0.35 dB/cm for a 4 μm thick waveguide is another demonstration of the low loss SOI waveguide.

Based on the basic SOI fabrication processes, some basic building blocks of photonic integrated circuits were then fabricated and characterised. These included adiabatic couplers and arrayed waveguide gratings (AWGs). The adiabatic couplers fabricated on SOI showed a very broad wavelength range from 1300 to 1600 nm with excess on-chip loss below 1 dB. The spectral range of this device was superior to that of the multi-mode interference coupler, which is commonly used today. The extinction of higher-order modes was not yet achieved complitely, but this can be improved by further optimising the device geometry. The SOI-based arrayed waveguide gratings integrated with variable optical attenuators showed very well-behaved optical filter characteristics. The overall insertion loss of the AWG was measured to be 5.5 dB, which was largely determined by the waveguide propagation loss of 0.35 dB/cm. In this case, the thickness of the rib-type waveguide was 4 μm. The optical cross-talk of the AWG was measured as 23 dB.

Traditional waveguide processing with only one mask level was developed further to include additional mask levels. The use of more than one mask in the microphotonic fabrication is not a novel approach, but during this work the related multi-step processing was studied extensively and this led to several successful device demonstrations. Two different fabrication concepts were proposed, and their applicability was tested with several different waveguide structures. As a result, an additional groove etched beside a bent 10 µm thick rib waveguide enabled a bend radius reduction from over 20 mm to 5 mm. A waveguide mirror exhibited optical losses below 1 dB/90°. The excess loss of a vertical taper between 10 and 4 µm thick rib waveguides was 0.7 dB. A converter between a rib and a strip waveguide showed a negligible optical loss below 0.07 dB.

Er-doped Al_2O_3 waveguides were fabricated on silicon substrates using the atomic layer deposition (ALD) method. In the waveguide applications ALD offers some significant benefits, such as accurate thickness control and superior thickness uniformity. The rib-type waveguides were processed on top of a silica buffer layer. The measured waveguides showed strong Er-induced absorption, the maximum being 6.2 dB/cm for non-polarised light, and a wide emission spectrum. In the measured 3.9 cm long Er-doped waveguide the net optical gain was not obtained due to the short fluorescence lifetime of the metastable state. However, a signal enhancement (the ratio of the output signal with and without the pump power) of about 6 dB was measured at 1550 nm wavelength. To reach a net optical gain, the doping process needs further development to realise a more uniform doping profile throughout the Er-doped active layer.

This work can be regarded as development of generic optical waveguide technology on silicon. As a result, detailed and practical knowledge, as well as experimental results from various demonstrations were obtained. They can be exploited e.g. in the realisation of compact silicon waveguide platforms. An example of such a platform is integration of compound semiconductor lasers on SOI waveguide chips. To successfully achieve this, the results from the multi-step processing, antireflection coatings, bending radius reduction, and various coupling schemes can be directly used.

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PUBLICATION I

Dry-etched silicon-on-insulator waveguides with low propagation and fiber-coupling losses

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Dry-Etched Silicon-on-Insulator Waveguides With Low Propagation and Fiber-Coupling Losses

Kimmo Solehmainen, Timo Aalto, James Dekker, Markku Kapulainen, Mikko Harjanne, Kaupo Kukli, Päivi Heimala, Kai Kolari, and Markku Leskelä

***Abstract*—Optical rib waveguides with various widths and heights were fabricated on silicon-on-insulator (SOI) substrates. Silicon etching was based on dry etching with inductively coupled plasma (ICP)-type reactive ion etcher. The etching process was developed to ensure low optical losses. Propagation loss of 0.13 ± 0.02 dB/cm was measured for the fundamental mode at the wavelength of 1550 nm in a curved 114-cm-long waveguide. The reflection losses were suppressed by applying atomic layer deposition (ALD) in the growth of antireflection coatings (ARCs).**

***Index Terms*—Atomic layer deposition (ALD), integrated optics, optical device fabrication, optical losses, optical waveguides, silicon-on-insulator (SOI) technology.**

I. Introduction

THE AIM of integrated optics technology is to realize a variety of different optical components on a single chip. As a consequence of the mature and widespread state of silicon-based technology, Si substrate has served as a base for many different waveguide material systems used in integrated optics. These include, e.g., silica [1], [2], germanium [3], silicon oxynitride [4], polymers [5], and silicon-on-insulator (SOI) [6]–[11]. Also III–V semiconductors have been structured on silicon [12]. One of the main advantages of SOI waveguides is the possibility for a size reduction of integrated optical structures. This results from the high refractive index of silicon, setting a high index contrast between the silicon core and the surrounding oxide cladding. Another strong motivation to study such structures has risen from the desire to monolithically integrate SOI-based optical components and control electronics.

The fabrication of single-mode SOI waveguides with low propagation losses (~ 0.1 dB/cm) has been demonstrated using a wet silicon-etching process [7]. The production of functional integrated optical components using wet etching is difficult due to the modest critical dimension control. Dry etching offers the required anisotropic etch profile and is therefore preferred in practical applications. However, achieving low-loss SOI waveguides with dry etching is not straightforward because of the surface roughness produced on the exposed sidewalls. The surface-roughness-induced scattering of light is the key factor determining the optical losses present in the SOI waveguide. In this work, a fabrication process based on dry silicon etching was developed to produce low-loss SOI waveguides. Waveguide test structures were designed to enable accurate determination of the optical loss.

The SiO_2/Si interface present at the fiber/waveguide connection reflects 16% of the incoming light intensity, if the possible airgap is ignored. Two waveguide connections produce reflection losses of 28% (1.45 dB), which has the same order of magnitude as the other loss components present in the waveguide. The reflection losses can be reduced with an antireflection coating (ARC). Typically, this is done by sputtering layers of suitable material on the end facets after the chip is diced and polished. Atomic layer deposition (ALD) is a promising technique for the realization of optical coatings [13]. In ALD, the film is grown in a sequential manner, which basically offers nanometer accuracy in thickness control. Since ALD offers an even growth regardless of the surface shape, it enables the preparation of high-quality optical coatings also on vertical sidewalls. Thus, ALD could be used for deposition of the ARC as a wafer-level-process step, instead of being a chip-level process. In this study, the feasibility of ALD in preparation of ARCs was tested by depositing tantalum pentoxide Ta_2O_5 films on polished waveguide-end facets.

II. Waveguide Fabrication

The formation of SOI waveguides is relatively simple compared to, e.g., silica-on-silicon technology, since growth of the active layer is avoided. The necessary processing steps include only the mask patterning, silicon etching, and cladding oxide deposition. In this study, a 300-nm SiO_2 film was used beneath the resist as an additional hard mask layer. The purpose of the SiO_2 mask was to ensure the protection of the patterned structures during the Si etching. The SiO_2 deposition was done with a low-temperature-oxide (LTO) process in a low-pressure chemical-vapor-deposition (LPCVD) furnace. Waveguide patterns were transferred to the oxide mask using standard photolithography and dry oxide etching in a parallel-plate plasma etcher. Silicon etching was done using an inductively coupled plasma (ICP)-type reactive ion etcher provided by Surface Technology Systems (STS). In order to minimize the surface roughness caused by the etching step, the etching process was modified from the STS advanced silicon etch (ASE) process [14]. In the ASE process, the sidewall passivation and

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K. Solehmainen, T. Aalto, J. Dekker, M. Kapulainen, M. Harjanne, P. Heimala, and K. Kolari are with the VTT Information Technology, Microelectronics, FIN-02044, Finland (e-mail: kimmo.solehmainen@vtt.fi; timo.aalto@vtt.fi; james.dekker@vtt.fi; markku.kapulainen@vtt.fi; mikko.harjanne@vtt.fi; paivi.heimala@vtt.fi; kai.kolari@vtt.fi).

K. Kukli and M. Leskelä are with the Laboratory of Inorganic Chemistry, Department of Chemistry, University of Helsinki, FIN-00014, Finland (e-mail: kaupo.kukli@helsinki.fi; markku.leskela@helsinki.fi).

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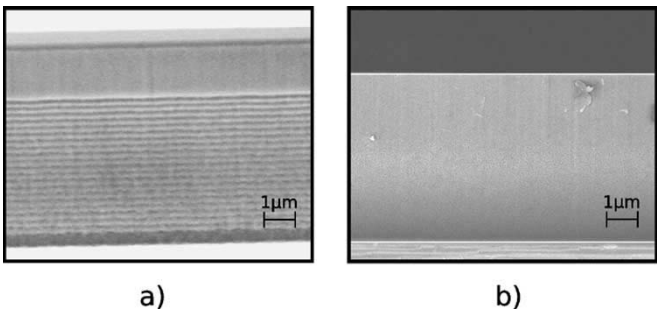

Fig. 1. SEM pictures of an etched waveguide sidewall fabricated with (a) standard ASE ICP etch process and (b) continuous-passivation ICP etch process.

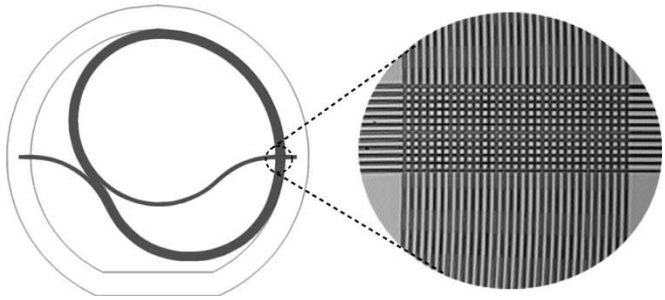

Fig. 2. Layout of the spiral waveguide mask showing a magnified microscope image of the mask section, where waveguide crossings take place. The spiral shown here includes several waveguides in parallel with different waveguide widths.

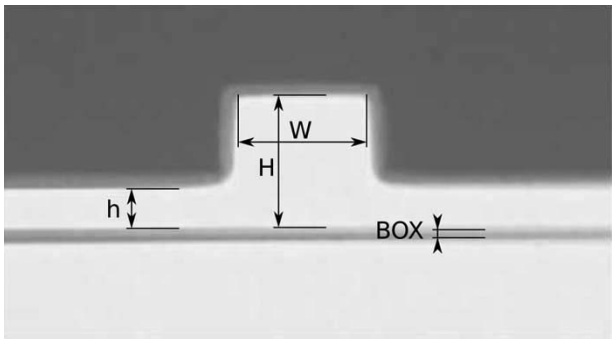

Fig. 3. Microscope photograph showing a cross section of the realized rib-waveguide structure.

silicon-etching steps are alternated subsequently. SF_6 and C_4H_8 are used as the etching and passivation gases, respectively. In this work, the passivation, which is necessary for anisotropic etching, was used continuously in the etching process. In continuous passivation, the flow rate of the passivating gas is linearly increased from its initial value as the etching deepens. The C_4F_8 flow rate was initially 120 sccm and was increased 2 sccm/min, while the SF_6 flow rate was kept constant at 40 sccm. The chamber pressure was 12 mtorr. The RF generator was operated at 13.56-MHz frequency. The power connected to the coil was constant at 600 W, while the power connected to the platen was initially 30 W and was then decreased at a rate of 1 W/min. The Si etch rate in ICP etching was 440 nm/min. The etch-depth variation over the wafer was measured with a profilometer as $\pm 7\%$. The etch selectivity against the AZ5214 resist was measured as 8:1, while the selectivity against SiO_2 was 13:1. The selectivities were significantly lower than in the typical ASE process because of the continuous passivation. In terms of surface roughness, the advantage of the continuous-passivation etch process over the standard ASE process can be seen in Fig. 1. The figure shows scanning-electron-microscope (SEM) images of the waveguide sidewalls etched with both processes. The alternating etching and passivation steps of the ASE process result in an undulated sidewall, as shown in Fig. 1(a). In principle, this undulation does not change the waveguide cross section along the direction of light propagation. However, the degree of random surface roughness of the ASE process is higher than in the continuous-passivation process shown in Fig. 1(b). After the silicon etching, the resist residuals and the oxide mask were removed with oxygen plasma stripping and wet chemical etching, respectively. The final step in the waveguide fabrication was the deposition of a 1-μm top-cladding oxide layer by wet thermal oxidation at 1050 °C.

The test structures in the mask included 114-cm-long waveguides with various widths. The long waveguides were fitted to the 10-cm wafer by constructing them in a spiral form, as seen in Fig. 2. As there were several waveguides traveling in parallel in the spiral, each waveguide passed through 100 waveguide crossings. The bending radius of these waveguides was not fixed, it varied from 2.5 to 4.2 cm along the length of the waveguide. In addition to the long curved waveguides, there were also 4-cm-long straight waveguides in the mask. They were used for studying antireflective coatings on waveguide-end facets. The waveguide geometry was of rib type (Fig. 3), which can confine large optical modes without sacrificing single-mode operation [11]. The waveguide core defined by the rib has thickness H and width W. The thickness of the slab surrounding the rib is h. The buried oxide layer (BOX) in the SOI wafers used was 1–3-μm thick. Three different SOI layer thicknesses were tested as a substrate, resulting in different waveguide thicknesses. A bond and etch-back SOI (BESOI) wafer yielded $H = 9$ μm (BOX $= 1$ μm). SOI layers of $H = 5$ μm (BOX $= 3$ μm) and $H = 2$ μm (BOX $= 3$ μm) were formed by epitaxially growing silicon on initially 1-μm thick smart-cut SOI wafers. The SOI thickness variation was measured to be ± 0.5 μm for BESOI wafers and ± 0.05 μm for the epitaxially thickened smart-cut wafers. The resistivity of the SOI layers was 1500–3500 Ωcm. For the waveguides studied here, such a high resistivity results in negligible absorption losses compared to the scattering losses. The etch depth H-h was varied in different samples, so that the ratio h/H varied between 0.5 and 0.4. The waveguide width in the mask varied between 2 and 11 μm. The lithography process and the thermal oxidation change the waveguide dimensions from the nominal values. The dimensions given in the text below are actual dimensions after the processing, verified with an optical microscope.

III. Propagation-Loss Measurements

Soref *et al.* [11] have proposed a formula for the waveguide dimensions that lead to single-mode operation in rib-type

straight waveguides:

$$\frac{W}{H} \leq 0.3 + \frac{\frac{h}{H}}{\sqrt{1-\left(\frac{h}{H}\right)^2}}. \quad (1)$$

The formula is applicable when $h/H \geq 0.5$. For the curved waveguides presented here, Soref's formula cannot be directly applied. An immediate contradiction comes from the fact that h/H was often made slightly less than 0.5 in order to minimize the bending losses. With such a slight deviation from Soref's condition, however, it is expected that one could estimate the approximate single-mode limit using the formula. This assumption has also been verified with simulations [6], [15]. Another discrepancy comes from the fact that in a curved waveguide, single-mode operation can be achieved with dimensions that would cause the corresponding straight waveguide to be multimoded. With an appropriate bending radius, the bending losses in a curved waveguide can be very high for the weakly guided higher order modes, while still very small for the fundamental mode. In that case, the curved waveguide is, in practice, single-moded, and the loss of the fundamental mode can be measured. In this study, the single-mode/multimode behavior was determined experimentally by monitoring the output of the waveguide with an IR camera while moving the input fiber in the vicinity of the waveguide input. With a waveguide showing single-mode behavior, the movement away from the optimal input-fiber alignment generates symmetrical intensity attenuation at the output, while the shape of the output intensity distribution is not changed. However, in the case of a multimode waveguide, such an input change results in variations in the output intensity distribution, which can be detected with the camera.

For the propagation-loss measurements, the waveguide ends were diced and polished to optical quality. In the measurement, unpolarized light from a broadband light source was coupled into the waveguide with a single-mode fiber. Transmitted light was coupled into another single-mode fiber and guided to an optical power meter. By replacing the power meter with an optical spectrum analyzer, the transmission spectrum could be measured. A fiber-to-fiber reference transmission was measured by directly butt coupling the input and output fibers. The propagation-loss results for one of the waveguide chips containing 114-cm-long curved SOI waveguides are shown in Fig. 4. The dimensions of these waveguides were $H = 9$ μm and $h = 4$ μm. A minimum insertion loss of 18.6 dB including propagation, bending, crossing, and fiber-coupling losses was measured at 1550 nm through a 6.7-μm-wide waveguide. The propagation losses were determined by subtracting calculated reflection and modal coupling losses of the fiber-waveguide connections from the insertion loss and dividing the remainder with the waveguide length. The reflection loss due to the two fiber-waveguide facets was calculated as 1.4 dB. Index-matching oil was used to eliminate the effect of the airgap. The modal coupling loss between the fiber and the waveguide depends on the waveguide geometry. The modal losses were defined by simulations with the commercial TempSelene software (version 4.3.04) from C2V, which calculates both the modal fields and the overlap integrals between them. For the fiber, a Gaussian field distribution with $1/e$ field radius of 5 μm was assumed. For the waveguide corresponding to the 18.6-dB insertion loss ($W = 6.7$ μm), the modal coupling loss due to two fiber couplings was simulated as 2.5 dB, yielding the propagation loss of 0.13 dB/cm. The length of the waveguides enabled accurate determination of the propagation loss, since coupling losses, which are typically difficult to estimate accurately, had only a small contribution to the result. Furthermore, the quality of the edge polishing had little effect on the results. The error in the loss measurement was estimated as $\pm$0.02 dB/cm, which is significantly more accurate than $\pm$0.3–0.5 dB/cm, typical to previous studies of SOI waveguide propagation loss [7]–[9]. As other loss components, such as misalignment loss, bending loss, and losses due to the waveguide crossings are neglected, this propagation-loss figure can be taken as a worst case approximation. The measured losses correspond to the fundamental mode only, as higher order modes had very high radiation losses along the curved waveguide. The disappearance of the higher order modes at the waveguide output was confirmed with the IR camera. After measuring several spiral waveguide chips and examining the propagation losses as a function of waveguide width, a pit-shape behavior similar to that of Fig. 4 was noticed. This behavior is consistent with previous SOI waveguide-loss studies [8]–[10]. With narrower waveguides, the intensity distribution is closer to the waveguide walls, increasing the scattering losses. As the width increases, it is expected that power leakage from the fundamental mode into the lossy higher order modes will be increased. If Soref's formula were to applied to the curved wavegu ides in Fig. 4, the width limit for single-mode operation would be $W \leq 7.2$ μm. This limit was confirmed with simulations for both straight and bent waveguides [6], [15]. The results suggest that propagation losses around 0.1 dB/cm can be achieved in single-mode straight waveguides with the current processing technology. This is the lowest propagation loss published so far in the literature for a dry-etched SOI waveguide.

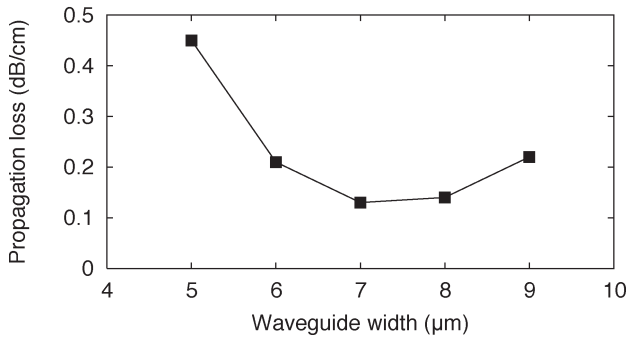

Fig. 4. Results of the propagation-loss measurements for a 114-cm-long curved SOI rib waveguide.

The propagation-loss spectrum was measured in the wavelength range of 1150–1650 nm for three waveguides with different thicknesses. The dimensions of these waveguides are shown in Table I. Because of higher losses, the measurements had to be performed on 7-cm-long straight waveguides for the waveguides with $H = 5.0$ and 2.0 μm. The results are shown in Fig. 5. As seen in the figure, the propagation loss increases

TABLE I
DIMENSIONS OF THE WAVEGUIDES USED IN THE PROPAGATION-LOSS MEASUREMENT

H (μm)	h (μm)	W (μm)	Length (cm)
9.0	4.0	6.7	114
5.0	2.5	4.4	7
2.0	1.0	3.6	7

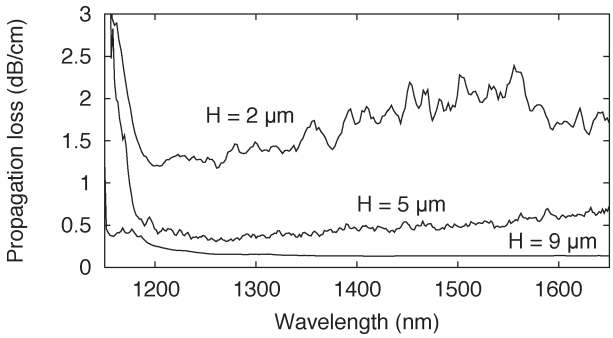

Fig. 5. Measured transmission spectra for SOI waveguides with various waveguide heights.

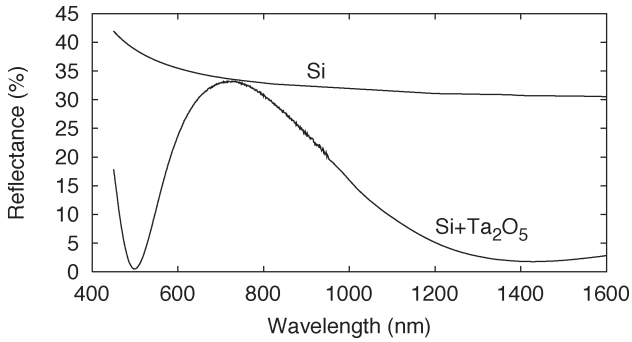

Fig. 6. Measured reflectance spectrum of an Si surface and an Si surface covered with 170 nm of Ta_2O_5.

TABLE II
MEASURED REFRACTIVE INDEX OF Ta_2O_5 GROWN WITH ALD

Wavelength (nm)	Refractive index
633	2.15
830	2.12
1300	2.11
1550	2.10

significantly as the waveguide thickness is decreased. This is a result of increased sensitivity to surface roughness with smaller waveguide dimensions. The fabrication process was optimized only for approximately 10-μm-thick SOI waveguides. Therefore, the propagation losses of thinner SOI waveguides are expected to decrease by further process optimization. As the waveguide dimensions decrease, spectra are also prone to distortions. The periodic fluctuations are probably due to interruptions in the waveguide structure originating from the fabrication process. As expected, below 1200 nm, the material absorption of Si increases the optical losses rapidly, making the material opaque. As long as the propagation losses caused by the waveguide structure are kept low, the Si material itself allows the use of a wide wavelength range from approximately 1.3 to 4 μm [16].

IV. ANTIREFLECTION COATING (ARC)

One of the main issues in any integrated optical-waveguide technology is the connection between the waveguide and an optical fiber, resulting in reflection, modal coupling, and fiber misalignment losses. In order to eliminate the reflection losses at the interface between the Si waveguide and an optical fiber, Ta_2O_5 ARCs were deposited with ALD on the waveguide-end facets. Ta_2O_5 was chosen as the antireflection material because it is transparent at the wavelengths of interest and its refractive index is known to be close to the optimum, which is 2.26 for the SiO_2/Si interface. The ALD apparatus used here was not designed for the wafer-level processing. Therefore, the deposition was done on the waveguide chips after polishing the chip facets. Amorphous Ta_2O_5 coatings were deposited at a temperature of 300 °C from $Ta(OC_2H_5)_5$ and H_2O [17] using 6500 growth cycles. A FilmTek 4000 fiber-optic-based spectrophotometer from Scientific Computing International was used to measure the film thickness and the refractive index of these layers. The setup did not allow the direct measurement of the waveguide-end facets. Therefore, the measurements were carried out on a reference surface. Fig. 6 shows the measured reflectance spectra of a blank Si substrate and Si substrate coated with Ta_2O_5. A thickness of 170 nm was solved from the reflectance spectrum for the Ta_2O_5 film. Measured refractive indexes for ALD-grown Ta_2O_5 at discrete wavelengths are given in Table II. Being away from the ideal thickness of 185 nm, the wavelength of minimum reflectance is shifted from the targeted 1550 nm to 1430 nm. The deviation from the targeted value was not due to thickness-control accuracy. Instead, it was a result of lack of calibration in the deposition process, a deprivation that can easily be eliminated in the future work. Despite the fact that the thickness was not ideal, the reflectance at 1550 nm was decreased from 30.5% of bare Si to 2.4% for Ta_2O_5-coated Si surface. The measurement shown was for air/Si and air/ARC/Si structures. The calculations showed that a 170-nm-thick layer of ALD-grown Ta_2O_5 reduces the reflection losses due to two fiber connections from 1.45 to 0.07 dB.

The impact of the ARC on the coupling losses was determined in the loss measurements. The insertion losses of straight 4-cm-long waveguides were measured before and after the ARC deposition. In the measurement, light was coupled into the waveguide with a single-mode fiber. The transmitted light was gathered with a multimode fiber. Index-matching oil was used to fill the air gaps between the fibers and the waveguide. The Ta_2O_5 coating decreased the losses significantly. On the average, the loss reduction after the Ta_2O_5 ARC deposition was measured as 1.6 ± 0.3 dB. This value is substantially close to the calculated value of 1.4 dB, which assumes a Ta_2O_5 ARC 170 nm in thickness. The difference between the simulated and measured value is within the accuracy of the insertion-loss measurement.

V. Conclusion

The fabrication of low-loss dry-etched silicon-on-insulator (SOI) rib waveguides was described. Propagation loss of 0.13 ± 0.02 dB/cm was measured at 1550 nm for a 114-cm-long curved waveguide. The measurement accuracy was exceptionally good. This is the lowest value reported in the literature for a dry-etching-based SOI waveguide and among the lowest reported in SOI material. Spectral measurements showed that the losses remained below 0.2 dB/cm from 1230 to 1750 nm. Reflection losses of 1.4 dB present at the waveguide/fiber interface were eliminated by growing Ta_2O_5 antireflection coatings (ARCs) on waveguide-end facets with atomic layer deposition (ALD).

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Kimmo Solehmainen received the M.Sc. Tech. degree, major in microelectronics, from Helsinki University of Technology, Finland, in 2000. He is currently pursuing the doctorate degree focusing on the subject of fabrication technology for integrated optics.

He has worked at VTT, Helsinki since 2001. His interests include microelectronics fabrication methods, optical device characterization, and spectrophotometric measurement techniques.

Timo Aalto received the M.Sc. Tech. and D.Sc. Tech. degrees in optoelectronics from Helsinki University of Technology, Finland, in 1998 and 2004, respectively.

He has worked at VTT, Helsinki, since 1997. His research interests are the design, simulation, fabrication, and characterization of silicon-based waveguides, especially silicon-on-insulator (SOI) waveguides.

James Dekker received the B.Sc. degree in Mechanical Engineering and the Ph.D. degree in materials science from the University of California at Davis in 1990 and 1997, respectively.

From 1997 to 1999, he held a postdoctoral position at Tampere University of Technology, Tampere, Finland, where he characterized defects in epitaxial III–V alloys. From 1999 to 2001, he worked at Helsinki University of Technology, characterizing defects in semiconductors and insulators. Since then, he has been at VTT, Helsinki, where he develops fabrication processes for microelectromechanical-system (MEMS) devices.

Markku Kapulainen received the M.Sc. Tech. degree in physics from Helsinki University of Technology, Finland, in 2001.

Since 2001, he has worked at VTT, Helsinki, as a Research Scientist. His interests include optical measurement techniques, fiber optics, and free-space optics.

Mikko Harjanne received the M.Sc. Tech. degree in optoelectronics from Helsinki University of Technology, Finland, in 2003.

Since his graduation, he worked at the Optoelectronics Laboratory of Helsinki University of Technology. He joined VTT, Helsinki, in 2005.

Kaupo Kukli received the Ph.D. degree from the University of Tartu, Tartu, Estonia, in 1999.

From 1996 to 1997, he was a Researcher at Helsinki University of Technology, Helsinki, Finland. Since 1998, he has worked as a Researcher both at the University of Helsinki and at the University of Tartu.

Päivi Heimala received the M.Sc. and Lic.Ph. degrees in physics from the University of Helsinki, Finland, in 1990 and 1993, respectively.

She is currently the Group Manager of the Photonics Group at VTT, Helsinki.

Kai Kolari received the M.Sc. degree in physics from the University of Helsinki, Finland, in 1999.

From 1999 to 2000, he was with Fortum Oyj, where he developed solar cell technology. He currently works as a Research Scientist at VTT, Helsinki, where his main interest is biomicrofluidics.

Markku Leskelä received the D.Sc. Tech. degree in 1980 from Helsinki University of Technology, Finland.

During 1980–1986, he worked as an Associate Professor at the University of Oulu, Finland, and during 1986–1990, as a Professor at the University of Turku, Finland. Since 1990, he has held the present position of Professor of Inorganic Chemistry at the University of Helsinki, Finland.

PUBLICATION II

Development of multi-step processing in silicon-on-insulator for optical waveguide applications

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Development of multi-step processing in silicon-on-insulator for optical waveguide applications

K Solehmainen, T Aalto, J Dekker, M Kapulainen, M Harjanne and P Heimala

VTT Information Technology, Microelectronics, PO Box 1208, FIN-02044 VTT, Finland

E-mail: kimmo.solehmainen@vtt.fi

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Abstract
Multi-step processing for a silicon-on-insulator (SOI) platform was developed. It allows the incorporation of additional grooves and steps into the basic optical waveguide structures, so that light can be adiabatically coupled between waveguides with different cross-sections. The processes were based on simple fabrication methods easily scalable for mass production. Two options for the fabrication sequence were tested, both having one silicon etch step with an oxide mask and another etch step with a resist mask. The applicability of the developed processes was tested with different waveguide structures. An additional groove etched beside a bent 10 μm thick rib waveguide suppressed the bend losses to below 1 dB/90° with a 5 mm bending radius. A waveguide mirror exhibited optical losses below 1 dB/90°. The excess losses of a vertical taper between 10 and 4 μm thick rib waveguides were 0.7 dB. A converter between a rib and a strip waveguide showed negligible losses, below 0.07 dB.

Keywords: integrated optics, optical device fabrication, optical losses, optical waveguides, silicon-on-insulator technology

1. Introduction

Based on the recent advances achieved in silicon-based photonics [1–5], it is now seen that silicon might well become the dominant material for photonics, as it has been for electronics since the early seventies. The ability to integrate both electronic and photonic circuits on a single silicon chip provides unique advantages and possibilities that cannot be reached with any other technology, at least for a competitive price. In silicon microphotonics, silicon can be used not only as a substrate, but also as a waveguide core material. Silicon-on-insulator (SOI) offers the most convenient platform for realizing silicon waveguides. SOI substrates allow monolithic and hybrid integration of different electronic and photonic functions. The very high index contrast in SOI waveguides allows the extreme miniaturization of optical devices by means of e.g. photonic nanowires or photonic crystal waveguides. This creates the potential for a significant increase in the density and integration of optical devices, which is a necessity for the increased performance and lower cost required for future microphotonic circuits.

The operation of the microphotonic components usually requires a single-mode (SM) behaviour. Other basic requirements are a small footprint enabling low cost, and a low-loss connection to the optical fibres, which couple the light into and out of the chip. Unfortunately, these requirements often conflict. For example, thick Si rib waveguides offer SM operation and a low-loss connection to standard optical fibres. However, they usually require very long bending radii, which results in large components. Thus, it is important to develop techniques for bend size reduction in thick Si waveguides. Significantly smaller bending radii are achieved with thinner waveguides, but then the coupling to standard SM fibres becomes inefficient. Here, a convenient solution is an on-chip coupler between a thick and a thin waveguide [6, 7]. More generally, it would be useful to combine different

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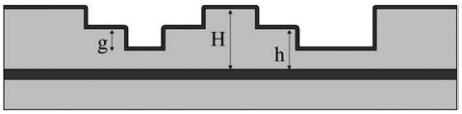

Figure 1. Multi-step structure in silicon. The SOI layer is patterned with two separate etching steps and covered with a cladding oxide layer.

waveguide cross-sections, each optimized for a given purpose, within a single silicon waveguide device. This can be achieved by using more than one etch step (and mask) in the fabrication process. The resulting multi-step structures can provide adiabatic conversions between different waveguide cross-sections.

In this study, multi-step processing in SOI was demonstrated using standard microelectronic fabrication methods. The target of the processes was the multi-step structure shown in figure 1. By changing the depths of the etch steps (H–h and g), various waveguide types and optical structures could be monolithically integrated on a single chip. The concept has been proposed before [8], but here the experimental work related to the fabrication and optical characterization of the multi-step structures is presented. Unlike in the processes proposed by others, no costly or complicated process steps such as epitaxial growth [6], grey-scale lithography [7] or e-beam lithography [9] were used. The processes reported here were based on two mask layers and two silicon dry etch steps. A contact mask aligner was used for lithographic exposures, ensuring fast and economical lithography. The applicability of the developed multi-step processing was tested with different waveguide structures. Additional grooves enabling a bend size reduction as proposed in [10] were realized in 10 μm thick rib waveguides. A waveguide mirror [11, 12] coupled to 10 μm thick rib waveguides was fabricated. Finally, two types of low-loss converters between different waveguides were fabricated and characterized. The first was a vertical taper [13–15] coupling rib waveguides with 10 and 4 μm thicknesses. The other was a rib–strip converter coupling waveguides of different types, as proposed in e.g. [8, 16].

2. Fabrication and characterization

The base for the fabrication was a 10 cm diameter BESOI (bond and etch-back SOI) wafer. The SOI layer and the buried oxide (BOX) were 9.5 ± 0.5 μm and 1.00 ± 0.01 μm thick, respectively. On top of the SOI layer a 1 μm oxide layer was deposited with a TEOS (tetra-ethyl-ortho-silicate) process in a low-pressure chemical vapour deposition (LPCVD) furnace. For the multi-step processing presented here, two photolithography masks were required. The first mask defined the upper step of the structure (H–h) and it was used to realize the basic waveguide structure. The default waveguide structure used for e.g. the input and output coupling was a 10 μm thick rib waveguide. The dimensions of the waveguides were chosen so that the SM condition was maintained [17]. The etch depth H–h and waveguide width varied slightly in different samples, but for the default rib waveguides dimensions with ratio $h/H \sim 0.5$ and waveguide

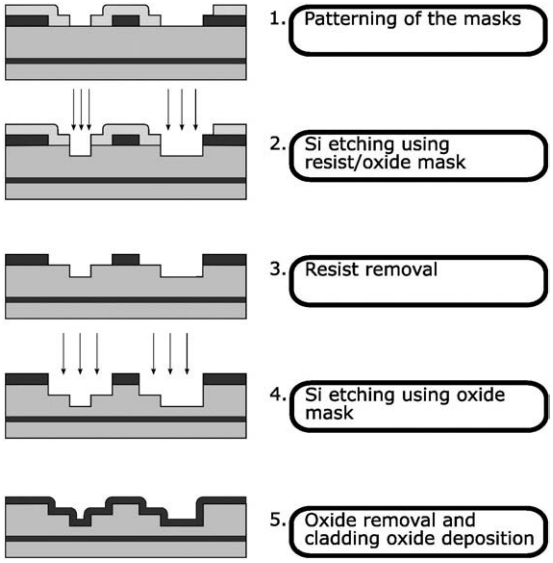

Figure 2. Double-masking multi-step process.

width of ~9 μm were used. The second mask defined the lower etch step, marked with the letter g in figure 1. It was used in realizing additional grooves for waveguide bends, mirrors, and optical mode-converters. The openings of the second mask were effective only when they overlapped with the openings of the first mask. This enabled the passive alignment of the two masks, which alleviated the effect of the limited alignment accuracy (± 1 μm) of the contact mask aligner. This feature of the multi-step process was especially useful in the realization of waveguide mirrors, where a deep vertical facet composed of two separate etch steps was realized. Two different process sequences, which could be used to fabricate the structure in figure 1, are described below.

2.1. Double-masking process

The first option was to use the *double-masking process* shown in figure 2. The essence of this process was to first pattern both mask layers and then etch the structures into silicon. The advantage of this approach was that the difficult lithography after a deep silicon etching was avoided. The upper etch step was defined first by patterning a 1 μm TEOS oxide layer with standard photolithography and dry oxide etching in a parallel plate plasma etcher. The patterned oxide was not used as an etch mask for silicon at this point, but a new photoresist layer was applied. This resist layer defined the lower step (g) and was used in the first Si etching step. Silicon etching was done using an inductively coupled plasma (ICP) type reactive ion etcher made by Surface Technology Systems (STS). The etching recipe was specially designed for low-loss optical waveguide applications [18]. After the etching, the resist was removed and the second etching step used the oxide layer as the etch mask, defining the dimension H–h. After the oxide mask removal, a cladding oxide layer was deposited. TEOS oxide was chosen for the cladding oxide, since among the available oxidation processes it generated the lowest stress to the waveguide structures [4].

The *double-masking process* is capable of achieving accurate mask patterning for both etch steps, since the lithography is always done on the unpatterned silicon surface. The only challenging part of this process is the second Si etching (step 4 in figure 2). After the first etch, there is topography in the structure, and etching this topography deeper in silicon results in localized surface roughness. The roughness is generated at the upper corners of the lower etch step in the form of a spiky structure along the corners. It can be reduced by a subsequent thermal oxidation or Si wet etching, but it is difficult to remove the residuals completely. However, the excess Si roughness might be avoided by slightly compromising the smooth waveguide side walls and verticality of the etch. This should be studied more, since the *double-masking process* is preferred when accurate lithography and deep etching is required.

2.2. Sequential process

The other process option was the *sequential process*, in which the basic waveguide structure and the additional grooves were fabricated sequentially, as shown in figure 3. The upper Si etch step was defined first by patterning the oxide layer with photolithography and dry oxide etching. After the Si etch, the resist was removed, while the patterned oxide was left on the unetched areas. The second lithography was then done, defining the lower etch (g). The spinning process over topography required special attention. Here, lithography with sufficient quality was achieved by changing the resist dispensing parameters and optimizing the exposure time. The exposure was done in the multi-exposure mode so that the lamp was on three times for a period of 20 s. For comparison, the standard exposure time for the contact aligner (Karl Süss MA6) used here was 30 s for the 2.1 μm thick resist (SPRT515). The total exposure time of 60 s and development time of 120 s (in AZ726 developer) proved sufficient parameters for the lithography. After the second Si etch, the resist mask and the oxide mask were removed. Finally, TEOS oxide cladding was deposited.

The use of the *sequential process* results in very smooth Si surfaces and corners, but the resolution of the lithography on the uneven surface limited the dimensions achievable with the process. The maximum etch depth before the second lithography depends greatly on the mask patterns and the lithography process used. With the lithography process used here the maximum depth of the first etch was approximately 6 μm. However, by using resists designed for high aspect ratio, structures with small features and deep etches can also be realized with the process. The *sequential process* is advisable when shallow etches are used, or when sharp corners must be achieved in the multi-step structure.

2.3. Optical characterization

The optical properties of the fabricated structures were determined using the insertion loss measurements. The set-up enabled separate transmission measurements for both TE and TM polarization. In the measurement the laser light was polarized and butt-coupled into a waveguide with a polarization-maintaining fibre. One axis of the fibre was aligned parallel to the chip surface, i.e. horizontally. This ensured that the polarization modes of the input fibre were coupled directly to the polarization modes of the waveguide with minimum cross-talk (below -25 dB). The transmitted light was coupled into a single-mode fibre and guided to a detector. The multi-step test structures had equally long reference waveguides on the mask set. They had a cross-section identical to the input and output waveguides of the corresponding multi-step structure. Thus, the coupling losses, as well as the losses of the input and output waveguides could be subtracted from the total (fibre-to-fibre) insertion loss. The accuracy of the resulting on-chip insertion loss determination was estimated as ± 0.5 dB. The measurement accuracy was further improved by joining identical successive components and measuring the on-chip insertion loss through several elements. Thus, the inaccuracy of the on-chip insertion loss measurement was divided between the successive elements. The measurements were carried out at 1550 nm wavelength.

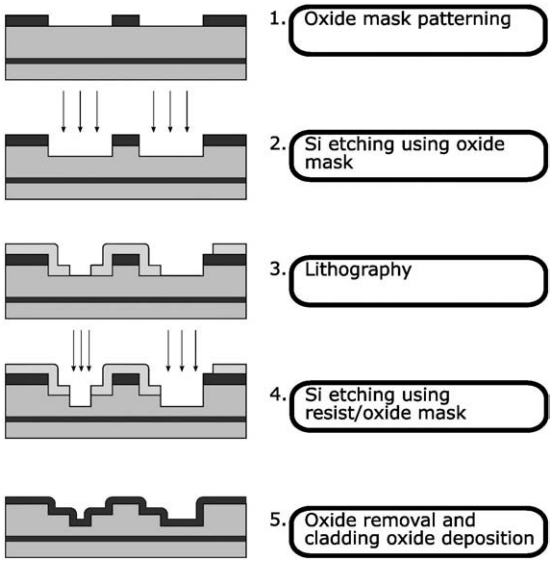

Figure 3. Sequential multi-step process.

3. Applications of the multi-step processing

3.1. Waveguide bends

The combination of SM operation and a large field profile requires very long bending radii. This was confirmed in the simulations carried out with the commercial TempSelene software (version 4.3.04) for SOI rib waveguides with various thicknesses. The minimum bending radius for a given bending loss depends significantly on the waveguide dimensions. For example, if the acceptable loss is set to a relatively high value of 1 dB/90°, a bending radius above 20 mm has to be used for 10 μm thick waveguides. This is clearly too large for useful components. A bend size reduction can be achieved by reducing the waveguide dimensions, but at the same time the advantages of large mode-field are lost. Another solution is the continuous fine-tuning of waveguide width and bending radius along the bend. However, the improvements with this approach are rather limited. The multi-step processing principle can provide an elegant and a radical solution for reducing the

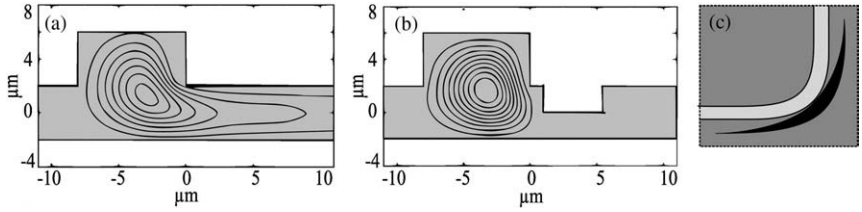

Figure 4. Cross-sections and calculated intensity distributions of SOI waveguides with a bending radius of 10 mm (a) without and (b) with an additional groove. (c) Top view showing the positioning of the groove in a bent waveguide.

size of a waveguide bend. By etching an additional groove to the outer edge of a bent rib waveguide (figure 4), one can increase its horizontal effective index contrast. Here, the groove bend test structures were fabricated with the *double-masking process.* The upper Si step was 5.1 μm deep for the bent 10 μm thick rib waveguide. The additional grooves were designed to approach the bent waveguide from a distance, so that coupling losses between the straight and bent waveguide sections were minimized. The width of the groove was of the same order as the rib of the bent waveguide. Each bend test structure was composed of four successive 45° bends.

Two bending radii were used for the test bent waveguides with a groove, 5 and 10 mm. For the 5 mm bending radius, the bend loss was determined as 0.9 ± 0.1 dB/90° and 0.7 ± 0.1 dB/90° for the TE and TM polarizations, respectively. Thus, the groove enabled a significant decrease of the bending radius from over 20 to 5 mm with 10 μm thick SOI waveguides, if the 1 dB/90° bending loss limit is used. For comparison, a similar waveguide with 5 mm bending radius without the groove resulted in a bending loss over 10 dB/90° for both polarizations. Similar results were achieved for the 10 mm bending radius. This suggests that the bending losses measured here were not dominated by the loss factor proportional to the bending radius, but another loss mechanism emerged. Since the *double-masking process* was used, the spiky Si residuals along the corner of the additional groove probably caused excess scattering losses along the bend. It is expected that by fabricating the grooves with the *sequential process*, the bending losses can be further decreased. It is worth noticing that the additional groove measured here was through-etched until the BOX layer, unlike the partially etched groove in figure 4. Generally, this enhances the multimode behaviour in a bend, reduces the bending losses through a higher index contrast, and increases the scattering losses at the etched surface.

3.2. Waveguide mirrors

Another application of the proposed multi-step process is a through-etched mirror facet monolithically integrated with a partially etched, 10 μm thick SM rib waveguide. The main advantage of the rib-type waveguide mirror is that it occupies a very small footprint when added to a SM rib waveguide circuit. The waveguide mirror fabricated in this study is schematically illustrated in figure 5. The angle between the input and output waveguides was 90°. The multi-step processing described here enabled a passive alignment of the lower etch step to the mirror facet. Thus, the alignment of the mirror to the input and output waveguides was not affected by the limited

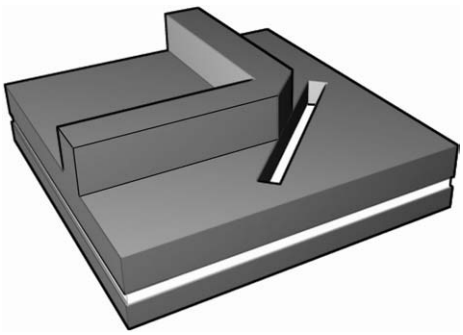

Figure 5. SOI waveguide mirror monolithically integrated with rib waveguides.

alignment resolution. Since the mirror facet is not formed during a single etch step, but two successive steps are used, it is crucial to avoid a discontinuity at the junction of the etch steps. This kind of discontinuity is typical for the *sequential process* due to the limited resolution of the second lithography. Thus, the fabrication of the waveguide mirror was done with the *double-masking process*. With this process, a uniform and smooth mirror facet was achieved. The upper Si etch step was 4.9 μm deep, while the lower etch step was done through the remaining SOI layer. Each mirror test structure involved eight 90° mirrors.

The best loss results for the 90° rib waveguide mirrors were measured as 0.59 ± 0.06 dB/90° and 0.74 ± 0.06 dB/90° for the TE and TM polarization, respectively. As the footprint of the mirror is significantly smaller than that of the bend, the use of the mirrors for thick waveguides is very attractive. It should be noted, however, that the optical losses of the mirror are very sensitive to the verticality and roughness of the mirror facet. Here, the *double-masking process* and the specially designed ICP Si etch process enabled the low optical losses of the waveguide mirror.

3.3. Waveguide converters

Thick Si rib waveguides have many advantages, such as simultaneous SM operation and good fibre coupling efficiency, which are impossible for strip-type waveguides. However, Si strip waveguides can also offer some advantages, such as simple design and simulation due to the vertical symmetry, low inter-waveguide cross-talk, extremely small bending radii, and a lack of waveguide dispersion. Therefore, a low-loss converter between strip and rib waveguides is very useful in the design and minimization of the microphotonic chips. Another

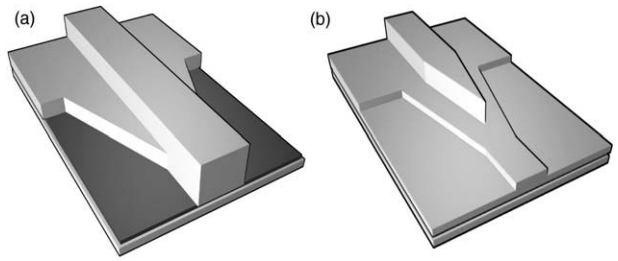

Figure 6. Schematic illustration of (a) a rib–strip converter and (b) a vertical taper.

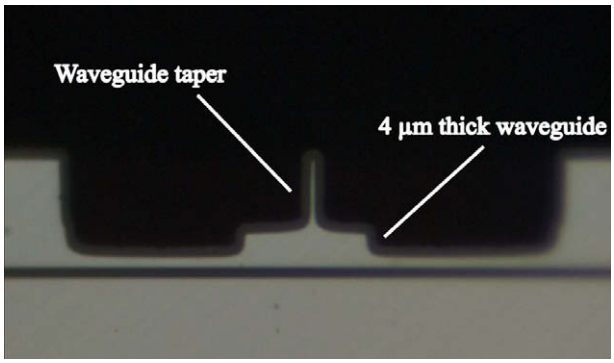

Figure 7. Microscope image of a cross-section of a vertical taper. Both 4 μm and tapered 10 μm rib waveguides are visible.
(This figure is in colour only in the electronic version)

useful element for microphotonics is a vertical taper, which adiabatically changes the thickness of an SM rib waveguide. Rib–strip converters and vertical tapers are schematically illustrated in figure 6. In the rib–strip converter (figure 6(a)) the additional grooves realized beside the rib waveguide are spread, until a strip waveguide is formed. In the vertical taper (figure 6(b)), the thick rib waveguide is narrowed down until it vanishes. By then, the light is coupled from the thicker waveguide into the thinner rib waveguide. It should be noted that the converters and vertical tapers can be modified by tuning the depths of the two etch steps (without modifying mask layouts). In figure 6 the etch depths relative to the SOI layer thickness are approximately 50% + 50% for the converter and 60% + 20% for the vertical taper. However, by using e.g. 50% + 25% etch steps for the converter, the conversion would appear between two rib waveguides with clearly different slab thicknesses and h/H ratios. Thus, the converter can be considered as a structure for changing the horizontal confinement of a waveguide. Similarly, using e.g. 60% + 40% etch steps for the vertical taper would provide a transformation between a thick rib waveguide and a thinner strip waveguide (instead of a thinner rib waveguide). Thus, the vertical taper essentially changes the waveguide thickness.

The vertical taper was fabricated with the *sequential process*, which ensured a low top surface roughness of the thinner waveguide. The upper etch was about 6 μm deep, defining the 10 μm thick rib waveguide. The thickness of the thinner waveguide was also defined by this etch step to 4 μm. The depth of the lower etch step was 2 μm. The taper section is illustrated in figure 7. In the figure, the 10 μm waveguide is narrowed well below 1 μm. The test mask had six successive vertical taper elements adjoint, so that the light was coupled from the 10 μm thick waveguide into the 4 μm waveguide and vice versa three times. Thus, the measurement accuracy for a single vertical taper was better than $\pm$0.1 dB. Based on the results, the excess losses for a single vertical taper were 0.7$\pm$0.1 dB, including the impact of the polarization dependent loss.

The *double-masking process* was used for the strip–rib converter. The upper etch step was 5 μm. This formed the basic rib structure for the input waveguides. The lower etch step reached through the remaining $\sim$5 μm of the SOI layer. The losses induced by the rib–strip converter were determined by measuring the transmission of 22 successive elements, which gave a measurement accuracy of $\pm$0.02 dB. The resulting excess losses for a single rib–strip converter were 0.05 $\pm$ 0.02 dB for TE and -0.01 ± 0.02 dB for TM. The apparently negative loss for TM is due to the finite measurement accuracy. In conclusion, the excess loss and the polarization dependent loss are both below 0.07 dB for a single rib–strip converter.

4. Conclusions

Multi-step processing to be used in microphotonic applications was studied. Two options for the fabrication sequence were tested, both having one silicon etch step with an oxide mask and another with a resist mask. The *double-masking process* utilized two lithography steps before the two silicon etching steps. In the *sequential process*, each lithography step was followed by an etching step. The choice between the two options depends on the special requirements of the targeted structure. The multi-step processing was tested with different optical waveguide structures. An additional groove etched in a bent 10 μm thick rib waveguide enabled a significant bend loss reduction with a bending radius of 5 mm. Optical losses below 1 dB/90° were measured for a waveguide mirror. A vertical taper for coupling rib waveguides of different thicknesses had excess losses of 0.7 $\pm$ 0.1 dB. A converter coupling a rib waveguide to a strip waveguide showed a negligible loss below 0.07 dB. In the future, the multi-step fabrication will be extended to structures with more masks and etch steps to further increase the versatility of the technique.

Acknowledgments

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PUBLICATION III

Adiabatic and multimode interference couplers on silicon-on-insulator

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Adiabatic and Multimode Interference Couplers on Silicon-on-Insulator

Kimmo Solehmainen, Markku Kapulainen, Mikko Harjanne, and Timo Aalto

***Abstract*—Adiabatic and multimode interference (MMI) 3-dB couplers based on silicon-on-insulator rib waveguides were fabricated and measured. For testing purposes, pairs of identical couplers were cascaded to form Mach–Zehnder interferometers. The adiabatic couplers showed excess on-chip loss of $\sim$0.5 dB, extinction ratio (ER) of 15–20 dB, and a wide spectral range. The MMI couplers processed on the same wafer showed similar loss per coupler, higher ER, and limited spectral characteristics.**

***Index Terms*—Integrated optics, optical device fabrication, optical planar waveguide couplers, silicon-on-insulator (SOI) technology.**

I. Introduction

OPTICAL couplers are used in photonic integrated circuits (PICs) when it is necessary to couple light between different waveguides. Traditionally, they were realized using directional couplers. Unfortunately, these components have been found to be sensitive to wavelength, fabrication tolerances, and polarization state of light. During the past ten years, they have mostly been replaced by multimode interference (MMI) couplers, which have relaxed fabrication tolerances and sufficiently low polarization dependency. However, MMI couplers still have rather large wavelength dependency. To circumvent these limitations, adiabatic couplers have been developed and tested on $LiNbO_3$ [1], SiO_2 [2], and more recently on polymeric [3] waveguide materials. The term adiabatic means that there is no energy change between different modes in the coupler structure. Thus, power coupled to the fundamental mode stays in the fundamental mode even in the presence of dimensional changes and additional modes. This principle distinguishes the adiabatic coupler from directional and MMI couplers, where the excitation of higher order modes is the main requirement for the operation. Unlike simple Y-junctions, adiabatic couplers can be used as passive 2×2 couplers and, thus, to construct, e.g., active 2×2 switches. The main drawback of previous adiabatic coupler demonstrations has been that in order to avoid the excitation of higher order modes, the adiabatic couplers have been significantly longer than the equivalent directional couplers or MMI couplers. Thus, adiabatic couplers have not been widely used in integrated optics.

Silicon-on-insulator (SOI) is an attractive platform for realizing PICs and for integrating them monolithically with control electronics. Due to the ultrahigh refractive index contrast, SOI technology allows the large-scale integration of optical circuits. Extreme device miniaturization can be achieved with submicron nanowires [4], while mirrors and groove bends [5] enable the miniaturization of thicker waveguide devices as well. Compared with nanowires, rib waveguides with a larger cross section offer lower coupling losses to optical fibers and lasers, while maintaing single-moded (SM) operation.

In this study, SOI-based adiabatic couplers were, for the first time, fabricated and characterized using 4-μm-thick SM rib waveguides. Their performance was compared with MMI couplers, which, having been processed on the same SOI wafer, had identical fabrication tolerances. The properties under study included optical losses, polarization sensitivity, and spectral characteristics.

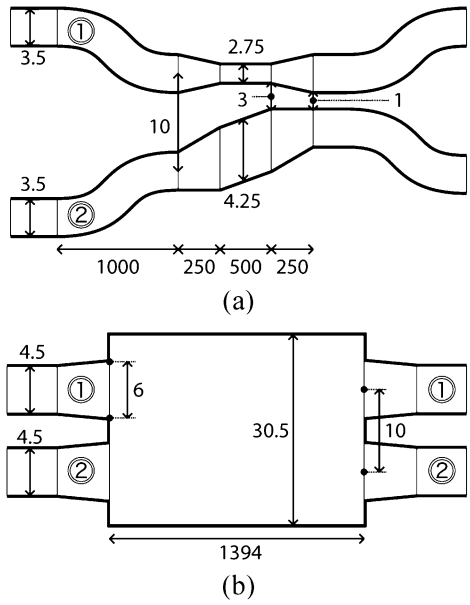

Fig. 1. Schematic view of (a) adiabatic coupler and (b) MMI coupler design. The dimensions are in micrometers (not in scale).

II. Design

The design was based on a simple waveguide cross section analysis carried out with a commercial TempSelene software. The layout of a single adiabatic coupler is shown in Fig. 1(a). The width of the input and output waveguides of the adiabatic coupler is 3.5 μm. From the initial (axial) separation of 50 μm, Waveguides 1 and 2 are brought to the axial separation of 10 μm with S-bends. After the bends, the waveguides are changed asymmetrically, so that Waveguides 1 and 2 are tapered to 2.75 and 4.25 μm, respectively. Then they are brought to a (edge-to-edge) distance of 3 μm, after which the actual

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The authors are with VTT Technical Research Centre of Finland, FI-02044 Espoo, Finland (e-mail: kimmo.solehmainen@vtt.fi; markku.kapulainen@vtt.fi; timo.aalto@vtt.fi; mikko.harjanne@vtt.fi).

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coupling section takes place. In this region, the waveguides are tapered to the same width of 3.5 μm and brought still closer to each other, to the minimum distance of 1 μm. The total length of the interaction region including all tapered waveguide sections is 1 mm. After the coupling section, the waveguides are brought apart with S-bends. The 3.5-μm-wide input and output waveguides of the couplers are tapered to the width of 8 μm at the output to reduce the fiber-coupling losses of the test chip (not shown in Fig. 1).

In fully adiabatic operation, the optical power from the input port of Waveguide 2 excites the even system mode of the coupler and splits evenly to the two output waveguides (with the same phase). Similarly, optical power from the input port of Waveguide 1 excites the odd system mode and splits evenly to the output waveguides (with opposite phases). In order to enable easy and accurate characterization of the couplers, a pair of these 3-dB couplers was cascaded to form a 2×2 Mach–Zehnder interferometer (MZI) device. The couplers are otherwise identical, but the latter one is point-mirrored from the first one. Thus, Waveguide 1 is made thicker and Waveguide 2 thinner in the latter coupling section. The MZI test device does not include any phase modulation structures, so that light coupled to Input 1 should always be transmitted to Output 2, and vice versa. High extinction ratio (ER) between the output powers of the two MZI outputs indicates that each coupler acts as a 3-dB coupler. Lower ER is an indication of unbalanced coupling, caused by the finite excitation of higher order modes.

The layout of an MMI coupler is shown in Fig. 1(b). The MMI tested here is based on paired interference, in which only some of the modes in the MMI region are excited [6]. In the layout, the length and width of the MMI region are 1394 and 30.5 μm, respectively. The input and output waveguides of the MMI structures are 4.5 μm wide.

Before the connection to the MMI region, they are tapered from 4.5 to 6 μm in order to avoid the excitation of higher order vertical modes. The axial separation of the input and output waveguides is 10 μm. As with the adiabatic couplers, a pair of identical couplers was used to form a 2×2 MZI layout.

When comparing the two design layouts, it can be seen that the adiabatic couplers are actually somewhat shorter than the equivalent MMI couplers. It was estimated that the used tapering angles are small enough to provide very adiabatic operation. However, longer tapers might behave even more adiabatically, i.e., to further suppress the excitation of any unwanted modes.

In order to measure the on-chip excess loss of the couplers, the mask design included also reference waveguides. They had a cross section identical to the input and output waveguides of the test devices. They also had the tapers and bends identical to the test devices, so that the loss originated from these sections did not contribute to the on-chip loss determination.

III. Fabrication and Measurements

The base for the fabrication was an SOI wafer with 100-mm diameter, 4.4-μm SOI layer, and 1-μm-thick buried oxide layer. First, a 1-μm-thick oxide hard mask was deposited on the wafer. It was then patterned with standard photolithography and etched using a parallel-plate reactive ion etcher. The silicon etch was carried out with an inductively coupled plasma etcher by using the patterned oxide as a hard mask. The etch recipe was a modification from the STS Advanced Silicon Etch, as described in [7]. The etch depth was 2 μm. After removing the oxide mask, a 1-μm-thick thermal oxide was grown on top of the patterned silicon structure to reduce the surface roughness. During the oxidation, the thickness of the SOI layer decreased to 4 μm. The oxidation also changed the linewidth, so that the total linewidth change due to the fabrication (oxidation and photolithography) was 1.2 μm. The thermal oxide was removed with wet etching in buffered hydrofluoric acid before the growth of the cladding oxide layer. The 1-μm-thick cladding oxide was deposited with the tetra-ethyl-ortho-silicate process in a low-pressure chemical vapor deposition furnace. The final steps of the fabrication process were the dicing of the wafer and polishing the chip facets to optical quality.

TABLE I
Loss of MZI Devices Based on Adiabatic and MMI Couplers (Two Couplers Cascaded)

Measurement	Excess On-Chip Loss at 1550 nm (dB)			
	$1_{in} \rightarrow 1_{out}$	$1_{in} \rightarrow 2_{out}$	$2_{in} \rightarrow 1_{out}$	$2_{in} \rightarrow 2_{out}$
Adiabatic TE	14.8	0.4	1.1	16.6
Adiabatic TM	20.7	0.8	1.2	19.0
MMI TE	21.5	1.0	2.1	23.2
MMI TM	29.8	0.3	0.6	27.3

The loss measurements were measured with both TE and TM input polarizations. In the measurements, linearly polarized light at 1550-nm wavelength was coupled from a polarization-maintaining fiber into an input waveguide. The transmitted light from an identical output waveguide was coupled into an optical power meter via a single-mode fiber. The use of SM fibers guaranteed that the insertion loss (IL) was measured for the fundamental mode only. Index matching oil (refractive index $\approx$1.5) was used to reduce the reflections at the waveguide facets. The total IL of all test devices was calculated by subtracting the power transmitted directly from the input fiber to the output fiber. In order to determine the on-chip excess loss of a coupler, the rather imprecise input and output coupling losses should be subtracted from the IL. To improve the measurement accuracy, the total IL measured for a test device was compared with an equally long and wide reference waveguide.

In the spectral measurements, unpolarized light from an optical source with a spectral range of 1250–1650 nm was coupled into the input waveguide with an SM fiber. The output light was coupled into another SM fiber and guided to a spectrum analyzer.

IV. Results and Discussion

The excess on-chip losses of MZI devices based on both adiabatic and MMI couplers are summarized in Table I at 1550-nm wavelength. For the adiabatic couplers, the loss is about 0.2–0.6 dB per coupler for both polarizations, while the ER of the MZI device is about 15 dB for TE and almost 20 dB for TM. The fiber-coupling loss of the test chips is estimated to be 3.9 dB/facet, which includes both the modal coupling and reflection losses.

The excess loss per MMI coupler is 0.2–1.0 dB for both polarizations. As with the adiabatic couplers, the variation in the

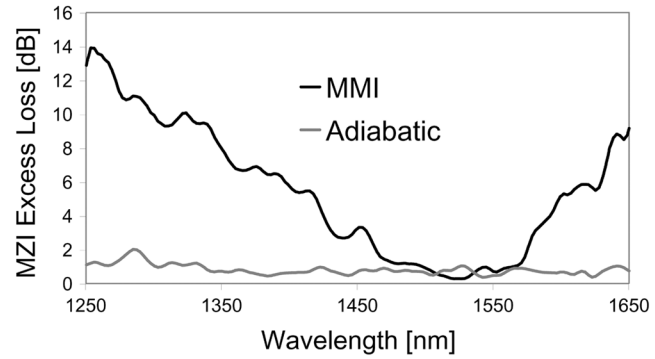

Fig. 2. Excess loss of the 2×2 MZI devices based on adiabatic and MMI couplers. The spectra are measured from input Port 1 to output Port 2.

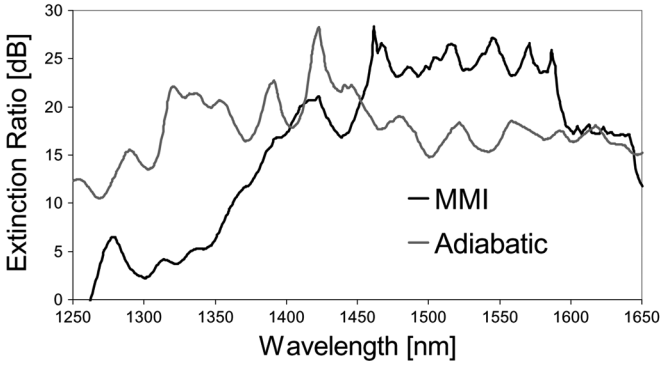

Fig. 3. ER of adiabatic and MMI couplers as a function of wavelength.

results is due to the finite accuracy of the measurement setup. The ER of the MMI-based MZI is over 20 dB for TE and almost 30 dB for TM, which is clearly better in comparison with the adiabatic coupler. The results of the MMI-based device are comparable to those achieved earlier with SOI [8]. In order to improve the ER of the adiabatic coupler-based device, the device geometry should be optimized to further suppress the residual excitation of the higher order modes.

The results from the spectral loss measurements are shown in Fig. 2. The MZI based on adiabatic couplers shows a very flat response with excess loss around 1 dB throughout the measured spectral range. The exception is the peak around 1290 nm, where the maximum loss of 2 dB was measured. The MMI-based MZI shows losses about 1 dB in a spectral range of 1480–1570 nm. However, outside this low-loss region, the losses increase rapidly.

The spectral behavior of the ER for the MZI devices is shown in Fig. 3. For the MZI based on adiabatic couplers, the ER remains above 15 dB for the best part of the spectrum, except around 1270 nm, where it reaches a minimum of 10 dB. The fluctuations in the spectrum are caused by the residual excitation of the higher order modes, which could not be completely avoided in this first experiment. However, it can clearly be seen that the overall behavior of the ER spectrum is much flatter for the adiabatic couplers than for the MMI couplers.

Indeed, for the MMI-based MZI the ER decreases to zero at the wavelength of 1260 nm. Only in the relatively narrow spectral range, near the targeted 1550-nm wavelength, the MMI couplers show superior ER.

V. Conclusion

Adiabatic and MMI couplers on SOI were fabricated and characterized. The adiabatic coupler design was based on asymmetric coupler arms and 3-dB operation. The MMIs were based on paired interference and tapered input and output waveguides. In order to test their performance, a pair of identical couplers was cascaded to form a 2×2 MZI structure. The fabrication of the devices was based on single-mode 4-μm-thick rib waveguide technology.

In the measurements, the couplers based on different principles showed comparable losses and polarization sensitivities at 1550 nm. However, the spectral range was clearly wider for the adiabatic couplers than for the MMI couplers. It was, therefore, shown that when a broad wavelength range is required, i.e., from 1300 to 1600 nm, low-loss adiabatic couplers with acceptable ER can be realized on SOI. Furthermore, it was shown that using adiabatic couplers does not necessarily require larger component size than MMI couplers with comparable characteristics.

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PUBLICATION IV

AWG based DWDM multiplexers combined with attenuators on SOI

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AWG Based DWDM Multiplexers Combined with Attenuators on SOI

G. Przyrembel (1), B. Kuhlow (1), K. Solehmainen (2), T. Aalto (2), P. Heimala (2) and L. Moerl (1)
1 : Fraunhofer Institute for Telecommunications, D-10587 Berlin, Germany, przyrembel@hhi.fhg.de
2 : VTT Technical Research Centre of Finland, Tietotie 3, FIN-02044 VTT, Espoo, Finland,
kimmo.solehmainen@vtt.fi

Abstract *We report on the design, fabrication and optical characteristics of SOI based AWG multiplexers combined with attenuators. The AWG devices and attenuators comprised 8 channels with 200 GHz channel spacing around 1550 nm wavelength.*

Introduction

Silicon-on-insulator (SOI) is regarded as an attractive platform for integrating optical and electronic functions, since it can utilize the mature materials processing and extensive electronic functionality of silicon technology [1]. It also has some important features for integrated optical components too, such as e.g. good optical properties at telecommunication wavelengths around 1.3 µm and 1.55 µm. Arrayed waveguide grating (AWG) structures and variable optical attenuators (VOA) are essential building blocks of such an optical board technology to serve e.g. as optical multiplexer and optical wavelength division multiplexer (WDM) filters, respectively, with equalization functionality.

In this work we present SOI based AWGs [2] with combined attenuators to act as optical multiplexers. The related AWGs were designed for the launched laser polarisation and had 8 channels in the C-band. VOAs relying on thermally controlled Mach-Zehnder interferometers (MZI) were integrated with the AWGs.

Simulation and Design

The AWGs were designed as 8 channels devices with 200GHz (1.6 nm) channel spacing on the ITU grid around 1.55 µm centre wavelength. The optical simulation was performed on AWGs relying on ridge waveguides in 4 µm SOI with 2.0 µm ridge height and 3.2 µm ridge width. The simulations of the AWGs included the input and output star couplers with the associated input and output ports of the device and the array waveguide ports, respectively. The waveguide array itself was introduced by appropriate phase shift terms. One of the results obtained from 3D BPM simulation is shown in fig. 1, where the grating order was chosen to be m=70. The insertion loss can be seen to be below 1 dB. The contribution of the waveguide propagation loss was neglected in these calculations.

The VOAs were implemented as symmetrical Mach-Zehnder interferometer structures with 2 mm long and 15 µm wide heaters on top, fig. 2. For the MZI-VOAs 3 dB couplers are required and these were realised by 1x2 multi-mode interference (MMI) couplers. They were also evaluated using 3D BPM calculations. The input and output waveguide ports of the MMI were designed as tapers at the waveguide-to-body interfaces. This structural layout was designed to ensure smooth optical transition and improve mode matching. Based on the dimensional optimisation an MMI structure with a length of 470 µm and a body width of 19.75 µm was chosen. The 3D BPM simulation results of this MMI are shown in fig. 3.

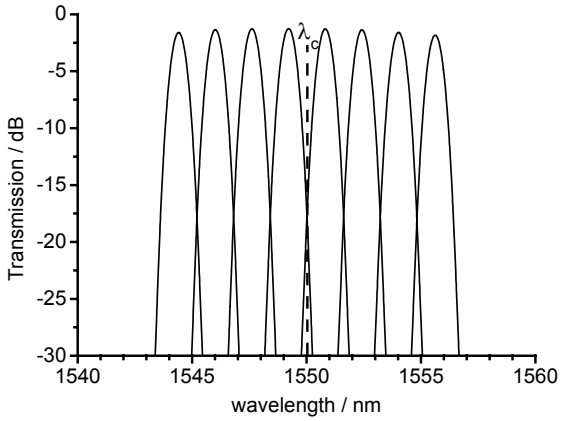

Fig. 1 Simulated transmission characteristics (3D BPM simulation) of an 8-channel, 200GHz AWG.

Fig. 2 Mach-Zehnder Interferometer with two 3-dB 1x2 MMIs. The grey areas represent the heaters.

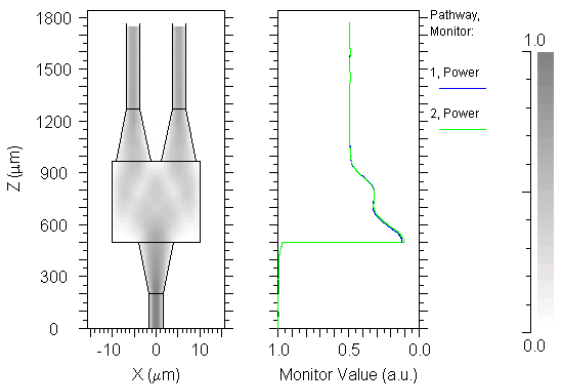

Fig. 3 BPM simulation (3D) of a 3 dB 1x2 MMI coupler at 1550 nm wavelength.

Fabrication

The device structures were fabricated on an epitaxially thickened smart-cut SOI wafer with a 4.5 µm thick SOI layer and a 1 µm thick buried oxide layer (BOX). The waveguides were defined by standard photolithography and dry Si etching. The etching was done using an inductively coupled plasma type reactive ion etcher [3]. The etch depth was 2.2 µm. After the etch, a 0.46 µm thick thermal oxide was grown to reduce the roughness of the waveguide sidewalls. The thermal oxide was removed with wet etching in buffered hydrofluoric acid before growing a cladding oxide layer. The 1 µm thick cladding oxide was deposited with the tetra-ethyl-ortho-silicate (TEOS) process in a low-pressure chemical vapour deposition (LPCVD) furnace. For the VOA structures metal heaters were formed on top of the waveguide structure using molybdenum. A thin layer of silicon nitride was used as passivation layer on Mo. Finally, the wafer was diced and the AWG chip facets were polished.

Results

In fig. 4 the measured characteristics of an 8-channel AWG with integrated VOAs are shown. The loss of the combined device was 7 dB. The excess loss of the VOAs can be estimated to be 1.5 dB from the difference to the measured loss of 5.5 dB of an identical AWG without the VOAs.

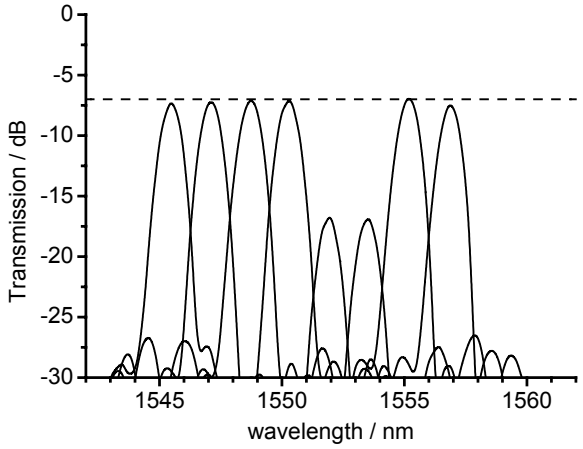

Fig. 4 Measured characteristics of an 8-channel 200 GHz AWG with directly attached MZI-VOAs. Ch.5 and Ch.6 are attenuated in this case by 10 dB.

Fig. 5 shows the VOA attenuation versus the applied heater power. For each VOA the electrical power corresponding the maximum optical attenuation is approx. 160 mW, where the dynamic range is about 15 dB. The transition times of the VOAs were measured at the optical chip output using an HP11982A Amplified Lightwave Converter and with the aid of an electrical pulse generator. Fig. 6 shows the transfer characteristic indicating a maximum attenuation of some 15 dB. The transition times for rise and fall were found to be smaller than 10 µs.

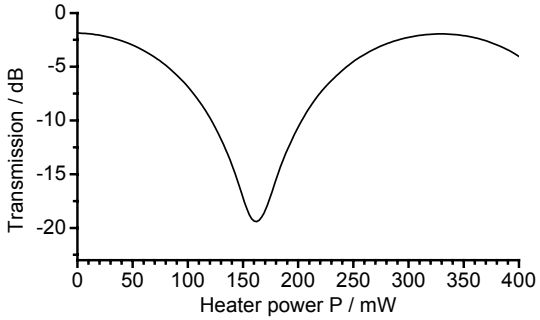

Fig. 5 Measured optical attenuation due to powered heater electrode.

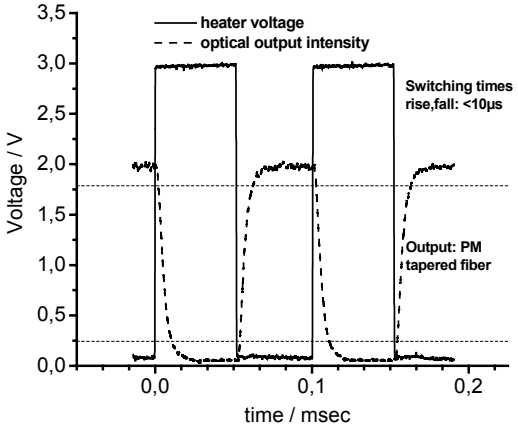

Fig. 6 VOA heater voltage and corresponding optical output intensity.

Conclusions

Simulation, component design, fabrication, and characterisation of AWGs integrated with thermally controlled VOA structures were performed. The AWG was designed for the launched laser polarisation with 8 channels in C-band. The channel spacing was chosen to be 200 GHz. The insertion loss of the fabricated AWG was measured as 5.5 dB The VOAs were based on MZIs incorporating 1X2 MMI couplers. The VOAs showed an excess loss of 1.5 dB and had a dynamic range of 15 dB on the average. The maximum attenuation was achieved at 160 mW power consumption of the heaters and the rise and fall times were below 10 µs.

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PUBLICATION V

Low-loss converters between optical silicon waveguides of different sizes and types

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Low-Loss Converters Between Optical Silicon Waveguides of Different Sizes and Types

Timo Aalto, Kimmo Solehmainen, Mikko Harjanne, Markku Kapulainen, and Päivi Heimala

***Abstract*—Two types of low-loss converters between different optical waveguides on silicon-on-insulator are demonstrated. A vertical taper between 9.4- and 3.8-μm-thick single-moded rib waveguides gives an excess loss of 0.7 ± 0.2 dB with negligible polarization dependency. The second structure converts a 9.7-μm-thick rib waveguide into an equally thick and highly multimoded strip waveguide with a negligible loss ($<$0.07 dB) for the fundamental mode. The fabrication of both structures is based on a simple two-step etch process with a relaxed mask alignment tolerance and no need for epitaxy.**

***Index Terms*—Adiabatic conversion, integrated optics, multistep patterning, silicon microphotonics, silicon waveguide, silicon-on-insulator (SOI) technology, vertical taper.**

I. Introduction

SILICON-ON-INSULATOR (SOI) is an attractive platform for realizing integrated optical circuits and for integrating them monolithically with control electronics. Due to the ultrahigh refractive index contrast, SOI technology allows the large scale integration of optical circuits. Extreme device miniaturization can be achieved with submicron nanowires [1], while mirrors and groove bends [2] enable the miniaturization of thicker waveguide devices as well. A rib structure provides single-moded (SM) operation even if the waveguide thickness is increased to >10 μm [3]. For low-loss coupling to standard SM fibers the silicon waveguide thickness should be approximately 10 μm. Some examples of typical cross sections in silicon waveguides are shown in Fig. 1.

The main problem in using thick rib waveguides in optical circuits is the required large bending radius. On the other hand, thin waveguides suffer from inefficient fiber coupling. Thus, the optimum solution would be an adiabatic converter between a thick and a thin waveguide on a single silicon chip. A more general target is an adiabatic conversion between two waveguide cross sections with different sizes and/or types. For example, a rib waveguide could be converted into a strip waveguide with the same or different thickness. This could be used, e.g., to realize compact waveguide arrays, tight bends, waveguide mirrors, or short multimode interference couplers [2].

The above-mentioned conversion structures can be realized by patterning silicon waveguides with more than one etch step. Adiabatic operation is achieved with a sufficiently long conversion structure. Previously, a vertical silicon waveguide taper was demonstrated by using epitaxial growth [4]. However, that process was relatively complicated to implement and its details were not disclosed. A rib-strip converter structure has been proposed by others as well [5].

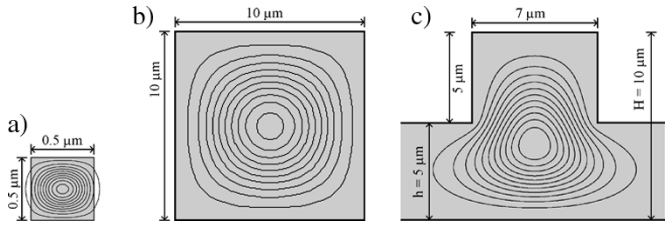

Fig. 1. Example cross sections of different silicon waveguides (not in scale): (a) a nearly SM nanowire, (b) a multimoded strip waveguide, and (c) an SM rib waveguide. Contour lines illustrate the intensity distribution of the fundamental TE mode. Cladding around the (gray) core is not illustrated.

In this study, two multistep waveguide structures were realized in SOI by using two mask layers, two silicon dry etch steps, and no epitaxy. The devices are a low-loss vertical taper and a converter from an SM rib waveguide into an equally thick, highly multimoded strip waveguide. Both devices are simple to fabricate and insensitive to a small misalignment between the masks. The target wavelength is 1550 nm, but the adiabatic devices should operate in a wide spectral range.

II. Design and Simulation

The design of both conversion structures was based on simple linear tapering in the horizontal direction. With two mask layers and two corresponding etch steps, it is possible to create various waveguide cross sections and to connect them with adiabatic converters. Example cross sections along the two chosen conversion structures are shown in Fig. 2 (including the input and output). The calculated mode profiles clearly show the potential for adiabatic conversions between the input and output waveguides—even in the case of finite mask alignment accuracy. Schematic device top views are shown in Fig. 3.

The simulations were carried out by two methods. The local modes corresponding to different waveguide cross sections were solved with a commercial mode solver (TempSelene, v. 4.3). This was used to estimate the impact of both the finite width in the vertical taper's tip and the finite distance of the second etch step at the input end of the multistep structure. Some simulations were also carried out using the three-dimensional beam propagation method (BPM) to provide a rough estimation for the maximum tapering angles for adiabatic operation. The horizontal tapering angles of the vertical taper and the rib-strip converter were chosen to be 0.3° and 1.7°, respectively. Otherwise the design was primarily based on the modal analysis due to the limited accuracy of the used BPM software (Prometheus v.

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The authors are with VTT, Espoo FI-02044, Finland (e-mail: timo.aalto@vtt.fi).

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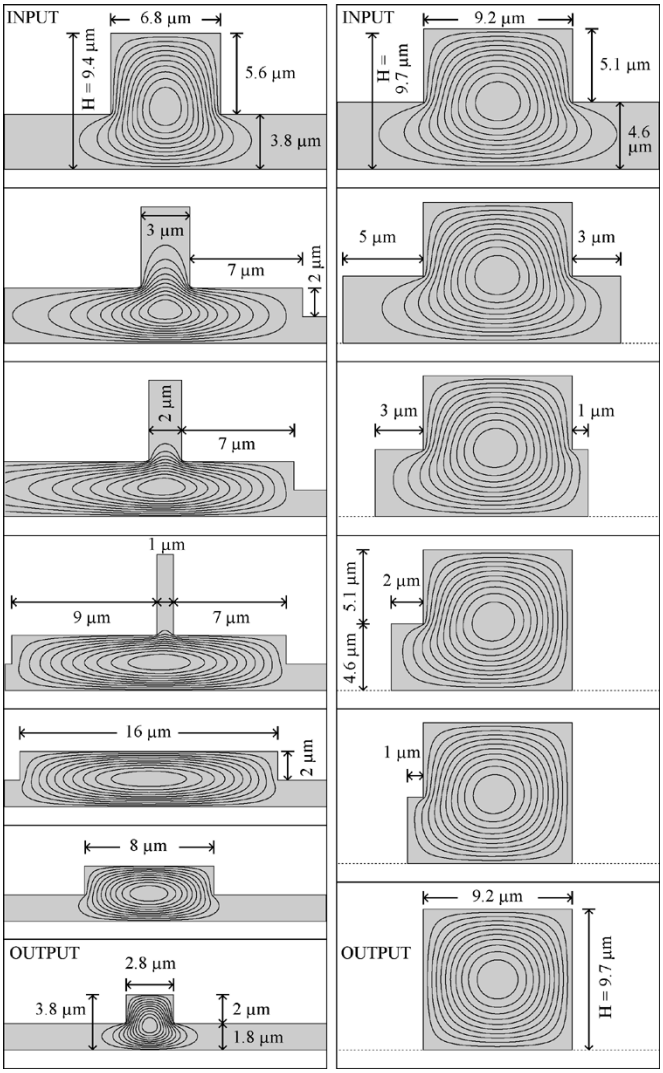

Fig. 2. Different cross sections of the vertical taper (left) and the rib-strip converter (right) with calculated intensity distributions for the fundamental TE mode. The results for TM polarization are almost identical. Misalignment of 1 μm is assumed between the two masks. Otherwise dimensions are identical to those measured from the fabricated devices.

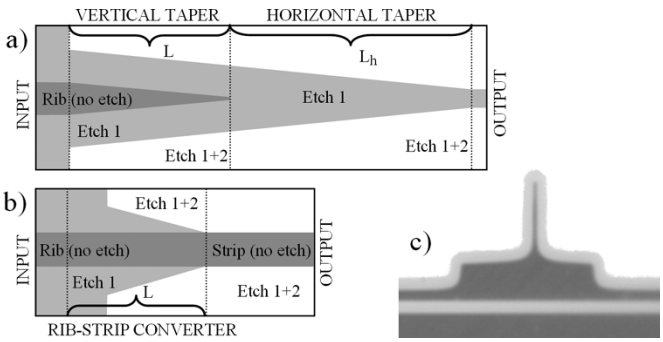

Fig. 3. Schematic top views of (a) the vertical taper and (b) the rib-strip converter. The three colors (dark gray, light gray, and white) illustratate the different silicon thickness after the two etch steps. (c) Microscope image of a fabricated vertical taper's cross section (inverted colors).

4.3). The lengths (L) of the multistep conversion structures were chosen to be 640 and 205 μm, respectively. The target distance between the two etch steps of the vertical taper was fixed to 8 μm and the length L_h of the horizontal taper behind the device was set to 1160 μm. Along the rib-strip converter, the etch step distance is reduced from 4 to 0 μm. The vertical taper is longer than the rib-strip converter as it induces a larger change into the effective index and the intensity distribution of the fundamental mode.

Special test chips were designed to obtain high measurement accuracy. Each test device converted a thick rib waveguide into a thin rib waveguide or a thick strip waveguide, and back, N times. The output ends of opposite vertical tapers were joined with a 2-mm-long thin rib waveguide. The output ends of opposite rib-strip converters were joined with 0.5-mm-long strip waveguides. The successive converter pairs were joined with 2-mm-long thick rib waveguides. The input and output waveguides of the vertical taper were designed to be clearly SM, while the input waveguide of the rib-strip converter was designed to operate at the SM-limit. The designs aimed to efficiently suppress the propagation of higher order modes.

Furthermore, each test chip included equally long straight reference waveguides with a cross section identical to the input of the corresponding converter structure.

III. Fabrication

Both devices were fabricated on bonded SOI wafers with 100-mm diameter and 9.5 ± 0.5 μm SOI layer thickness. A 1-μm-thick oxide hard mask was first deposited on the wafer and then patterned with standard photolithography and mask #1. The minimum linewidth on the laser-patterned lithographic masks is 900 nm. The primary silicon etch was carried out with an inductively coupled plasma (ICP) etcher by using the patterned oxide as a hard mask. The etch depth was 5.6 ± 0.3 and 5.1 ± 0.3 μm for the vertical taper and the rib-strip converter, respectively. This formed the basic rib structure for the input waveguides. Both the original SOI thicknesses and the etch depths involve small variations over the wafer (as indicated above), but these do not disturb the operation of the adiabatic devices.

The secondary silicon etch was also carried out with the ICP etcher, but with a resist mask only. This resist mask was deposited and patterned with the mask #2 after removing the previous resist layer. The underlying oxide mask patterned with mask #1 was not removed before the secondary silicon etch. Therefore, the patterned oxide layer below the second resist layer prevented the secondary etching of those areas that were not subject to the primary etch as well. This enabled the passive alignment of the two etch steps in the formation of deep vertical sidewalls for the rib-strip converter. In the lithography equipment used in this work, the misalignment between the two masks can be kept below 1 μm. The secondary etch depth was 2.0 ± 0.1 μm for the vertical taper and through the remaining $\sim$5 μm of SOI for the rib-strip converter.

The remaining resist and oxide layers were then removed and a 1-μm-thick thermal oxide was grown on top of the patterned silicon structure to reduce surface roughness and to narrow the finite width of the vertical taper's tip. To minimize the waveguide birefringence, this high-stress oxide was then removed and a low-stress tetraethyl orthosilicate cladding oxide layer of $\sim$1 μm was deposited. Finally, the wafers were diced and the

chip facets were polished to optical quality. A microscope image of a vertical taper's cross section close to the tip is shown in Fig. 3.

IV. Measurement Setup

In all loss measurements, linearly polarized light at 1550-nm wavelength was coupled from a polarization-maintaining fiber into an input waveguide and then collected from an identical output waveguide into a detector via SM fiber. Index matching oil ($n \approx 1.5$) was used to reduce the reflections at the waveguide facets. The total insertion loss (IL) of all test devices was calculated by subtracting from the result the power transmitted directly from the input fiber to the output fiber. However, the key to the high measurement accuracy was the comparison of the total IL measured for a test device (with $2N$ converters) and for its equally long reference waveguide. For the measurement of the on-chip excess loss of a single converter structure this procedure almost completely eliminates the impact of the input and output coupling and, furthermore, reduces the impact of the limited transmission measurement accuracy (± 0.5 dB) by a factor of $2N$. Due to the slightly increased top surface roughness the propagation loss is higher in the thin rib waveguide than in the reference waveguide, which leads to a worst-case loss estimate for the vertical taper.

The use of SM fibers guarantees that the IL is measured for the fundamental mode only. The polarization-dependent loss (PDL) can be calculated after measuring the excess loss with both TE and TM input polarization.

V. Measurement Results

The measured total IL for a test device with six successive vertical tapers was 10 and 9.5 dB for the TE and TM polarization, respectively. For the reference waveguide, the corresponding losses were 5.8 and 5.6 dB, respectively. Thus, the majority of the losses does not originate from the vertical tapering, but from the reflections ($\sim 2 \times 0.8$ dB) and the mode mismatch ($\sim 2 \times 1.8$ dB) at the nonoptimized waveguide facets, and the propagation loss along the 24-mm-long waveguides ($\sim$0.5 dB). Based on the results, the estimated excess loss for a single vertical taper is 0.7 ± 0.1 dB for TE and 0.65 ± 0.1 dB for TM. Therefore, the PDL is below the measurement accuracy and the excess loss can be estimated as 0.7 ± 0.2 dB including the impact of the PDL.

Similarly, the measured total IL for 22 successive rib-strip converters was 5.4 and 5.2 dB for TE and TM polarization, respectively. For the reference waveguide, the losses were 4.4 and 5.3 dB, respectively. The excess loss for a single rib-strip converter is 0.045 ± 0.02 dB for TE and -0.005 ± 0.02 dB for TM. The apparently negative loss for TM is due to the finite measurement accuracy. In conclusion, the excess loss and the PDL are both below 0.07 dB for a single rib-strip converter.

VI. Conclusion

Two types of waveguide conversion structures were successfully demonstrated on SOI. An SM vertical taper provided waveguide thickness conversion from 9.4 to 3.8 μm with an excess loss of 0.7 ± 0.2 dB. The other device converted a 9.7-μm-thick rib waveguide into an equally thick and highly multimoded strip waveguide with a negligible loss ($<$0.07 dB). Both devices were fabricated with a simple process involving two masks and two Si etch steps.

In the future, the device geometries should be further optimized with respect to both the excess loss and the device size. Based on the simulations, it is expected that, e.g., nonlinear tapering can reduce the tapering loss. Other waveguide thicknesses and other types of conversions should also be tested.

The applicability of the vertical taper is mostly limited by the thickness variation of the down-tapered waveguide. However, vertical tapers can also be used on a separate input coupling chip with an array of SM fiber pigtails on one side. A dense array of thin Si waveguides on the opposite side can then be used to couple light into various optical devices that would otherwise have high fiber-coupling losses. With antireflection coatings and optimized cross sections at the ends of the input and output waveguides the reflections and mode mismatch losses can be minimized and the main remaining loss element is the vertical taper itself.

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PUBLICATION VI

Erbium-doped waveguides fabricated with atomic layer deposition method

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Erbium-Doped Waveguides Fabricated With Atomic Layer Deposition Method

Kimmo Solehmainen, Markku Kapulainen, Päivi Heimala, and Kirsi Polamo

***Abstract*—Atomic layer deposition was used in preparing erbium (Er)-doped waveguides. Ridge-type Er-doped Al_2O_3 waveguides were patterned on silica-coated silicon wafers using photolithography and wet etching. Optical absorption, emission, fluorescence lifetime, and signal enhancement measurements were performed. Polarization dependence of the absorption spectrum and birefringence of the waveguide were measured. The material showed strong absorption and wide emission spectrum around 1530 nm with full-width at half-maximum of 52 nm. Signal enhancement of 6 dB was measured for a 3.9-cm-long waveguide.**

***Index Terms*—Aluminum oxide, atomic layer deposition (ALD), erbium (Er), optical amplification, optical waveguides.**

I. Introduction

ERBIUM (Er)-doped optical waveguides offer a means for optical amplification or compensation for the losses present in passive integrated optical circuits. In addition to the flexible integration, planar technology can offer cost efficiency through mass production when compared to the fiber-optical amplifiers. Several different techniques have been used to produce Er-doped waveguides [1]–[5].

The cost-efficiency of the planar optical amplifiers is only achieved if large-area thin films can be grown with a sufficient uniformity and a precise thickness control. Atomic layer deposition (ALD), also known as atomic layer epitaxy, excellently addresses these issues. In ALD, the thin film is grown in a sequential manner. The deposition is based on surface reactions of the precursor gases, which are introduced in the deposition chamber one at a time. The process consists of a selected amount of reaction cycles and it allows basically a nanometer accuracy in the material growth control. Generally, the film is deposited conformally regardless of the surface shape. Temperature is kept relatively low during the growth, typically below 400 °C. Low processing temperature ensures that the thermally induced stress in the deposited film stack remains reasonably low.

A wide range of materials has been grown with ALD [6]. It is suitable for various applications and today it has also been adopted by large semiconductor manufacturers. In optical applications, ALD has been used since 1980 for depositing large-area electroluminescence-based thin-film displays [7]. It has also been used for preparation of dielectric multilayer structures for some basic optical components such as antireflection and high-reflection coatings, neutral beam splitters, and Fabry–Pérot filters [8]. Nonetheless, it has not been a common technique for fabricating integrated optical components. In this field, the excellent uniformity of ALD can offer a well-controlled device operation, e.g., in the phase sensitive devices. In addition to this, ALD offers a way to fabricate antireflective or reflective waveguide end coatings as well as to connect different waveguide sections with low loss, both these directly on a wafer level. This is possible due to the conformal growth of ALD. Since ALD has been used for over two decades for fabrication of electroluminescence-based displays, it is a natural step to investigate rare-earth doped ALD films also for other applications. In this letter, results on the ALD-grown Er-doped Al_2O_3 waveguides are presented. Aluminum oxide has been used as a host material for Er, because the ALD process for Al_2O_3 is well known and the Er solubility in Al_2O_3 is reasonable high.

II. Experiment

Ridge-type waveguides were formed on 2-μm-thick ALD-grown Al_2O_3 films on silicon substrate. A 5-μm-thick plasma-enhanced chemical vapor deposition (PECVD)-grown silica film was used as an under cladding. Er-doping was done by adding Er cycles between the Al_2O_3 cycles in the ALD process. The Er concentration was measured with X-ray fluorescence resulting in an average Er concentration of 2.3 wt %. The measurement method did not take into account the layered doping structure. The measured doping level corresponds to the Er ion concentration of 3.2×10^{20} cm^{-3} (assuming density of 4.0 g/cm^3).

For the ridge waveguide formation, a thin molybdenum (MO) film was sputtered as a hard mask for the Al_2O_3 etching. The Mo film was patterned with standard photolithography and wet etching in a commercial aluminum etchant (PS 70/10). The Al_2O_3 wet etching in 50% phosphoric acid at 75 °C for 7.5 min was followed in order to define the waveguide structure. This resulted in a ridge height of 390 nm as measured with a profilometer. After the resist removal the samples were immersed in NH_4OH–H_2O_2–deionized water solution to remove the Mo mask. No upper cladding was used on top of the waveguides. Finally, the waveguides were cleaved in order to perform the optical characterization.

The waveguide structure was selected to fulfill a single-mode operation, but it was not optimized for the low-loss fiber coupling. The realized waveguide structure was examined with an optical microscope and the measured dimensions were used for the mode-field simulations. The simulations were done with the TempSelene program, which uses the finite difference method.

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K. Solehmainen, M. Kapulainen, and P. Heimala are with VTT Information Technology, Microelectronics, FIN-02044 VTT Espoo, Finland (e-mail: kimmo.solehmainen@vtt.fi).

K. Polamo is with Planar Systems, Inc., FIN-02201 Espoo, Finland (e-mail: kirsi_polamo@planar.com).

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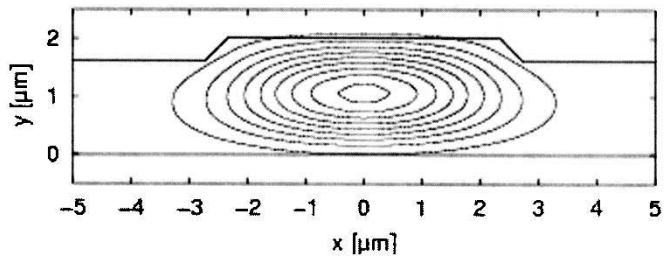

Fig. 1. Simulated cross-sectional power distribution of the fundamental TM mode for a nominally 6.0-μm-wide ridge-type waveguide. The ridge height is 390 nm. The contours are for normalized intensities 0.1, 0.2,. . ., and 0.9.

Resulting cross-sectional power distribution of the fundamental transverse magnetic (TM) mode for a nominally 6.0-μm-wide waveguide is shown in Fig. 1.

From the cleaved waveguides, optical transmission, emission, fluorescence lifetime, and signal gain characteristics were measured. The measured straight waveguide sample was 3.9 cm long. The width of the measured waveguide was 6.0 μm except in the emission spectrum and fluorescence lifetime measurements, where the waveguide width was 2.8 μm.

The polarization dependence of the transmission spectrum was measured, because it was observed that the waveguides were birefringent. In the measurement setup, the input light was butt-coupled into the waveguide with a single-mode polarization-maintaining fiber. The setup enabled the transmission measurement of both transverse electric (TE) and TM polarizations independently. The transmitted light was coupled into a multimode fiber and guided to an optical spectrum analyzer. The birefringence, i.e., the difference between the effective refractive indexes of TE and TM modes, of the waveguide was measured using the fixed analyzer method [9].

In the emission spectrum measurement, the Er ions in the waveguide were excited using a 980-nm pump source. Light from a 980-nm diode laser was coupled to the waveguide with a standard single-mode fiber. Backward-directed emission light was gathered back to the same fiber. A 1550/980-nm wavelength-division multiplexer (WDM) was used to filter the pump light from the emitted light before feeding the emitted light to an optical spectrum analyzer.

The fluorescence lifetime was measured with the same setup as the emission spectrum. The only differences were that the backward-directed emission light was fed to an InGaAs photodetector and the pump laser was modulated with a pulse generator. The electrical signal of the photodetector was measured with a digitizing oscilloscope. The fluorescence lifetime was defined as a time during which the emitted intensity from the waveguide dropped to 1/e of the initial intensity after the pump was switched off.

In the gain spectrum measurement, the waveguide was pumped with a 980-nm laser and the signal was provided by a tunable narrow-band laser. The signal and the pump light were combined with a 1550/980-nm WDM to a single-mode fiber, which was coupled to the waveguide input. Light from the waveguide output was coupled to a multimode fiber and measured with an optical spectrum analyzer.

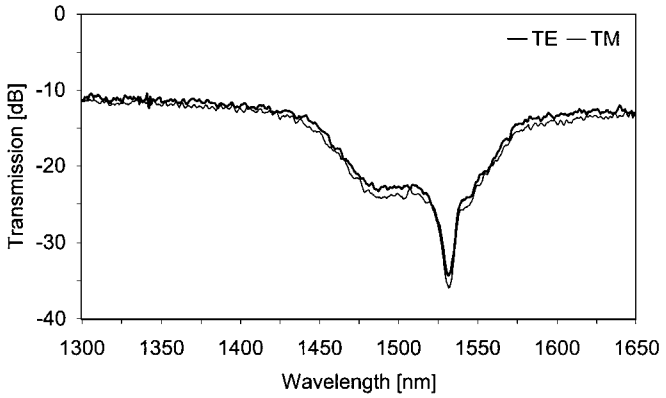

Fig. 2. Transmission spectra of a 3.9-cm-long Er-doped waveguide for TE and TM polarizations.

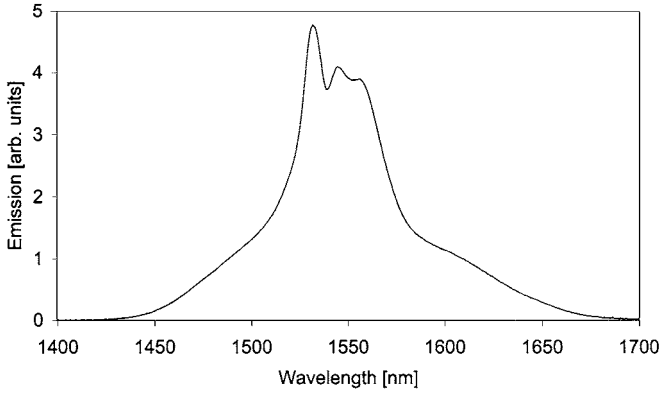

Fig. 3. Emission spectrum of an Er-doped waveguide. The FWHM of the spectrum is 52 nm.

III. Results and Discussion

Measured transmission spectra for both TE and TM polarizations of an Er-doped waveguide are shown in Fig. 2. The spectra show clearly the absorption due to the Er ions, the maximum being 6.1 dB/cm for TE and 6.4 dB/cm for TM at 1530 nm. The maximum absorption measured for nonpolarized light was 6.2 dB/cm. The birefringence of this waveguide around 1550 nm was measured as 0.004, which coincided with the simulated birefringence value for a corresponding waveguide structure. The birefringence can be lowered by modifying the waveguide structure. The background losses can be estimated from the transmission values around 1300 nm, where no Er-induced absorption occurs. In Fig. 2, the background losses are about 11 dB. According to the simulations, this figure contains 4.5 dB of fiber coupling losses. The rest consists of fiber misalignment and propagation losses. Since the wet etching does not increase the surface roughness of the waveguides considerably, the high propagation losses are expected to be caused by scattering in the material.

Fig. 3 shows the measured emission spectrum of an Er-doped waveguide. The pump power in the input fiber was 100 mW, of which about 35 mW reached the waveguide. The highest peak of the emission spectrum is around 1530 nm, followed by a broad emission shoulder from 1540 to 1560 nm. The full-width at half-maximum (FWHM) of the emission spectrum is 52 nm.

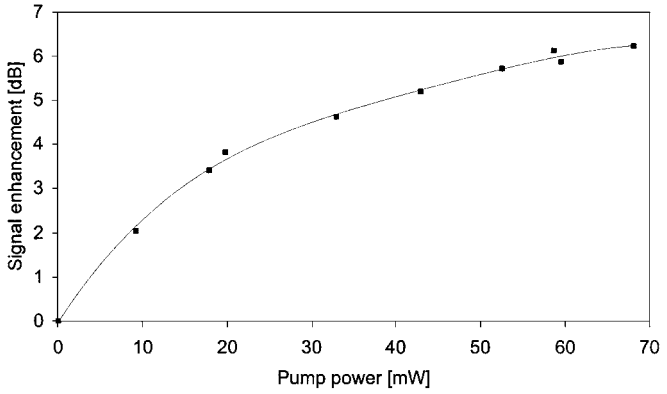

Fig. 4. Signal enhancement of an Er-doped waveguide as a function of the pump power at 1550-nm signal wavelength. The pump wavelength was 980 nm.

The broad emission spectrum is typical for Er-doped Al_2O_3 material, being broader than for Er-doped silica [10].

In the gain measurement, the absorption of the signal light competed with the stimulated emission and net optical gain was not reached. This indicates that the inversion of the Er ions was not sufficient. However, the signal at the output was clearly amplified when the pump was switched on. The ratio of the output signal with and without the pump power is commonly referred to as the signal enhancement. The signal enhancement at 1550 nm as a function of pump power is shown in Fig. 4. The pump power given in the figure indicates the optical power in the input fiber. The actual power in the waveguide is estimated to be 65% lower. As can be seen from the figure, the signal enhancement saturates to a level of about 6 dB when the pump power is increased.

The measured fluorescence lifetime of 0.9 ms verified the poor inversion of the Er ions. The short lifetime is most probably due to the inhomogeneous doping profile generated by the fabrication method. The pure Er layers between the Al_2O_3 layers with a locally high volume density of the Er ions cause the doping profile to be inhomogeneous. This is expected to increase the cooperative upconversion of the Er ions, especially if ions in the Er layer are clustered [11]. The spreading of the doping profile would most likely increase the fluorescence lifetime and enable net optical gain in these waveguides. This is hard to realize with annealing because the diffusivity of the Er ions in Al_2O_3 is low. However, the spreading of Er ions within a single doping layer by codoping (e.g., with ytterbium) or by using other elements to adjust the Er ion density within a single layer in the ALD process should be fully examined to improve the lifetime characteristics.

IV. Conclusion

In this letter, the fabrication of Er-doped Al_2O_3 waveguides using ALD was demonstrated. The ridge-type waveguides were processed on a silicon substrate with a PECVD silica buffer layer. The measured waveguides showed a broad emission spectrum with FWHM over 50 nm and strong Er-induced absorption, the maximum being 6.2 dB/cm for nonpolarized light. The birefringence of the measured waveguide was 0.004. The birefringence influenced only moderately on the polarization dependence of the optical transmission. Signal enhancement saturated to about 6 dB for a 3.9-cm-long waveguide. To reach a net optical gain, the doping process needs further development to realize a more uniform doping profile throughout the Er-doped active layer.

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Author(s)
Solehmainen, Kimmo

Title

Fabrication of microphotonic waveguide components on silicon

Abstract

This thesis reports on the development of silicon-based microphotonic waveguide components, which are targeted in future optical telecommunication networks. The aim of the work was to develop the fabrication of silicon microphotonics using standard clean room processes which enable high volume production. The waveguide processing was done using photolithography and etching. The default waveguide structure was the rib-type, with the waveguide thickness varying from 2 to 10 µm. Most of the work was done with silicon-on-insulator (SOI) wafers, in which the waveguide core was formed of silicon. However, the erbium-doped waveguides were realised using aluminium oxide grown with atomic layer deposition. In the multi-step processing, the basic SOI rib waveguide structure was provided with additional trenches and steps, which offers more flexibility to the realisation of photonic integrated circuits.

The experimental results included the low propagation loss of 0.13 and 0.35 dB/cm for SOI waveguides with 9 and 4 µm thicknesses, respectively. The first demonstration of adiabatic couplers in SOI resulted in optical loss of 0.5 dB/coupler and a broad spectral range. An arrayed waveguide grating showed a total loss of 5.5 dB. The work with SOI waveguides resulted also in a significant reduction of bending loss when using multi-step processing. In addition, a SOI waveguide mirror exhibited optical loss below 1 dB/90° and a vertical taper component between 10 and 4 µm thick waveguides had a loss of 0.7 dB. A converter between a rib and a strip SOI waveguides showed a negligible loss of 0.07 dB. In the Er-doped Al_2O_3 waveguides a strong Er-induced absorption was measured. This indicates potential for amplification applications, once a more uniform Er doping profile is achieved

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Tekijä(t)
Solehmainen, Kimmo

Nimeke

Piipohjaisten mikrofotoniikan valokanavakomponenttien valmistus

Tiivistelmä

Tässä väitöskirjatyössä kehitettiin piipohjaisia mikrofotoniikan valokanavakomponentteja, jotka on tarkoitettu käytettäväksi tulevaisuuden optisissa tietoliikenneverkoissa. Työn tavoite oli kehittää piipohjaisen mikrofotoniikan valmistusta käyttäen yleisesti käytössä olevia puhdastilaprosesseja, jotka mahdollistavat suuret valmistusmäärät. Valokanavien valmistuksessa käytettiin fotolitografiaa ja syövytystä. Valokanavat olivat perusrakenteeltaan harjannetyyppiä, ja niiden paksuus vaihteli kahdesta kymmeneen mikrometriin. Suurin osa työstä tehtiin välioksidoiduilla piikiekoilla (silicon-on-insulator, SOI), jolloin valokanava muodostui piistä. Erbiumilla seostetut valokanavat tehtiin sen sijaan alumiinioksidiin, joka oli valmistettu atomikerroskasvatuksella. Moniporrasprosessoinnissa SOI-harjannevalokanavan perusrakenteeseen lisättiin ylimääräisiä uria, joiden ansiosta valosignaalin ohjaukseen perustuvien integroitujen piirien toteutus muuttuu joustavammaksi.

Kokeellisiin tuloksiin kuuluivat alhainen etenemishäviö 9 ja 4 µm:n paksuisilla SOI-valokanavilla, joiden häviöiksi mitattiin 0,13 ja 0,35 dB/cm. Ensimmäisillä SOI-valokanaviin valmistetuilla adiabaattisilla optisilla tehonjakajilla saavutettiin 0,5 dB:n optinen häviö komponenttia kohden sekä laaja aallonpituusalue. Optiselle aallonpituusjaotinkomponentille mitattiin 5,5 dB:n häviö. SOI-valokanavilla saavutettiin myös merkittävä kaarroshäviön pieneneminen käyttäen moniporrasprosessointia. SOI-rakenteeseen perustuvan valokanavapeilin optinen häviö oli alle 1 dB/90°. 10 ja 4 µm:n paksuisten valokanavien välille tehdylle liitoskomponentille mitattiin puolestaan 0,7 dB:n häviö. Komponentti, joka muunsi harjannetyypin SOI-valokanavan suorakulmaiseksi valokanavaksi, aiheutti vähäpätöisen, 0,07 dB:n suuruisen häviön. Erbiumilla seostetuista Al2O3-valokanavista mitattiin voimakas erbiumin aiheuttama absorptio. Tämä viittaa mahdollisuuksiin valokanavavahvistimien tuottamisessa, kunhan saavutetaan tasaisempi erbiumin seostusprofiili.

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