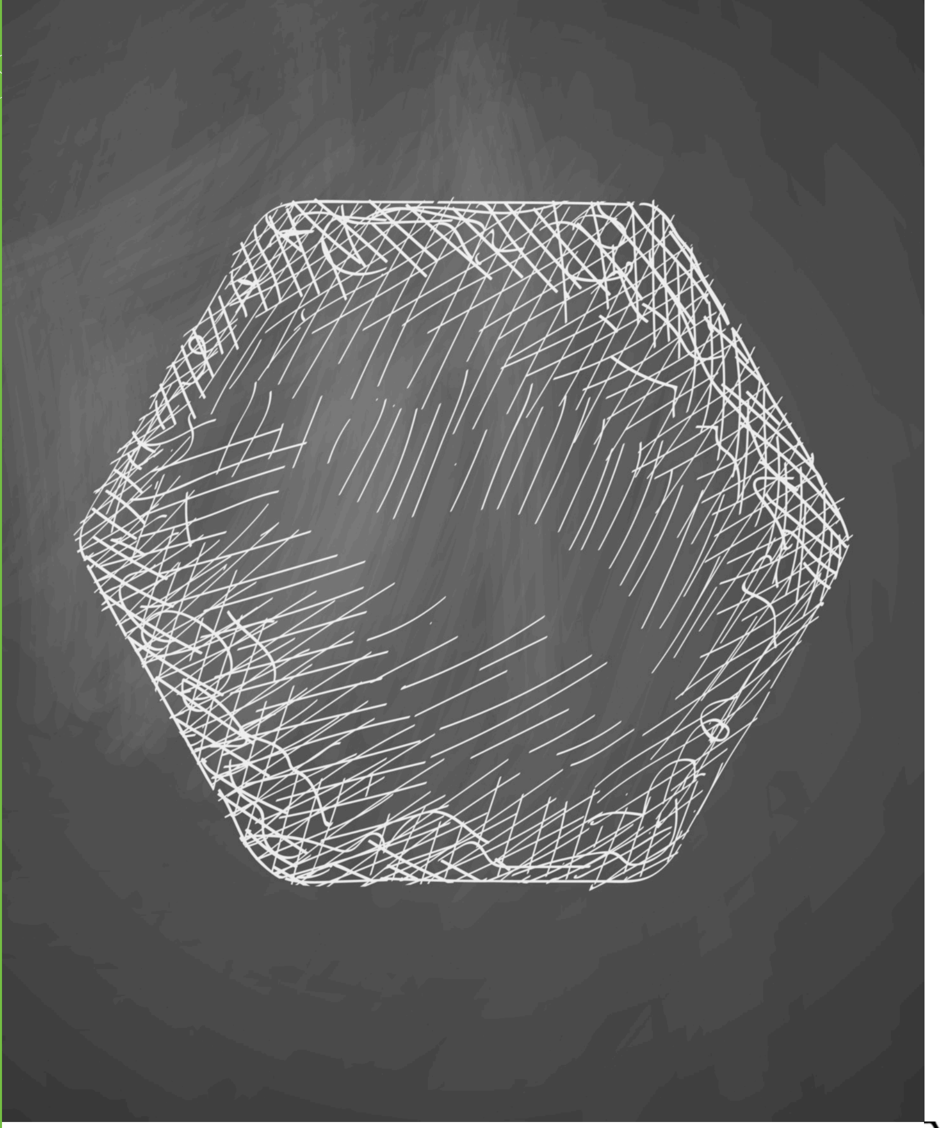

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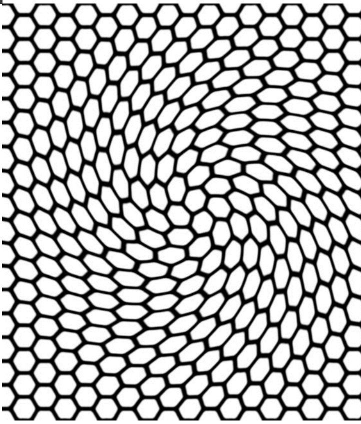
Integration of 2D and 3D nanostructure fabrication with wafer-scale microelectronics

Photonic crystals and graphene

Sanna Arpiainen



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Integration of 2D and 3D nanostructure fabrication with wafer-scale microelectronics

Photonic crystals and graphene

Sanna Arpiainen

Senior Scientist, PhD candidate

A doctoral dissertation completed for the degree of Doctor of Science (Technology) to be defended, with the permission of the Aalto University School of Science, at a public examination held at the lecture hall F239a of the school on 24 July 2015 at 12.

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PREFACE

This text is a compendium of research aiming towards integration and large scale fabrication of promising nanoscale structures and materials in a form of PhD thesis. The work has been conducted over more than ten years and the world has changed as well as the understanding of the prospects of the once novel technologies, but the basic problems and processes have still remained the same.

The nanostructures and materials considered are photonic crystals and graphene. In photonic crystal research, the role of the author was to develop waveguide materials and 2D and 3D photonic crystal fabrication and integration with the conventional waveguides in photonic circuits. For the research done in these topics, whether included in these thesis or not, the author would like to thank Jouni Ahopelto, Harri Lipsanen, Clivia Sotomayor-Torres and Fredrik Jonsson for initial research ideas; James Dekker, Antti Säynätjoki, Timo Aalto, Martin Kulawski, Tapio Mäkelä, Mikael Mulot, Jianhui Ye and Gudrun Kocher for their help in process and component design; Markku Kapulainen, Worawut Khunsin, Klas Lindfors, Esa Räikkönen and Amit Khanna for their contribution in the measurements; Karri Varis and Kevin Vync for simulations; Merja Markkanen and Teija Häkkinen for processing – and Martti Blomberg for teaching what is important in process design and silicon deposition

In graphene related activities, the author has guided the research trough different graphene fabrication methods towards application development. Also this work would have been impossible without generous help and valuable contribution of colleagues. Jani Kivioja, Mika Prunnila, Harri Lipsanen, Jouni Ahopelto and Päivi Laaksonen reserve thanks for many of the research ideas; David Gunnarsson, Andrey Shchepetov, Markku Kainlauri, James Dekker, Tomi Haatainen, Olli Svensk, Wonjae Kim, Changfeng Li, Juha Riikonen, Miika Soikkeli, Katri Kurppa, Marika Ekroos, Martin Kulawski, Tapio Mäkelä, Markku Kapulainen, Jaakko Salonen, Matteo Cherchi and so many others have contributed in this and related work in numerous ways.

As it is customary to thank also the sister's cat for support without which the work would not have been possible, the author wants to thank her daughter for delaying the accomplishment by being the most important and adorable accomplishment anyone can hope for and her spouse for forcing her to accomplish this now.

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LIST OF PUBLICATIONS

This thesis is based on the following original publications which are referred to in the text as I–VIII. The publications are reproduced with kind permission from the publishers.

I M. Soikkeli, K. Kurppa, M. Kainlauri, S. Arpiainen, A. Paananen, D. Gunnarsson, J. Joensuu, P. Laaksonen, M. Prunnila, M. Linder and J. Ahopelto, “Graphene biosensor programming with genetically engineered fusion protein monolayers”, submitted. 4 pages.

II J. Riikonen, W. Kim, C. Li, O. Svensk, S. Arpiainen, M. Kainlauri and H. Lipsanen, “Photo-Thermal Chemical Vapor Deposition of Graphene on Copper”, Carbon 62, 43–50 (2013).

III D. Naumenko, V. Snitka, B. Snopok, S. Arpiainen and H. Lipsanen, “Graphene-enhanced Raman imaging of TiO_2 nanoparticles”, Nanotechnology 23 (46), 465703 (7 pages) (2012).

IV S. Arpiainen, K. Vynck, J. Dekker, M. Kapulainen, W. Khunsin, T. Aalto, M. Mulot, G. Kocher, R. Zentel, C. Sotomayor Torres, D. Cassagne and J. Ahopelto “Self-Assembled Three-Dimensional Inverted Photonic Crystals on a Photonic Chip”, to be submitted. 4 pages.

V S. Arpiainen, F. Jonsson, J.R. Dekker, G. Kocher, W. Khunsin, C.M.S. Torres and J. Ahopelto, “Site-Selective Self-Assembly of Colloidal Photonic Crystals”, Adv. Funct. Mater. 19 (8), 1247–1253 (2009).

VI M. Mulot, A. Säynätjoki, S. Arpiainen, H. Lipsanen and J. Ahopelto, “Slow light propagation in photonic crystal waveguides with ring-shaped holes”, Journal of Optics A: Pure and Applied Optics 9 (8), S415–S418 (2007).

VII J.H. Ye, R. Zentel, S. Arpiainen, J. Ahopelto, F. Jonsson, S.G. Romanov and C.M.S. Torres, “Integration of self-assembled three-dimensional photonic crystals onto structured silicon wafers”, Langmuir 22 (17), 7378–7383 (2006).

VIII K. Varis, M. Mattila, S. Arpiainen, J. Ahopelto, F. Jonsson, C.M. Sotomayor-Torres, M. Egen and R. Zentel, “Reflection of focused beams from opal photonic crystals”, Optics Express 13 (7), 2653–2667 (2005).

AUTHOR'S CONTRIBUTIONS

I Graphene biosensor programming with genetically engineered fusion protein monolayers

Author's contribution was to define the requirements for the biological model system to be studied, to assist in the graphene sensor fabrication process, to define the principles of the ionic screening in protein layer and to write most of the manuscript.

II Photo-Thermal Chemical Vapor Deposition of Graphene on Copper

Author's contribution was to develop the photo-thermal CVD process on copper and to participate in the writing of the manuscript. Author published the initial results, without electrical characterization, in Graphene 2011 conference.

III Graphene-enhanced Raman imaging of TiO_2 nanoparticles

Author's contribution was to fabricate the substrates and to participate in the analysis of the results and in writing of the manuscript.

IV Self-Assembled Three-Dimensional Inverted Photonic Crystals on a Photonic Chip

Author's contribution was to design and fabricate the samples and to develop the fabrication processes, to design and perform the measurements and analysis and to write the manuscript.

V Site-Selective Self-Assembly of Colloidal Photonic Crystals

Author's contribution was to design and fabricate the samples and to develop the fabrication process, to design and perform the measurements and analysis and to write the manuscript.

VI Slow light propagation in photonic crystal waveguides with ring-shaped holes

Author's contribution was to develop the process for 2D photonic crystal integration on pre-patterned thin SOI waveguides with low alignment accuracy EBL tool and to prepare the MIT photonic bands software with input files suitable for 2D photonic crystal and waveguide calculations.

VII Integration of self-assembled three-dimensional photonic crystals onto structured silicon wafers

Author's contribution was to prepare the substrates and to participate in the writing of the manuscripts.

VIII Reflection of focused beams from opal photonic crystals

Author's contribution was to present the problem, help to formulate the problem on a codable form, to prepare samples for testing the code performance and to contribute to writing of the manuscript.

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ABSTRACT

TIIVISTELMÄ

LIST OF SYMBOLS

a	amorphous, lattice constant
c	speed of light
λ	wavelength
H, h	height
h	hexagonal
κ	extinction coefficient
n	refractive index
n_1, n_0	mode refractive index
n_{imp}	impurity concentration
ϕ	diameter
R, R_0	resistance
R_S	sheet resistance
θ	angle
ν_F	Fermi velocity
W	width

LIST OF ABBREVIATIONS

5N	99.999 % purity
AFM	atomic force microscope
ALD	atomic layer deposition
BHF	buffered HF
BiSFET	bilayer pseudospin field effect transistor
BOX	buried oxide
CDSA	capillary driven self-assembly
CCD	charge-coupled device
CNT	carbon nanotube
CVD	chemical vapour deposition
DLC	diamond like carbon
EBL	electron beam lithography
FWHM	full width at half maximum
fcc	face centered cubic
FET	field effect transistor
GFET	graphene field effect transistor
GO	graphene oxide
hcp	hexagonal close packed
HFBI	hydrophobin I
high-k	high dielectric constant
HMDS	hexamethyl disilazane [$C_6H_{19}NSi_2$]
HOPG	highly oriented pyrolytic graphite
HSQ	hydrogen silsesquioxane
ICP	inductively coupled plasma
IgG	Immunoglobulin
IPA	isopropyl alcohol
ITO	indium tin oxide
LED	light emitting diode
LNA	low noise amplifier

LPCVD	low pressure chemical vapour deposition
MEMS	microelectromechanical system
NA	numerical aperture
NIR	near infrared
NMP	n-methyl-2-pyrrolidone [C_5H_9NO]
OLED	organic light emitting diode
OSA	optical spectrum analyzer
PECVD	plasma enhanced chemical vapour deposition
PET	polyethylene terephthalate [$(C_{10}H_8O_4)_n$]
PhC	photonic crystal
PMMA	poly(methyl methacrylate) [$(C_5O_2H_8)_n$]
PoC	point-of-care
PSG	phosphosilicate glass
PT-CVD	photo-thermal chemical vapour deposition
Q-switch	variable attenuator
RF	radio frequency
RCA1	ammonia-peroxide based semiconductor cleaning bath
rGO	reduced graphene oxide
RH	relative humidity
RTP	rapid thermal processing
SEM	scanning electron microscope
SO	surface optical (phonon)
SOI	Silicon-on-Insulator
TEM	transmission electron microscope
TFSA	trifluoromethanesulfonic acid [CF_3SO_3H]
TMA	trimethylaluminum [$C_6H_{18}Al_2$]
UHV	ultrahigh vacuum
UV	ultraviolet
XPS	x-ray photoelectron spectroscopy
Z_E, Z_R	zipper peptides

1 INTRODUCTION

New materials require new approaches. Road from research to technology can be hard, as the materials, dimensions and fabrication technologies used in research are often not suitable for large scale fabrication. Controlled positioning of the nano-objects with conventional electronic and photonic circuits can require manipulation of the nanostructure fabrication techniques, surface adhesion properties and rethinking of the whole device fabrication sequence. In this work this problem is addressed in several different cases, ranging from the integration of 3D photonic crystals into silicon waveguides to large scale graphene deposition, processing on silicon and plastic substrates & integration with biomolecules.

1.1 ROUTES TO INTEGRATION

Utilization of novel materials and structures in real microelectronics and photonics applications requires integration with the conventional platform. Because the fabrication processes of the conventional circuitries are optimized for the traditional materials and generally require both high thermal budget and purity, the novel elements need to be integrated and aligned with the pre-existing structures on the substrate. For that, there are basically three alternatives; (i) self-assembly, (ii) high precision placement and (iii) methods related to the traditional thin film growth and lithographic definition of the nanostructure.

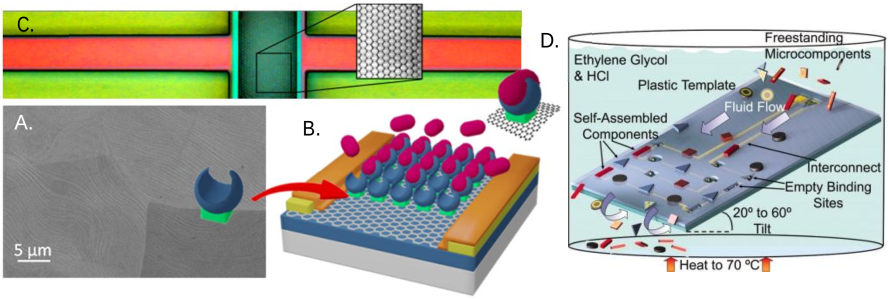

FIGURE 1.1 Examples of self-assembly at different length scales. A) Growth of a crystalline lattice, for example graphene on a catalytic surface, is self-assembly on atomic scale. [II] B) Biomolecule self-assembly on graphene, size of the biomolecules is measured in nanometers. [I] C) Capillary self-alignment of 3D opals from micron sized particles [V] and D) chip self-assembly with tens of micron objects[1].

Self-assembly is the most controversial of the assembly methods. It has a large potential in the scale up of the integration process, as it is based on the universal utilization of microfluidic, chemical or biological interactions but, at the same time, it can be very sensitive for variations of the system and thus prone to misalignment and failure. Self-assembly can be employed both in the formation of the nanostructured objects and in the micron scale integration of different objects to a template. As an example of the latter is the ability of specifically shaped droplets to sort, pick and align microchips with up to 100 µm in size[1] which also presents the upper limit of self-assembly with respect to the object size. In this thesis the special cases of opal formation in a microfluidic process [V] and the formation of heterogeneous protein monolayer [I] are addressed. In both cases the directed self-assembly process is utilized to form the desired structure directly on the microphotonic or -electronic template.

Precision placement and high resolution 3D structuring form the other class of integration technologies. The precision placement has rather poor scalability but much higher reliability than the self-assembly. The scalability limit is reached even in the lowest resolution variations of these technologies, such a flip-chip bonding and pick & place tools where the adequate physical precision in placement and speed of the process are often achieved by adding a component of self-assembly, e.g. in a form of melted metal droplet mediated alignment. Ultra high precision robotic instruments and e.g. scanning probe microscopy based nanomanipulation methods reaching single atom accuracy can mainly be used in realizing physical experiments, including device prototyping and analysis.

An emerging method in this group is 3D printing which at high resolution applications is based on confocal lithography and two-photon absorption. The prospects of the method lie particularly in the customization and in the high degree of freedom it gives for the geometry of the structure. Alike other high precision technologies, it also suffers from limited scalability, but can nevertheless find its place in the production chain of strategic components. And even though the material selection is restricted by the process chemistry to special polymers, combination with atomic layer deposition allows the construction of even metallic 3D structures.

The traditional mass production of microelectronics and –photonics relies on thin film growth and patterning, which are wafer level processes. The technology is based on a variety of physical and chemical deposition methods, patterning with photoresists and subsequent selective wet and plasma etching processes to transfer the pattern into the films. This approach, sometimes referred to as top-down, is the basis behind the modern information society. The same principles are also applied in the production microelectromechanical systems (MEMS), which are basically 3D devices, but designed to be fabricated by 2D processes.

Nanoscale dimensions have become the mainstream in microelectronics by the increasing integration density and the highest resolution patterning based on deep-UV immersion lithography, reaching sub 30 nm linewidths, is currently in use at the few sites where microprocessor and memory chips are manufactured. These small dimensions, however, are based on carefully optimized design and utilization of all possible tricks. For research, more general methods such as electron beam exposure and nanoimprint lithography have been developed for miniaturization. Another trend is in roll to roll production, based on the same principles in structuring, but with focus on low cost and flexibility instead of the integration density.

The integration of 2D photonic crystals discussed in this thesis is an example of this traditional fabrication method based on lithography. Also graphene components are fabricated with conventional lithographic methods, after the sheet is first deposited and transferred on a conventional substrate. The two dimensional structure of a single graphene sheet is actually one of the major benefits of graphene in comparison to one dimensional carbon nanotubes (CNTs) and increases the prospects of graphene over those of CNTs despite the lack of electronic band gap that is a major drawback when considering digital electronics applications.

2 PHOTONIC CRYSTAL INTEGRATION

Photonic crystal is a 1, 2 or 3-dimensional periodic lattice of diffractive elements where photons are subject to constructive and destructive interferences that can limit the propagation of light at some frequency bands. 1D photonic crystals are Bragg gratings such as periodic grooves or thin film multilayers that can act as mirrors for some frequencies, typically optimized so that the optical thickness of each film is ¼ λ of the reflected wavelength. 2D photonic crystals are planes with a periodic array of holes or rods, where the light propagation is prohibited at some finite frequency band in all directions parallel to the plane. 3D photonic crystals equivalently prevent the light propagation in all directions.

Photonic crystal waveguides are lines of defects generated into 2D and 3D crystals that allow light propagation with a speed defined by the lattice properties. Typically this speed is much less than the speed of light in solid materials, allowing strongly enhanced light-matter interaction. The reduced speed and increased interaction can also be considered as a result of multiple reflections required to propagate inside the photonic crystal material. The ability to guide light (theoretically) without dissipation along the defects has potential in reducing the footprint of integrated optics by allowing abrupt bends and the increased light-matter interaction can provide means to enhance nonlinear optical phenomena in signal processing, generation and transformation.

For practical applications, the photonic crystals generally have to be integrated with conventional waveguides. The challenges in integration are related to mode and impedance matching between different types of waveguides and into the development of scalable fabrication technologies. In the following, the waveguide types and materials used in this thesis in Publications IV–VI are presented. The relatively straightforward integration of 2D photonic crystals is reviewed only shortly, with more focus on the 3D crystal integration and inversion.

2.1 SILICON WAVEGUIDES

Silicon waveguides are an ideal platform for optical information processing at telecommunication wavelengths (around 1550 nm) defined by the transmission properties of glass fibres carrying the information. Waveguiding in silicon relies on the low absorption and high index of refraction ($n = 3.5$) enabling large index contrast with the environment, which is typically a ceramic cladding ($1 < n < 2$). This allows to confine the light beam into a relatively small cross section waveguide core and to bend the trajectory of the beam without significant losses. When considering silicon as a tool for all optical data processing, there are, however, many challenges to overcome. For example, the indirect band gap does not allow lasing and thus requires heterogeneous integration of compound semiconductor light sources.

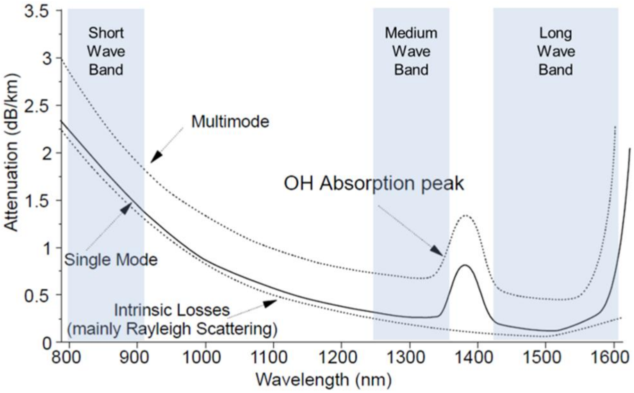

FIGURE 2.1 Bands relevant for optical telecommunications are determined by attenuation in photonic fibers. Short wave band relates to the fiber attenuation minimum in the early generation of optical fibres.[2]

Silicon waveguides operate at wavelengths above the absorption band of 1.1 µm (energies below 1.1 eV) defined by the silicon band structure. Undoped single crystalline silicon is transparent at wavelengths between 1.1 µm and 6.5 µm (extinction coefficient $\kappa < 10^{-6}$), but doped silicon can have significant attenuation due to the free electron absorption. Silicon waveguides can be based on different qualities of silicon from amorphous to single crystalline and on different principles of light confinement. In this thesis, the optical properties of amorphous, polycrystalline and single crystalline silicon are in a crucial role also as the photonic crystal material. With regards to waveguide geometry, both thin silicon strip waveguides and thick rib waveguides are considered.

2.1.1 SILICON STRIP WAVEGUIDES

Strip waveguides are the most common template for integrated silicon photonics. They require high quality SOI substrates with 200–300 nm thick SOI film, but due to their small volume, they can be controlled by an external electric field to provide functionalities such as fast switching based on free electron absorption. In the case of photonic crystal integration, the thin strip waveguides are ideal with respect to the geometry and the mode size for coupling with 2D PhC waveguides. Both the strip waveguides and the 2D PhCs are generally fabricated by etching through the thin silicon slab. Guiding in the strip waveguides is based on a large contrast index between the core and the cladding and the single mode operation on the physical dimensions being too small for the existence of higher order modes.

The width of the strip waveguides used in the research relevant to this Thesis for e.g. accessing the 1 and 2D PhCs varied from 1 µm to 10 µm.[3,4] [VI] Such waveguides can accommodate several propagating light modes and a single mode input beam coupled from tapered single mode fiber to the waveguide decays rapidly to a large variety of coexisting modes along with the mode propagation.

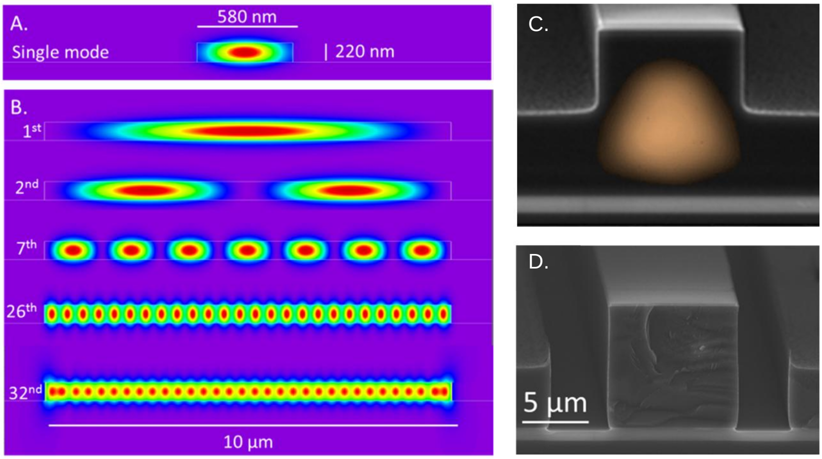

FIGURE 2.2 A) Single mode strip waveguide and the mode intensity profile. The propagation of higher order modes is limited by the size of the waveguide. B) A 10 µm wide strip waveguide and some mode intensity profiles. Such a wide waveguide can support up to 32 TE modes.[5] C) SEM image of a single mode rib waveguide cross section and the mode intensity profile measured from similar waveguide end with CCD camera. The first order optical mode (orange colour) is positioned into the waveguide core on a manner illustrated in the image, whereas the higher order modes propagate and decay in the lower part of the waveguide. D) Large strip waveguide supporting a multitude of TE and TM modes.

2.1.2 SINGLE MODE SILICON RIB WAVEGUIDES

Rib waveguides differ from the strip waveguides by the fundamental principle of guiding. The waveguide core is not defined by etching through the SOI film, but only the guiding rib is defined at the top of the SOI film. In principle the rib waveguides allow the existence of all modes, but guiding of only the fundamental mode is supported by the rib, whereas all higher order modes decay.

In order to obtain single mode guiding, the width W of the waveguide can be determined from the Soref's width limit[6]

$$W < 0.3H + \frac{h}{\sqrt{1-\left(\frac{h}{H}\right)^2}}, \tag{2.1}$$

where H is the height of the waveguide core and $(H - h)$ is the etch depth. This formula is invariably valid for $h \geq 0.5\,H$,[6] but can be extended to approximately $0.45\,H$ at $H = 10\ \mu m$.[7] Attenuation values below 0.2 dB/cm have recently been measured on similar ridge waveguides.[7]

The intensity distribution of the mode propagating in the ridge waveguide is slightly non-symmetric, as shown in FIGURE 2.2. If that is considered as a disadvantage, or when light propagation is to be manipulated by on chip mirrors, the waveguide can be transformed into a large strip waveguide with symmetric, circular mode profile. Large straight multimode waveguides can maintain single mode propagation over long distances, as long as the transition from rib to strip is adiabatic and there is no scattering due to surface roughness or material inhomogeneities.

2.1.3 CRYSTALLINE, POLYCRYSTALLINE AND AMORPHOUS SILICON

Crystalline silicon waveguides are fabricated on silicon-on-insulator (SOI) wafers, consisting of a thin crystalline silicon (or SOI) layer and buried oxide (BOX) insulator on thick silicon handle wafer. The SOI wafers are available for electronics and photonics with different characteristics and fabrication technologies. Photonics applications typically have very stringent requirements for the SOI thickness variations and interface quality, and the wafers can be rather expensive. The fabrication process typically includes SOI film generation from bulk silicon with e.g. hydrogen bombardment, delamination, transfer and polishing steps.

Single crystalline silicon waveguides rely on SOI wafers based on wafer scale bonding and thinning techniques. Wafers with thin (200–300 nm) high quality SOI film on thick (2–3 µm) SiO_2 insulator (buried oxide, BOX) are extremely costly, not only because of the low tolerances set by the strip waveguides with respect to the thickness variations. SOI films with micron scale thickness are more economical and applicable for the rib waveguides.

In order to reduce the cost, thin SOI can also be produced from amorphous and polycrystalline silicon, but this requires addressing the absorption due to dangling bonds in the amorphous silicon and in the grain boundaries of the polycrystalline silicon, and the light scattering from those grain boundaries.

Polycrystalline silicon can be deposited directly on the insulator with e.g. low pressure CVD (LPCVD). In general, the direct deposition of polycrystalline silicon is done at temperatures around 700 °C and provides material with highly absorbing grain boundaries unsuitable for photonic applications. Better optical quality can be obtained by plasma enhanced chemical vapour deposition (PECVD) of amorphous silicon at 580 °C, followed by annealing at 600 °C to gently crystallize the silicon. The attenuation constant can be further decreased by subsequent annealing at 1100 °C.[8] With this method we have obtained loss of 11 dB/cm, from which the estimated contribution of 7 Å surface roughness was roughly 5 dB/cm.[9] The material absorption is thus rather significant, as the attenuation measured from similar SOI waveguides was only 2 dB/cm. The same LPCVD process can also be optimized to allow conformal deposition so that the SiH_4 decomposition occurs only at the surfaces, thus providing the means required for the inversion of the 3D photonic crystals.

Amorphous silicon has high absorption due to the dangling bonds, but when those are properly terminated with hydrogen (*a*-Si:H), the material provides an economic and feasible alternative for commercial SOI wafers. Hydrogenated amorphous silicon can be deposited at low temperatures with PECVD or with any other low-temperature CVD process capable for silicon dioxide (SiO_2) deposition from silane. Due to the relatively conformal low temperature process, typically from 120 °C to 250 °C, *a*-Si:H waveguides can be deposited and patterned on top of pre-processed components with existing surface topology and low thermal budget. We obtained the best transmission characteristics with 20 W plasma power at 200 mTorr pressure with 75 sccm silane flow, resulting in a surface roughness of 2.5 Å at 170 nm thickness. The waveguides were patterned with optical cavities defined by 1D Bragg gratings as described in the next chapter. The attenuation obtained without gratings was 3–4 dB/cm and when extracted from the Fabry-Pérot oscillations, the estimated attenuation was 1.5 dB/cm with upper limit of 5.3 dB/cm.[3]

2.2 INTEGRATION OF 1D AND 2D PHOTONIC CRYSTALS

1D and 2D photonic crystals provide additional tools for modifying the flow and properties of light in waveguides. 1D photonic crystals, or Bragg gratings, act as mirrors with transmission and reflection characteristics defined by the number and properties of grooves in the grating. 2D photonic crystals are generally considered as the building blocks of 2D photonic crystal waveguides, where the flow of light in lateral dimensions is prohibited by the lattice of holes and allowed only along the line of missing holes called defects. These are analogous to defects inside the electronic gap in semiconductors, providing allowed energy states inside otherwise forbidden energy region. When these states from the neighboring defects overlap in the momentum space, they form bands that allow transport between the defect states. As the guiding is based on well-defined defect band located within an otherwise forbidden zone, the path can include tight and abrupt bends without losses, provided the light does not escape from the plane.

In analogy to the dispersion relation, the photonic band structure modifies the group velocity of light also within allowed frequencies. As the control of light is essentially based on multiple reflections, the group velocity of a mode traveling in the defect line is much slower than in conventional waveguides. This provides means for increased light-matter interactions and allows utilizing weak non-linear effects. However, the increased light-matter interaction also increases the requirements for material quality and surface smoothness.

Even though the material requirements are easier to understand by considering the system via multiple reflections, the operation principles of the crystal are based on wave interferences and can be modelled with Maxwell’s equations. In this thesis the PhC modelling was carried out with MIT Photonics-Bands,[10] which is a freely available software package. There the fully-vectorial eigenmodes of Maxwell's equations with periodic boundary conditions are computed in a planewave basis. The software gives full freedom for the generation of the unit cell of the photonic crystal and is able to calculate the band structure for the extraction of parameters such as group velocity determined from the dispersion relation. The software was used as a design tool to optimize the dimensions of the 2D and 3D photonic crystals.

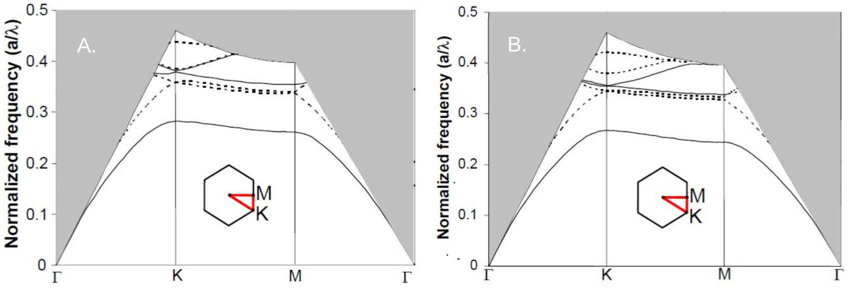

FIGURE 2.3 Photonic dispersion relation of 2D photonic crystal with a) ring shaped holes (ring radius 0.28*a*, width 0.16*a*) and b) conventional empty holes (radius 0.3*a*).[11] Silicon slab thickness 0.5*a*. Photonic band gap in both lattices is roughly at 0.28–0.32 *a*/λ.

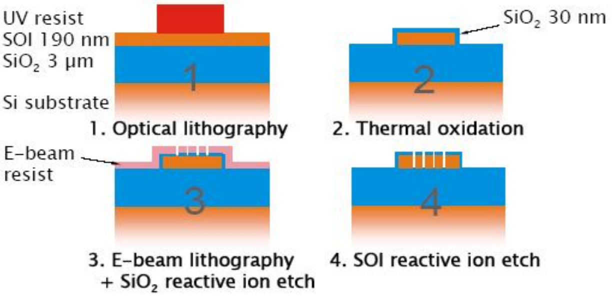

FIGURE 2.4. Main steps of the fabrication process of a PhC waveguide.

The main steps of the fabrication process are illustrated in FIGURE 2.4. The photonic crystals were patterned with electron beam lithography (EBL), as their dimensions are too small to be defined with standard UV lithography. However, the size of the writing field in electron beam lithography was small and in the absence of laser stage, the stitching error was too large as to allow for the definition of the whole photonic chip with EBL. Therefore, in order to be able to characterize the transmission properties the PhC waveguides, they had to be fabricated in wide prepatterned conventional strip waveguides (FIGURE 2.5A). The small writing field also limited the length of the PhC to about 100 µm, as the alignment with the waveguides and adiabatic tapering from wide waveguide to narrow photonic crystal waveguide had to be defined into the same writing field. The length required for the adiabatic taper must be defined so that the angle θ is kept smaller than the adiabatic limit, which can be defined from Bookham's condition

$$\theta \leq \frac{W(n_1 - n_0)}{2\lambda}, \qquad (2.2)$$

where W is the width of the waveguide and n_1 and n_0 the effective refractive indices for the neighboring modes.

1D photonic crystals are used mainly as mirrors for example to form a Fabry-Pérot cavity[12,13] into the waveguide. Multiple reflections inside the cavity with well-defined length allows direct measurement of the propagation losses and group velocities in the waveguides, which we have employed to compare the properties of strip waveguides fabricated on commercial SOI wafers and on experimental polysilicon and *a*-Si:H films deposited on thick insulator.[3] The same method we employed in the definition of the properties of 2D photonic crystal waveguides.[4] The small length of the PhC waveguides, the non-reproducible coupling loss into the sample and the reflections at the waveguide interfaces make conventional transmission measurements impossible to interpret on a reliable manner. The measured loss of the PhC waveguide was 3–8 dB/mm and the total loss over the PhC section was less than 0.3 dB.[4]

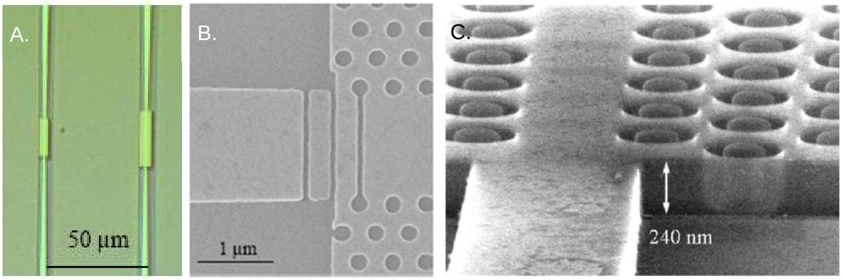

FIGURE 2.5 A) Optical micrograph of PhC waveguides inserted between conventional strip waveguides. A taper is necessary to bring the light from the 5–8 µm wide strip waveguides into the 1.2 µm wide PhC waveguide. B) SEM image of the PhC waveguide cavity end with a triple-groove mirror[4] on and D) of a PhC waveguide defined with ring-shaped holes. [VI] © Mikael Mulot

2.3 INTEGRATION OF 3D PHOTONIC CRYSTALS

Three dimensional photonic crystals (3D PhCs) with optical cavities have been considered to bear large potential in optical signal processing and detector applications as they combine the increased light-matter interaction, cavity resonance modes, photonic band edge frequency and large void space of the porous 3D network. However, the challenges in both the integration of the 3D PhCs into photonic circuits and controlled defect fabrication are retarding their development for real applications.

Two conceptually different approaches have been employed to generate the 3D PhC structures. One approach relies on controlled patterning and microfabrication methods such as focused ion beam milling,[14] direct laser writing by multiphoton-polymerization,[15] robotic ink writing,[16] conventional[17] or holographic[18] lithography or micromanipulation[19]. Most of these methods readily offer means for defect inscription inside the structure, but are limited either by the speed of processing or by the resolution, though in some cases this is expected to change in the future. The first demonstration of the guiding of light in three dimensions in a 3D PhC waveguide was recently demonstrated with silicon rod based PhC fabricated by aligned wafer bonding,[20] which has also rather limited prospects from the point of view of integration and large scale manufacturing.

The other approach is based on self-assembly of monodisperse colloidal spheres, featuring, e.g., gravitational sedimentation,[21] vertical deposition,[22] colloidal epitaxy,[23] electrophoresis,[24] moulding into capillaries[25] and the flow cell method[26]. These self-assembly techniques can be applied to form photonic crystal structures with photonic band gaps ranging from deep UV to far IR frequencies, while being both fast and cost efficient. However, they cannot be directly employed to fabricate deterministic defects, for which they have to be complemented by lithographic means[27,28]. They are also incompatible with microelectronics processing due to uncontrolled particle contamination.

2.3.1 SELF-ASSEMBLY OF COLLOIDAL OPALS

Self-assembly of colloidal opals is typically based on vertical deposition, which is a chip- or wafer scale method where a hydrophilic substrate is immersed into the colloidal suspension and slowly withdrawn to form a thin meniscus at the liquid-vapor interface as shown in FIGURE 2.6A. The microspheres agglomerate on the meniscus with solvent evaporation and self-organize into a face centered cubic (fcc) lattice due to the strong attractive forces in the liquid necks between the drying spheres. In this thesis, the method was developed further in Publications IV–V. First it was noticed during a vertical deposition experiment, that as chips with narrow trenches were slowly immersed into the suspension, the suspension began to move upwards in the channels. It was clear from the first experiments that the crystallization process was similar to the vertical sedimentation.

In capillary directed self-assembly (CDSA), instead of dipping the substrate into the suspension, a sub-µl droplet of the suspension is dispensed into a reservoir well (R) on the substrate as presented schematically in FIGURE 2.6D. The colloidal microspheres are directed into the desired positions via capillary channels (C) and self-assembled into opal basins (B) due to solvent evaporation and capillary force. The major advantages introduced by CDSA over the former self-assembly methods is the full spatial selectivity of the opal growth, resulting in negligible particle contamination of the substrate. The technological advantage of the method lies in the exploitation of the existing standard microelectronics or MEMS fabrication processes combined with directed self-assembly. Automated delivery of the suspension combined with fully controlled deposition environment could facilitate the up-scaling of CDSA to large scale production.

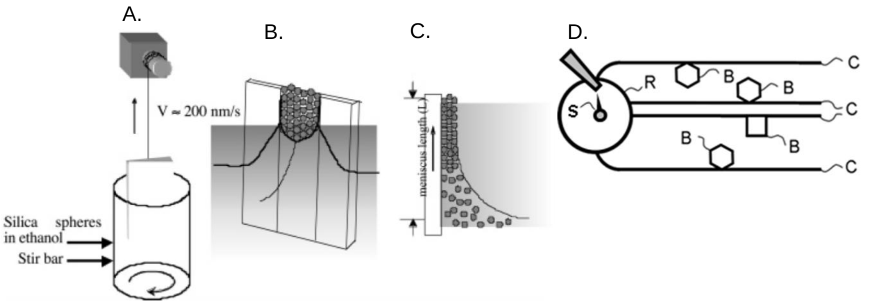

FIGURE 2.6 Schematics of the capillary opal deposition methods utilized in this thesis. A) Vertical sedimentation [VII] is based on controlled withdrawal of the substrate from the colloidal suspension. B–C) The microspheres agglomerate on the meniscus with solvent evaporation. D) In CDSA the suspension (S) is dispensed into a reservoir (R) from which the suspension is directed via capillaries (C) into the opal basins (B). [V] In both methods, the microspheres self-organize due to capillary forces between the drying spheres.

The factors influencing the deposition in CDSA are capillary channel geometry, sidewall smoothness, surface hydrophilicity and solvent evaporation rate. The solvent evaporation rate can be controlled by the ambient temperature and by the relative humidity: the best opals have been obtained when the level of humidity has been close to 97 %, i.e. when the evaporation rate is relatively slow. In the early phase experiments, the suspension dried before moving any considerable distances, but when some moist air was applied simultaneously with dispensing, the process somehow succeeded. Therefore a small temperature and humidity controlled chamber was constructed for the experiments. The nominal RH of 97 % was obtained with oversaturated dipotassium sulfate (K_2SO_4) dissolved in de-ionized water.[29] The high relative humidity practically closes the open facet of the capillary channel.

After succeeding to fill plain trenches with artificial opals (FIGURE 2.7A) from aqueous suspension of large silica beads with 890 nm diameter,[30] substrates with opal basins connected to optical waveguides were designed and fabricated on bonded SOI wafers with a 10 µm thick (100) SOI film on 1 µm thick BOX. The wafers were patterned using optical lithography and the pattern was transferred into silicon in an inductively coupled plasma (ICP) etcher with fluorine chemistry. The process utilized was originally developed for the fabrication of the rib waveguides with tapers converting them into strip waveguides.[31] Instead of the standard pulsed Bosch ICP process, with sequential etch and passivation cycles, a continuous process with simultaneous etch and passivation was employed. With a gradually decreasing platen bias power and ramping of the etch and passivation gas flow rates, trenches with optically smooth and vertical sidewalls were defined up to a depth of 5–6 µm in each run. Two layer etch process was realized as a single etch run with several successive treatments and two different mask layers. After the first etch step an in-situ oxygen plasma was employed to remove the first sacrificial resist mask and all excess sidewall passivation polymers before initiating the last etch in which the pattern definition was based on a SiO_2 hard mask. After the ICP process, the remaining fluorine polymer residues were removed by harsh oxygen plasma and wet chemical treatments, after which the substrates were thermally oxidized to reduce surface roughness. The 250 nm thick thermal SiO_2 film grown at this step was removed in diluted HF to improve the edge profiles and then another 250 nm SiO_2 film was grown as the final coating of the waveguides. Prior to the capillary deposition, the substrates were hydrophilized in RCA1 bath (NH_4OH:H_2O:H_2O_2 1:5:1 at 65 ºC) for 5–10 minutes.

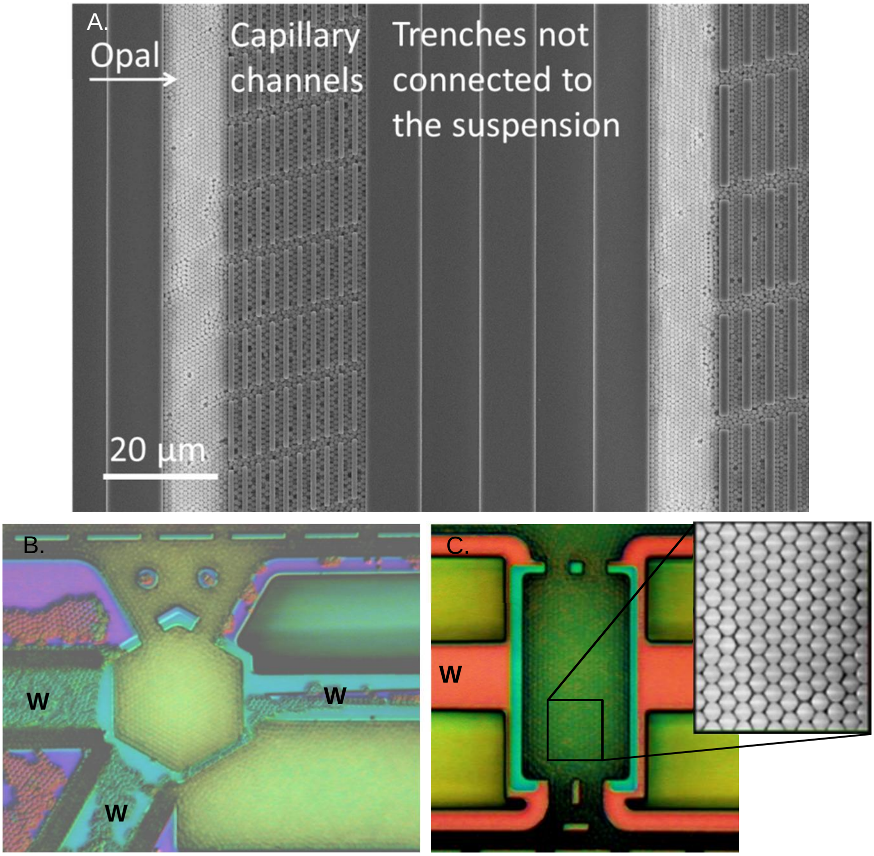

FIGURE 2.7 Top views of the opals. A) CDSA opal in capillary trenches. B, C) Waveguide – opal structure (waveguides marked as W). Silica opals (Ø = 890 nm) were deposited by B) vertical deposition on 30 µm wide hexagonal well at JOGU and C) CDSA on 16 µm wide well at VTT.

2.3.2 OPAL ANALYSIS

Optical reflectivity is an important measure of the crystalline quality of the opal. Instead of visualising only the top surface, reflectance spectra provide information on the layer spacing and optical, or packing, density of the opal. The surface reflection of opals originates from the (111) lattice planes and from that it is not possible to distinguish between fcc (ABCABC stacking) and hexagonal close packed (hcp) (ABAB stacking) structures and their random combinations due to the equal spacing of the (111) planes in these structures. However, the formation of pure fcc lattice is energetically favoured in evaporation-based ordering of colloidal spheres, when the growth direction is perpendicular to the surface, i.e., perpendicular to the (111) plane.[32]

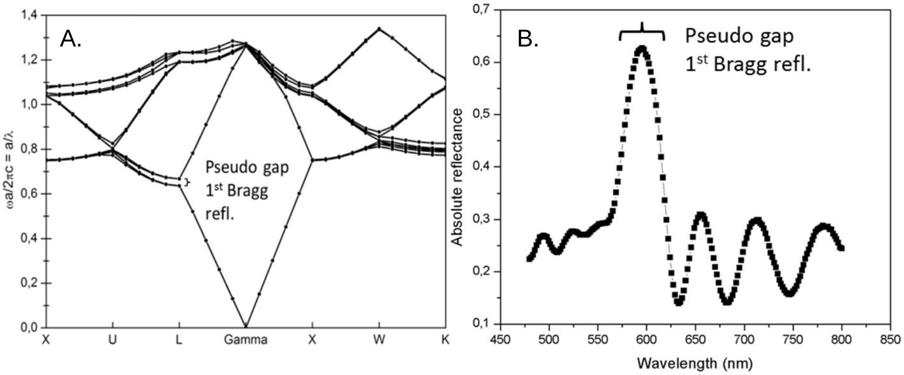

FIGURE 2.8 A) Photonic band structure of an fcc opal made of silica beads with refractive index n = 1.42 after annealing. The [111] reflection at 0.65 a/λ is the 1st Bragg reflection. B) Reflection spectrum from artificial opal with silica bead diameter of 330 nm. The intense peak at 575 nm is the 1st Bragg reflection and the smaller oscillations result from the Fabry-Pérot reflections through the opal.

The band structure of an fcc opal is presented in A. Opals are not photonic crystals with full band gap, but they already have a pseudo gap that can be characterised by optical spectroscopy. The first order Bragg reflection is due to the pseudo gap at around 0.6 a/λ in ΓL [111] direction when measured incident to the surface. The Bragg reflection characteristics reveal the crystalline quality of the opal and the thickness of the opal can be determined from the period of the Fabry-Pérot resonance resulting from multiple reflections at the interfaces of the opal. When the lateral size of the opal is small, the reflection measurement becomes more complicated due to the large numerical aperture (NA) of the microscope. Instead of light incident to the surface, the measurement averages over several incident angles defined by the NA of the lens, which significantly broadens the reflected characteristics.

In order to allow accurate analysis of the opal quality from optical spectroscopy, we developed a program that is able to extract the characteristics from the measured spectra as the magnification, NA and focal length of the lens were given as input parameters as discussed in detail in Publication VIII and in FIGURE 2.9.

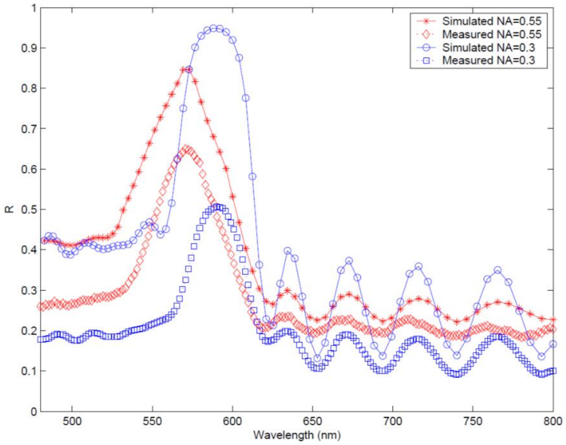

FIGURE 2.9 Measured and simulated reflection spectra from typical PMMA opal on silicon. The NA of 0.55 corresponds to 50x magnifying optics with spot size of 3 µm and NA of 0.3 to 10 x magnifications with 15 µm spot size. [VIII]

Opals reflect light in many angles and wavelengths, based on the different separation of the lattice planes in different directions, just like atomic crystals reflect X-rays. When deposited over large areas, the reflections from artificial opals can also be measured with goniometer setup to gain quantitative information about the lattice properties. When inspected with bare eye (FIGURE 2.10), they appear visually similar to natural opals which are gem stones, and the lattice planes reflect colours beautifully when turned into right angles in sunlight. For beads of the order of 1 µm, the first order reflections are beyond the visible range. The surface arrangement of opals can also be detected by SEM (FIGURE 2.11), and some indication of the quality can even be obtained visually by optical microscopy when the bead size is approaching 1 µm.

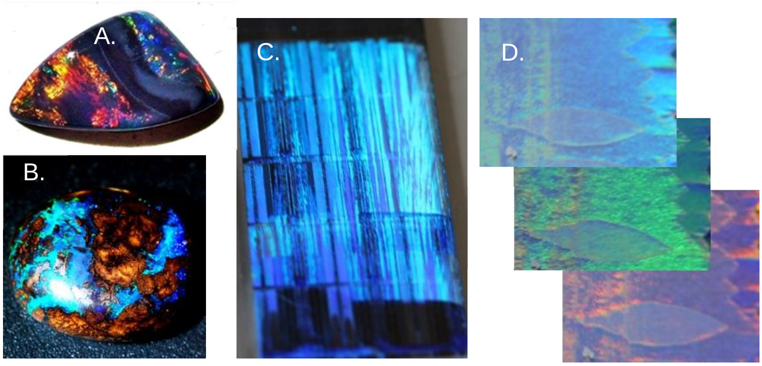

FIGURE 2.10 A–B) Natural opals from Australia (http://www.godsstones.com/Opal.html and http://www.opals-on-black.com/) and artificial opals for science, C) made from small PMMA beads and D) larger silica beads on silicon wafer in JOGU. In D), images taken from different angles show reflections from different planes of the lattice.

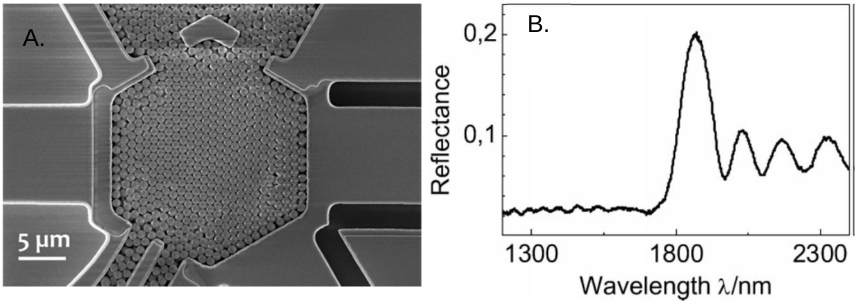

Figure 2.11 a) SEM image of a CDSA opal made from 890 nm silica beads and b) the corresponding reflection spectrum at IR region.

2.3.3 Inverted 3D PhC

The full photonic band gap requires a high refractive index contrast in the photonic crystal in order to obtain high enough degree of internal reflections. It is equally important that the materials have negligible absorption and that the interfaces are smooth enough for not to induce scattering, because all these effects are strongly magnified in the reflections. As this is the prerequisite for obtaining the photonic band gap, the ability to enhance non-linear effects and light-matter interaction is also the major motivation for the research of the 3D photonic crystals.

The refractive index of the silica beads is too small to allow the generation of a full band gap. Conformal deposition techniques such as ALD, LPCVD and some liquid phase deposition methods can be employed to fill the voids between the spheres with high index material. When the spheres are removed, the structure is called inverted photonic crystal. An example of inversion with ALD TiO2 is presented in Figure 2.12, together with the band structure. The refractive index of TiO2 is too small to generate full band gap.

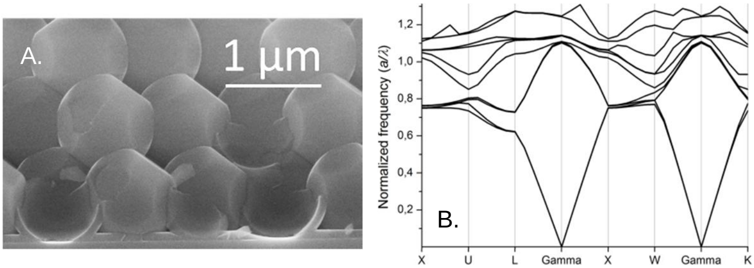

Figure 2.12 a) ALD TiO_2 is smooth and fully conformal in inversion process. b) Band structure of opal inverted with ALD TiO_2 with $n = 2.24$. Only pseudo gaps in 111 direction (ΓL) exist; in addition to the 1st Bragg reflection, a second pseudo gap is present at around 1.15 a/λ.

In addition to the conformal deposition of a high refractive index material, the inversion process requires the removal of the silica spheres, which can only be done with HF based acids. When considering integration with waveguides, the necessity to remove the silica spheres becomes problematic as the etchants can also damage the waveguide claddings and the underlying photonic chip. The integration process was developed in Publication IV. As a first step, the 200–250 nm SiO_2 optical cladding covering the waveguide cores were protected by a 20 nm thick alumina (Al_2O_3) film. Al_2O_3 can be grown conformally with ALD and it has extremely high selectivity to silicon, 1:80 000, in SF_6 based plasma etch which allows for the efficient removal of excess silicon deposited during the inversion. Most importantly, after annealing at 900 °C for 30 minutes the Al_2O_3 film becomes chemically resistant to certain HF based chemistries that can be used in silica sphere removal, where the underlying photonic components could easily be destroyed. The only major drawback is the high annealing temperature, which can easily exceed the thermal budget of the photonic chip.

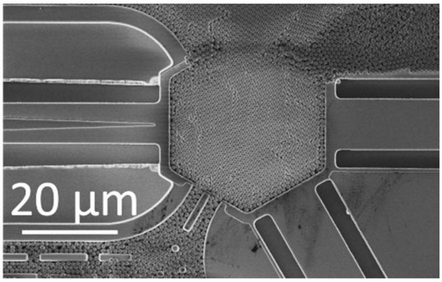

FIGURE 2.13 Scanning electron micrograph showing the top view of the integrated opal before inversion. The small over-flow of silica spheres illustrates the importance of careful control of the surface properties and is due to too high level of hydrophilicity of the Al_2O_3 surface during the opal self-assembly.

Opal deposition was based on CDSA [V] of monodisperse colloidal silica spheres. The spheres with a diameter of 890 nm were synthetized by Unger's method[30] and used as 2–5 vol. % aqueous dispersion. A droplet of suspension, 0.2–0.8 µl in volume, was dispensed into a reservoir well defined on the substrate, and readily directed via capillary channels into the attached opal basins. The agglomeration of the spheres into the basins and their simultaneous self-assembly into face centered cubic (fcc) lattice were driven by solvent evaporation. Prior to the opal deposition the substrates were chemically hydrophilized, and an about 40 hour settling time was required to reduce the Al_2O_3 hydrophilicity (surface OH groups) to optimal level for CDSA. Opal deposition on highly hydrophilic Al_2O_3 substrate immediately after the chemical treatment led to uncontrolled spreading of the suspension over the surface, whereas in slightly too hydrophilic substrates the suspension occasionally escaped from the capillary channels and opal basins as presented in FIGURE 2.13. The opal depositions were performed in a process chamber with 93 % relative humidity of the solvent (water) and 30 °C temperature.

After drying the opal, thin silicon film of 100–130 nm was conformally deposited on the structure with LPCVD by decomposing silane (SiH_4) at 540–560 °C, which tends to slightly decrease the silica sphere diameter. Silicon deposition was made both at Ioffe Institute (Russia) in a custom made LPCVD furnace and at DanChip (Denmark) with state-of-the art commercial LPCVD furnace similar to the ones in Micronova. Unfortunately, neither of these institutes was able to deposit perfect conformal silicon film.

The silicon deposition at DanChip was performed at 560 ºC. The resulting film thickness was uniform over the 3–6 topmost sphere layers, but below that the deposited silicon was rough (FIGURE 2.14c), which is detrimental for the optical properties of the PhC. This kind of roughness typically results from silane depletion during the deposition and could be avoided by slightly decreasing the growth temperature to 550–540 ºC. This would slow down the silane decomposition at the surface and thus reduce the depletion inside the opal. Unfortunately DanChip refused from any modifications of their deposition process.

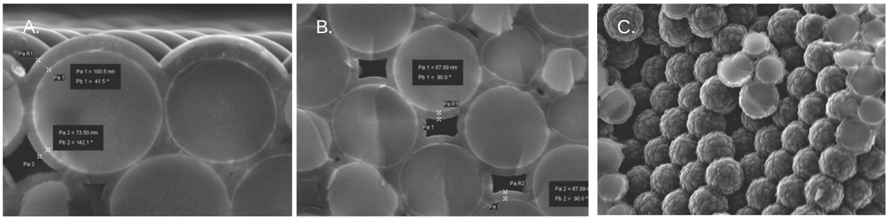

FIGURE 2.14 SEM micrographs of opals after silicon deposition at DanChip. Cross section views from A) the opal top layer B) a few layers below the top and C) a crack deeper within the opal, showing the roughness of the silicon layer. Silica sphere size is 890 nm.

In the case of the LPCVD silicon deposited in Ioffe, the surface roughness of the amorphous silicon film inside the silica opal template was rather small, with film thickness varying from 100 nm to 130 nm but being constant throughout the thickness of each opal. However, the sample top surface was covered with a several micron thick blanket of black silicon that had to be removed before inversion (FIGURE 2.15A,B). Both the top surface opening and HF etch were first subcontracted to Ioffe, but their silicon etch process left deep holes into the opal template and also the SiO_2 claddings of the sample were damaged during the HF etch based removal of the silica spheres. These successive damages made the samples unusable for coupling measurements.

To overcome these problems, we strongly modified the SF_6 based dry etch process to allow fully selective silicon removal from top of the spheres, and also developed the material combinations and etch chemistry to protect the waveguide claddings during the removal of the silica spheres. After testing different combinations, the dilute mixture of CH_3COOH and NH_4F, known as phosphosilicate glass (PSG) etch, was found to be able to etch SiO_2 fully selectively to annealed Al_2O_3. The annealing temperature has to be high, close to 900 °C, which is similar to the thermal oxidation temperature of the waveguide claddings but may be too high for the protection of other possible elements integrated on the photonic chip.

In practice, unfortunately, the selectivity of the dry etch process was found not to be stable over ICP chamber conditioning (many etch processes change with time as the materials covering the chamber walls change) and when the actual samples were etched, the selectivity was not high enough for perfect removal of the thick black silicon film as can be seen from the damage at the top of the opal in FIGURE 2.15E,F. However, this only damaged the topmost layers of the opal and the Al_2O_3 cladding protections were left intact. The inversion was completed by the removal of the silica opal template.

Amorphous silicon grown by LPCVD has a high concentration of dangling bonds that induce a considerable absorption at near-IR. Therefore, silicon was crystallized after inversion by annealing first at 600 ºC for 3 hours and some of them further at 900 ºC for 1 hour. As already discussed in Section 2.1.3, this kind of two phase annealing transforms the amorphous LPCVD silicon into a polycrystalline phase that is rather transparent at wavelengths above the fundamental absorption gap of silicon at 1.15 µm.

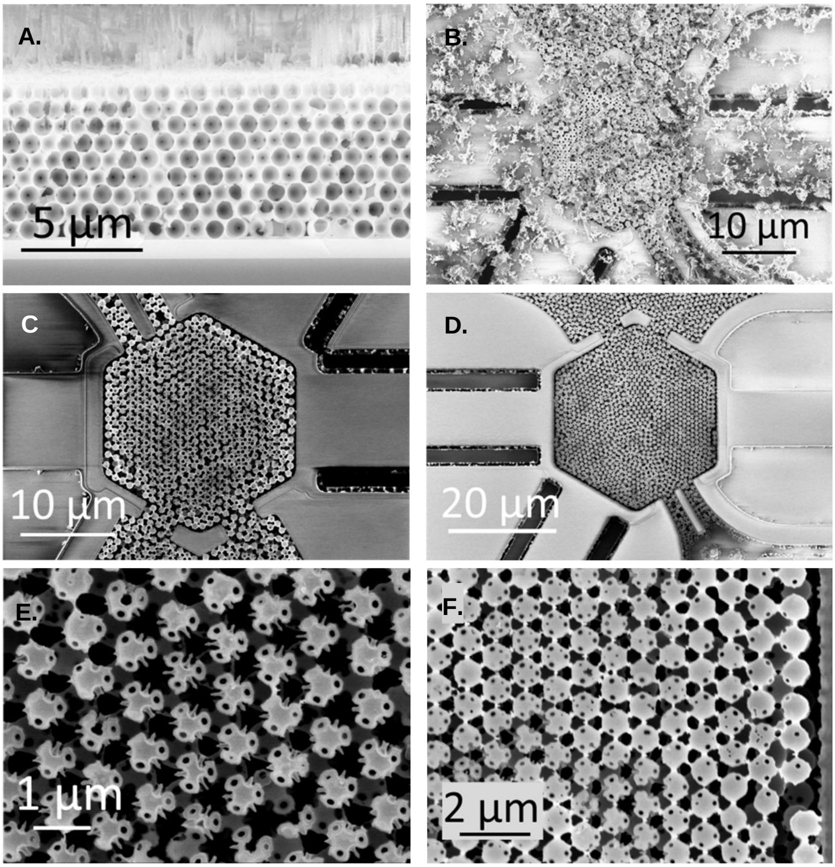

FIGURE 2.15 SEM micrographs of opals after silicon deposition and inversion at Ioffe. A) Cross section and b) top views of inverted opals showing residues of the black silicon at top surface. The silica sphere size was 890 nm. B–D) Inverted PhCs in hexagonal wells. E) is a close views of C) and F) of D). Silica opals (Ø = 890 nm) were deposited by CDSA on Al_2O_3 protected substrates at VTT. Spheres below the first layers are undamaged.

2.3.4 OPTICAL ANALYSIS OF INTEGRATED OPALS AND 3D PHCS

When the opals are integrated with waveguides, their properties and the characteristics of the integration can be probed via the waveguides. The planes perpendicular to the mode propagating in the waveguide are between $(1\bar{1}2)$ and (110), represented by M and K points in the reciprocal space, respectively. An example of the transmission spectrum, measured from a poly-crystalline opal with 810 nm beads and about 10 µm crystallites, is presented in FIGURE 2.16. The 1st Bragg reflection in the [111] direction (ΓL) is theoretically located at 1680 nm, possibly associated with the measured transmission dip at around 1670 nm, even though this ΓL direction is not the direction of the mode propagation. A deep transmission dip is detected also at 1450 nm, rather close to the theoretically narrow ΓΞ reflection; though it may also correspond only to a pronounced Fabry-Pérot oscillation minimum.

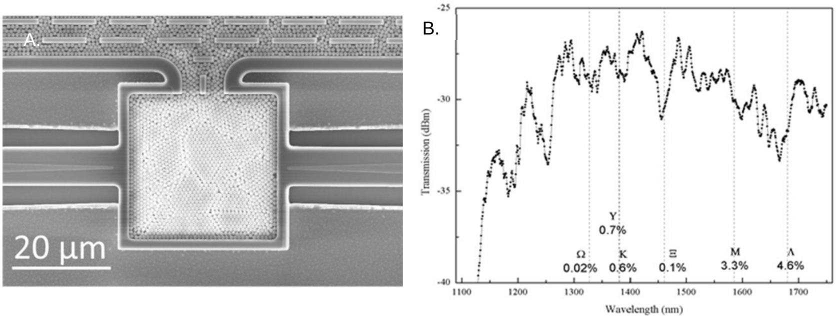

FIGURE 2.16 A) Polycrystalline silica opal (Ø = 810 nm, opal thickness 10 µm) inserted between two tapered ridge waveguides. B) Corresponding transmission spectrum in dBm. The vertical lines indicate theoretical positions of the 1st order Bragg reflections.

The behaviour of the light at the waveguide – PhC interface was studied by 3D finite-differential time-domain (FDTD) analysis by Kevin Vynck in USTL. In the case of a bulk 3D PhC without defects to allow waveguiding, coupling between the elements is reduced to reflection, transmission, scattering and self-guiding.

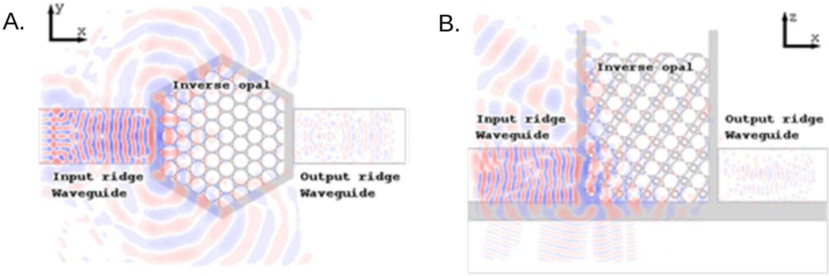

FIGURE 2.17 A) Top view and B) side view of a continuous TE-polarized wave sent from a 3 µm strip waveguide to a 5 µm wide hexagonal well filled with silicon inverse opal.

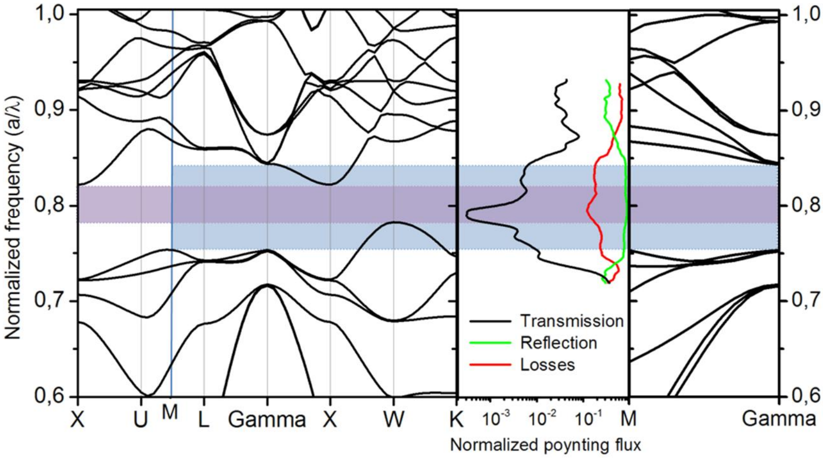

FIGURE 2.18 Simulated transmitted and reflected spectra for fully infiltrated inverted opal and the corresponding photonic band structure. The transmission through the PhC is reduced by the reflection from the pseudo gap in $\Gamma\mathrm{M}$ direction (pale blue), with further reduction resulting from the full photonic band gap (violet).

The FDTD simulations were performed for a 4–5 µm long PhC interposed by waveguides with height and width of 3 µm. The 3D PhC was defined as void spheres with a diameter *d* in a silicon matrix, arranged in an fcc lattice with (111) plane at the surface and $\Gamma\mathrm{M}$-direction parallel to the mode propagation from the waveguide as shown in FIGURE 2.17. The lattice constant $a = d\sqrt{2}$ was defined by *d* of 890 nm. The necks between the hard spheres were not included into the model, and at the side interfaces the spheres were cut, otherwise maintaining the fcc arrangement. Silicon was treated as dielectric with frequency independent refractive index (n = 3.45), which is adequate at near infrared region at wavelengths above the optical absorption gap tail at 1.15 µm.

As shown in FIGURE 2.18, the simulated transmission and reflection spectra are directly related to the photonic band structure of the inverted opal. In the simulated spectra the full PBG of the inverse opal is observed as a clear dip in the transmission, accompanied with smaller intensity reduction due to the pseudo gap in $\Gamma\mathrm{M}$ direction. The simulated field intensity distribution illustrates the behavior of a continuous wave reaching the interface between the waveguide and PhC at a wavelength in the photonic band. The light is clearly stopped by the inverse opal, but the decrease in transmission is not complete as the light reflected by the inverse opal is partially coupled into the silicon walls and substrate, where it propagates and reaches the output ridge waveguide.

The calculated photonic band structure for the experimental inverted opal structure in FIGURE 2.19 is aligned with measured transmission characteristics of the inverted PhC. The dimensions used in the band structure calculation were extracted from SEM images, with lattice constant d = 860, silicon shell thickness of 100 nm and the diameter of the void between the sphered equal to 60 nm. The measured spectral data is based on reflection spectra measured with an IR microscope from the top (111) surface of the inverted fcc opals in ΓL direction. Due to the roughness of the inverted PhC surface and the spot size exceeding the PhC dimension, only small part of the total intensity of the spectra was reflected from the top surface of the inverted opal and thus the PhC reflection could not be directly extracted from the measured data. However, the Fabry-Pérot oscillations originating from multiple reflections between the top and the bottom interfaces of the 10 µm thick PhC were clearly distinguishable. The amplitude of these oscillations is proportional to the interface reflectivity and PhC transmittance and allows extraction of the transmission characteristics in ΓL direction perpendicular to the substrate. The contributions from the PhC top surface reflection and from the simultaneous low frequency Fabry-Pérot oscillations through the BOX film between the PhC and the silicon handle wafer were excluded by normalising each amplitude with average reflection. As shown in FIGURE 2.19, at the photon energies in range of full photonic band gap (a/λ = 0.8–0.87 or $\lambda = 1.3–1.53$ µm) there is a drastic decrease in the amplitude, extending over the adjacent pseudo gaps between the 11th and 12th bands and 5th and 6th bands, thus covering the range from 1.3 to 1.65 µm. The amplitude is strongly reduced also near the position of the first order pseudo gap (a/λ = 0.43–0.54, $\lambda = 2.2–2.9$ µm) in ΓL direction.

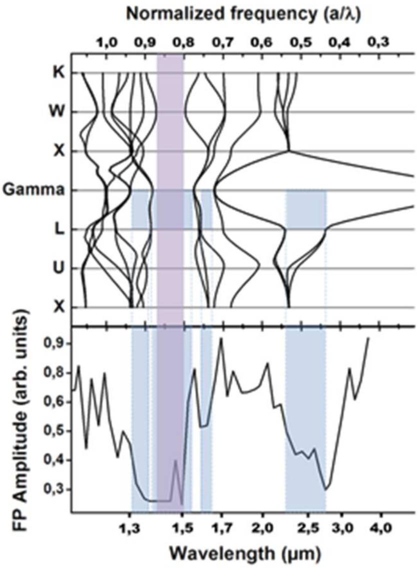

FIGURE 2.19 Optical analysis of the inverted 3D PhC interposing ridge waveguides. A) Simulated band structure of inverted fcc crystal constructed from thin silicon shells as in the experiment. B) Fabry – Pérot amplitude of the reflected IR light as measured from top of the PhC in [111] direction (ΓL).

As detailed in Publication IV, the transmission through the waveguide – PhC – waveguide structure was measured by end coupling the incident light from a single mode optical fiber into the waveguide. White light supercontinuum laser was used as the light source, as it offers a wide spectral range with high intensity that is optimal for probing the band structure of embedded PhCs with photonics instrumentation operating at NIR frequencies. The supercontinuum is generated by coupling the 1064 nm output radiation from a miniature Q-switched Nd-YAG laser into a highly non-linear photonic crystal fiber. The result is a broadband spectrum extending from 600 to 1800 nm with an approximately -15 dBm/nm output power. The supercontinuum light was coupled into a single mode photonic fiber, which was aligned with the ridge waveguide. Light coupling into the waveguide was monitored by detecting the mode profile at the waveguide output with CCD IR camera and scattering from the vicinity of the PhC. The transmission spectra was found to depend strongly on the input fiber alignment since the waveguides were not truly single mode, but able to support a multitude of modes with only one properly confined into the ridge waveguide core. However, when properly aligned, the shape of the output signal was elliptical, with FWHM width of 7 µm and height 5 µm, respectively. The measurement configuration was complemented with a multimode optical fiber coupled to the waveguide end, and the transmitted intensity was recorded with optical spectrum analysers (OSAs) as presented in Figure 2.20. Because the difference between the transmitted intensity and the reference was larger than the dynamic range of the OSAs, two different analysers with different intensity distortion were used to confirm the main features of the spectra.

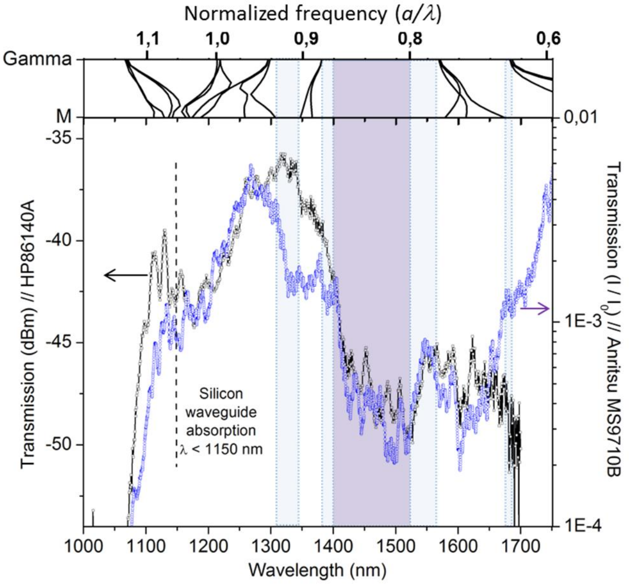

Figure 2.20 a) Calculated band structure presenting the ΓM direction and b) transmission spectra in ΓM direction measured through the waveguides coupled with the photonic crystal. Measurement was repeated with two different spectral analyzers (blue and black spectra) to determine which spectral features are due to the non-linear dynamic response of the analyser and which are due to the sample. Pale blue colours indicate the pseudo gaps in ΓM direction and violet corresponds to the full photonic band gap defined at W point as presented in Figure 2.19.

Both transmission spectra show the silicon absorption below 1.15 µm and a 5 dBm reduction in the transmitted intensity from 1.4 to 1.53 µm, corresponding the spectral position of the full photonic band gap at reduced frequencies of $a/\lambda = 0.8–0.87$, similar to the simulated fully infiltrated PhC. In the partially filled PhC the full band gap is much wider than in the simulated structure and thus the effect of the pseudo gap in the direction of mode propagation (ΓM) is nearly identical to the band gap. The wider reduction in the transmitted intensity, assumed to correspond the ΓM pseudo gap in the simulated structure, can however be seen also in the measured spectrum, with spectral range of 1.3 µm to 1.65 µm exactly corresponding to the three pseudo gaps in the ΓL direction. On the other hand, the narrow pseudo gaps in ΓM direction do not align with the measured spectra.

Even though the wider region in the FDTD simulation also corresponds to the pseudo gap in ΓL direction, the origin of these spectral features is probably different. In the simulation the lattice is perfect, and the reduction is mainly due to reflection which is close to unity across the whole range of interest. In the experimental structure, scattering from defects and surface roughness of the spheres will have an influence. The L point is a high symmetry point in the reciprocal lattice, related to the (111) plane with tight arrangement of spheres, thus a strongly reflecting plane. In addition to the (111) planes parallel to the direction of the mode propagation (opal surface), the fcc lattice contains several similar planes nearly perpendicular to the mode propagation. Light scattered into these directions (ΓL) is reflected and eventually guided into allowed directions such as ΓU or ΓW, adding to losses rather than reflection. Another effect of the disorder is to smear out the narrow pseudo gaps.

As a conclusion, the simulation clearly identifies issues that have to be considered in the device integration, such as elimination of the weak optical paths allowing light coupling from input to output waveguide around the PhC element. Simultaneous measurement of the band gap from ΓL and ΓM directions verifies both the fcc order of the lattice and the existence of the band gap in the integrated 3D PhC, but also the existence of scattering due to defects and surface roughness. From the PhC fabrication point of view, this indicates successful demonstration of the integration of the 3D PhCs with the conventional waveguides, even though not yet on a level adequate for integrated optics.

2.4 PROSPECTS OF INTEGRATED PHOTONIC CRYSTALS

The research conducted for this Thesis (Publication IV) has, to our knowledge, been the only demonstration of a full photonic band gap in 3D photonic crystals integrated with waveguides.

3D photonic crystals, or more precisely opals, are currently used as visual effects and colour changing indicators responding to a change in the refractive index of the media surrounding the opals or to a change in the opal beads themselves. The inversion of the crystal increases the light-matter interaction which has been shown to speed up the rates of photo-oxidation and photo-isomerization;[33] this does not necessarily require a defect line or a cavity, but the group velocity already at the band edge of the PhC can be significantly reduced[34]. The combination of fluidic channels and inverted crystals with optical access to monitor the state of the process could have interesting applications in bionanotechnology. In integrated optics the tolerances with respect to lattice order and alignment and to surface quality in the defect lines or defect cavities, combined with the large scale production requirements, are still beyond the reach of the currently available technologies.

2D photonic crystals are easier to integrate and control, but also their prospects seem rather limited. Most application studied are also related to sensors, as the properties of the 2D PhC waveguide transport and cavities also have an extremely strong response to the dielectric constant variations in the holes. Applications include also enhancing the light flow and coupling perpendicular to the crystal in solar cells and LEDs by preventing the in-plane transmission.

3 GRAPHENE

Graphene is a single atom thick layer of carbon atoms packed into a two-dimensional (2D) honeycomb lattice. In nature, it exists as an atomic plane of graphite and 2004 it was finally extracted as isolated 2D atomic lattice.[35] Due to its 2D nature, symmetric lattice and strong carbon-carbon bonds, graphene is different from any other material. The electrical, optical and mechanical properties of graphene have broken records with respect to charge carrier mobility and quantum effects at room temperature, high transparency as a conductive film, high tensile strength and impermeability to gases. In addition, as a two dimensional material all the atoms are on the surface, providing strong electrical and optical responses to all changes in the close vicinity. The amount of potential applications is vast, ranging from electronics and photonics to light weight composites.

3.1 GRAPHENE MATERIALS

Macroscopic graphene sheets were first demonstrated 2004 by A. Geim and K. Novoselov by mechanical exfoliation of lattice planes from graphite crystallites.[35] The simple method was based on repetitive thinning of the crystallite with scotch tape, until the adhesive surface was full with thin graphite flakes. When pressing this surface on a desired substrate and ripping off the adhesive tape, the probability of achieving some single layer graphene sheets on the substrate was slightly above zero. This method, called the Scotch tape method, is still used in the production of the highest quality graphene and other 2D crystalline monolayers in small separate flakes for fundamental research purposes.

The Scotch tape method is usually accompanied with aligned transfer for the production of multilayer 2D crystallite heterostructures. There graphene or other 2D sheets are first located from the original substrate, covered with thin sacrificial PMMA layer and thicker thermal release adhesive, peeled off and repositioned on desired position on another substrate. This method has been used to reveal fundamental physics, for example, to demonstrate the extreme limits of the charge carrier mobility in graphene on smooth *h*BN dielectric[36] and of the vertical transistor based on graphene – WS_2 – graphene heterostructure with high on-off ratio above 10^6.[37] Unfortunately, the method is too laborious to be applied in the production beyond individual devices.

The extraordinary interest of the research community to graphene has however nurtured a variety of methods that can be applied on large scale production of different graphene qualities. In practice, there are two fundamentally different approached to produce graphene, one relying on chemical vapour deposition (CVD) and epitaxy for the production of high quality graphene monolayers and the other on different routes of exfoliation and growth of graphitic micro- and nanoparticles for printable graphene films and graphene composites. The characteristics of graphene in various applications can be categorized as below:

- Semiconductor grade graphene for high speed electronics, photonics, THz-applications, sensors and MEMS. Requirements include high mobility, continuous grain boundaries and wafer scale production process.
- Transparent conductive graphene for transparent electrodes in organic optical devices such as touch screens and OLEDs. The main requirements are high conductivity and transparency with low-cost large area production.
- Flexible conductive graphene for printed electronics, requiring high conductivity and very low cost.
- Stretchable graphene for transparent and / or stretchable electronics and photonics.
- High surface area graphene for energy storage, catalysis and sensing. Requires application specific functionalization, high yield and low cost production.
- Graphene additives for light weight composites and foams.

The high quality graphene monolayers can potentially be applied in the first four categories, though the cost may become an issue in all other than the high end applications. Graphene flake based materials can be tailored for almost all applications, by modifying the geometry and functionalization, though the conductivity levels achieved this far have remained rather modest. In the following the most important production methods on both of these categories are summarized.

The most promising route to synthesize high quality large area graphene is CVD from hydrocarbon molecules on a catalytic copper[38], platinum[39] or germanium[40] surface at 900–1000 °C. Graphene is typically transferred from the catalytic surface to the final substrate, either plastic, ceramic or semiconductor, with the help of a resist layer (such as PMMA) which mechanically supports graphene during the separation from the growth substrate. In general, the CVD and transfer processes provide means for efficient wafer level graphene production for all applications requiring high quality graphene. When applied on metallic foils, the graphene area can be extended beyond any explicit limit, and has been demonstrated up to 30 inch[41] and now most probably already up to square meters. Graphene growth by ALD has also recently been demonstrated, but the quality is still rather doubtful.[42]

Another way to produce high quality graphene is based on the sublimation of silicon from silicon carbide (SiC) substrate at ultra-high vacuum (UHV) or low pressure conditions at ~1600 °C. The benefit of this method is that graphene is formed readily on an optimal substrate for high frequency and high power applications, but the SiC wafers are expensive, thus limiting the applicability of the growth method. Graphene grows on the carbon facet as a thick multilayer and on the silicon facet as a monolayer or defected bilayer, depending on the definition. There the topmost layer is clearly graphene, but the underlying layer is strongly attached to the SiC lattice, leading to a formation of a small electronic band gap of 0.26 eV.[43]

CVD on catalytic surface and sublimation on SiC are the only demonstrated methods with potential to provide large area graphene with quality close or similar to the exfoliated graphene. However, films and composite materials based on small graphene flakes and other graphene related powders currently dominate the commercial graphene market and may retain the position also in the future.

Graphene powders and dispersions can also be produced by various routes. The most common routes are based on exfoliation of graphite in different solutions but several methods to produce large quantities of graphene platelets and more complex structures from hydrocarbon gases with the aid of plasma have been developed. Graphene powders and dispersions can be tailored into inks for printing conductive or functional films, into pastes used as energy storage media with a high surface area, they can be used as additive for reinforcing composites and they can be a building block in light weigh foams.

The highest volumes of graphene flakes are produced by first treating graphite with strong acids, such as sulphuric acid, which intercalates between the graphite layers. Subsequent heating allows the acid to oxidize the graphene sheets which expands the graphite crystals into separate sheets of graphene oxide (GO). GO is a poorly conductive material that can be further reduced into graphene (rGO) by chemical treatment. However, only part of the oxidized defect sites are healed in the process, others leaving holes in the graphene platelets. GO and rGO have been employed in composite materials, energy storage, biomedical applications, catalysis and as surfactants.

Higher quality graphene dispersions can be produced by chemical mechanical exfoliation in intercalating solvent such as n-methyl-2-pyrrolidone (NMP) under ultrasound agitation. Unfortunately this process is slow and has a low yield, and it also requires centrifugation to separate the thin graphene flakes from thicker graphite flakes. Recently promising progress has been reported with e.g. electrochemical exfoliation[44], providing much higher yield and efficiency. This development is important in the quest for low-cost printable high conductivity electrodes for flexible applications.

The information available from the graphene powders generated from gaseous ingredients is not extensive, as the development is mostly done in companies such as Haydale (US) and Durhamn Graphene Science (DGS; UK) that do not reveal the production methods to the scientific community. These methods include catalytic CVD and arc discharge based graphene formation and they also seem to provide means to simultaneously functionalize the sheets with gaseous impurities present during the growth. Further, they are not restricted by the planar shape of the graphite source material, but can grow in different hollow geometries thus maximizing the surface area.

This thesis will present two different approaches for the production of high quality graphene for semiconductor industry. The first method is an attempt to develop the Scotch tape method for larger scalability, by using the patterned graphite as a stamp that is pressed on the substrate to release one graphene sheet. This would have allowed the automated exfoliation of graphene sheets directly on the active device areas on the substrate, but the development of the method was superseded by the introduction of graphene CVD and thus the results were not published. The other method presented is rapid photo-thermal CVD on copper and platinum wafers and foils.

3.2 ATTEMPTS FOR GRAPHENE FABRICATION BY STEP & STAMP MECHANICAL EXFOLIATION

Step & stamp exfoliation played an important role in the early days of graphene industrialization due to the large scaling potential in the absence of continuous thin film deposition method. Theoretically the adhesion forces between the graphene sheets in graphite are weaker than the adhesive force to e.g. a SiO_2 substrate, thus suggesting that after adhering the oriented graphite stamp to the substrate, the detachment would lead into exfoliation of only the first graphene layer.[45]

The initial results of the step & stamp exfoliation were promising. There a non-patterned graphite stamp was pressed on the substrate, lifted up, and shifted into adjacent position where the action was repeated. Scanning µRaman studies on these wafers indicated uniform coverage of small, slightly defected monolayer graphene flakes inside the stamping areas. The large graphite stamps were inhomogeneous and lattice planes were far from parallel to the substrate, thus the small size of the flakes was natural. Much better results were expected with stamps where the stamping area was clearly defined to consist of only one graphite crystallite parallel to the surface to be stamped. However, this research line was not found to be productive.

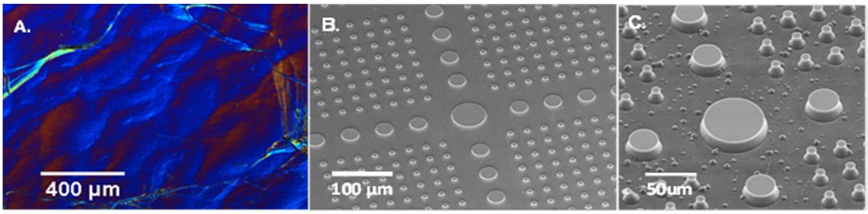

FIGURE 3.1 HOPG stamps. A) Phase contrast image showing the surface modulation of HOPG. SEM image of B) shallow and C) deep etched stamp pattern in HOPG.

3.2.1 STAMP FABRICATION

Stamps were patterned on highly oriented pyrolytic graphite (HOPG) and on natural graphite flakes, which were carefully parallelized on a carrier. The best commercially available HOPG had roughly 10 µm crystallite size with ± 0.4° mosaic spread, i.e., ± 0.4° off-axis orientation with respect to each other and average c-axis (vertical axis). This results in ~ 200 nm modulation on 40 µm area. The ~ 4 µm surface modulation on chip can be easily compensated by etching to avoid unwanted surface contact upon printing. The overall handling of HOPG is relatively easy, and the larger pieces were cut into few mm chips with dicing saw. The patterns were generated by electron beam- and optical lithography and the structure was transferred into the HOPG by inductively coupled plasma (ICP) etching with O_2 plasma and Ti, SiN_x or HSQ hard mask.

Natural graphite flakes can have much larger crystallite sizes than commercially available HOPG. Small natural flakes are also generally used as the raw material in Scotch tape exfoliation due to the better crystalline quality of graphite as compared to HOPG. However, on macroscopic level the flakes are highly inhomogeneous, which makes their processing into planar stamps rather cumbersome, though not impossible. The flake sizes vary from few mm to few cm, thicknesses from 40 to 700 µm. The small flakes can be used as such after attachment to the carrier chip and planarization, though the quality cannot be properly controlled. Large flakes can be rather easily cut with a surgical knife and cleaved into desired shape with uniform z-axis orientation. The material is much softer than HOPG, and sometimes contains impurity crystallites that are revealed upon etching.

3.2.2 STEP & STAMP PRINTING

The first stamp made on HOPG was a 60 µm square with alignment marks that were designed to coincide with the patterned substrate to allow aligned printing on wafer with predefined local bottom gate. The position of the stamping area on the HOPG surface was carefully selected to be as flat as possible, and the pattern was defined with electron beam lithography and etched deep enough into the HOPG with oxygen plasma. After initial cleaving to get a fresh graphite surface on the stamping area, the printing was performed with extreme care over planarization and force control. However, the results were confusing. Though it was clear from the marks on the printed substrate that almost all the patterned area had touched the substrate as planned, there was no graphene.

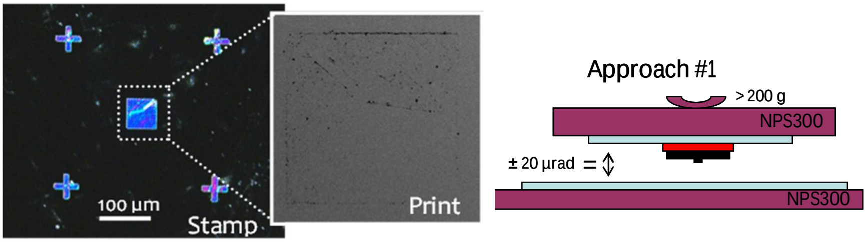

FIGURE 3.2 Optical image of the first patterned HOPG stamp, SEM image of the printing result on SiO_2 with no graphene detected and sketch of the printing configuration.

To optimize the process, new stamps with multitude of pillars were prepared and the printing process was tested with varying printing time, force, surface hydrophilicity and moisture levels using all possible combinations or parameters with reasonable steps. The effect of printing time was found to be insignificant. Increased force broke pillars more easily, but otherwise the effect on the printing was insignificant. Hydrophilicity of the substrate was the only significant factor but only in the way that if the substrate was not hydrophilic enough, nothing stuck into it. Hydrophilicity is basically a measure of the density of polarity, OH- groups and other dangling bonds at the surface, that induce polarization on graphene, leading to strong adhesion if the polarization density is high enough. The adhesion mechanisms are discussed in a bit more detail in section 3.4.2.

The quality of the edges of the structures etched into the graphite was suspected as the reason for the cleavage of thick pillars instead of thin sheets. If the sheets are attracted by each-others at the edges due to polymer contaminants, new carbon-carbon bonds etc., the hypothesis on the higher bonding strength of the graphene sheet attached to the substrate, if compared to that to the sheet next to it, would no longer hold. The patterning process was modified several times to exclude possible contaminants. On the samples with the Ti mask, the XPS surface analysis was performed showing fluorocarbon contaminants originating from the plasma etching of Ti or from the plasma etcher in general. After this the new stamps were made by patterning SiN mask with wet etching (BHF) and etching only graphite with plasma, or were cleaved and patterned solely with razor blade, with no improvement in the printing results.

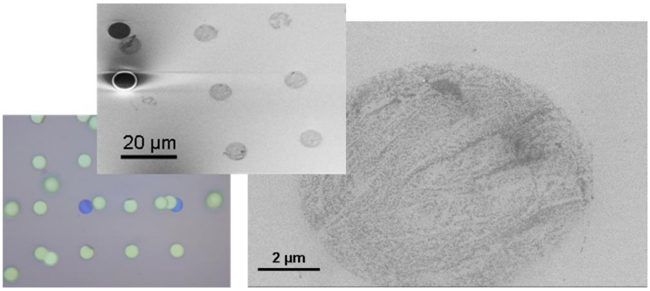

Figure 3.3 Printed graphene and graphite. The printed structure was either a thick graphite pillar or a thin non-continuous graphene sheet.

Natural reason for the printing of thick pillars instead of thin flakes is that if there is any angular force during printing, the pillars break on position defined by the geometry or the weakest point. However, when the alignment seems to be perfect, it is still not clear why only a non-continuous film is attached to the substrate either directly or after detachment of the longer pillar.

3.2.3 Summary & Prospects

Successful printing of thin graphene was reported by one other group during the course of the above experiments, thus with rather modest yield.[45] The use of electrostatic forces seems to be a requirement for somewhat successful printing, which we also have noticed in our transparent tape experiments: reducing the friction of the UV tape by UV exposure prior to tape removal from the substrate left the substrate empty despite the substrate properties. However, even with electrostatic effect the quality reported for the printed graphene is rather modest and the yield is low.[46] As a conclusion, this method fails to compete even with the Scotch tape exfoliation due to the complexity and low yield of the process.

3.3 GRAPHENE PRODUCTION BY CVD

The most promising route for the production of high quality large area graphene is chemical vapour deposition from hydrocarbon molecules to catalytic surfaces. This process allows for the fast and reproducible production of continuous, typically polycrystalline, graphene films on wafers and foils with catalytic surface. The role of the catalyst is to decompose the hydrocarbon and to provide a template for the growth in 2D, whereas the hydrocarbon decomposition and pyrolysis in the gas phase are typically prevented by the presence of hydrogen. The hydrocarbon sources are typically gaseous, like methane or acetylene, but also solid sources such as a thin PMMA film on the catalytic surface[47] or organic waste in the close proximity of the surface[48] have been successfully employed. The catalytic surface can be a transition metal like nickel[49], copper[38] or platinum[39], a metal alloy[50] or germanium[40] that was recently reported to support epitaxial graphene growth. When the carbon solubility into the catalyst is negligible, graphene growth is a self-limiting process that terminates as soon as the catalyst surface is covered with a single-layer of graphene. In the opposite case, carbon atoms diffused into the catalyst during the annealing will precipitate to the surface upon cooling as the solubility decreases with temperature, thus forming a multilayer graphene film.[51] The optimal growth temperature, typically around 950°C, depends on the catalytic substrate and on the hydrocarbon source – and on the process pressure and partial hydrocarbon pressure, which are also strongly linked with the quality of graphene.

The graphene CVD processes can be roughly divided into three categories; single layer graphene growth in a (i) rapid process (growth time typically 5–20 minutes) producing small (1–2 µm) grain size with well-connected grain boundaries, (ii) slow process (1–24 hours) producing large, up to 1 cm crystallites with poor grain boundary connections and (iii) various multilayer processes.[52] The pressure range allowing continuous growth reaches from at least 1 atm to 0.5 Torr.[53,54] Experiments on higher pressures have also recently been reported, allowing the growth on a molten copper[55], and the first attempts on graphene CVD were made in ultra-high vacuum (UHV) conditions on transition metals such as Ru,[56] providing isolated crystallites with tens on nm diameter. The method described in these thesis is an extreme form of (i), photo-thermal CVD where the deposition time is only few tens of seconds.

When considering graphene production for applications, the growth has to be followed by a suitable transfer and cleaning processes. These are all shortly addressed in the following chapters.

3.3.1 PHOTO-THERMAL CVD INSTRUMENTATION AND SET-UP

The graphene CVD furnace in Micronova was modified from a rapid thermal processing (RTP) furnace first by installing safety interlocks required for working with explosive gases and gas flow and mixing units to control the methane and hydrogen flows. In the first phase setup 2010, the nominal process pressure was limited to 20 Torr. This was because the flammable gases had to be diluted with nitrogen to 2 % concentration before entering into the pump. The second phase modification 2013 added possibility to control the deposition pressure from 0.5 to 50 Torr and to add argon into the process in addition to methane and hydrogen.

The RTP system is based on halogen lamps that heat the substrate directly, keeping the reflecting chamber walls relatively cool. This reduces the possible contamination from the walls and also minimizes the energy consumption by limiting the heated mass into the wafer. Another advantage of the RTP based system is the fast operation and the possibility for accurate control of the thermal gradient over the wafer or even larger area substrate with local *in-situ* pyrometer controlled power profile. The current RTP enables fast and industrially standard processing of wafers of up to 300 mm in diameter, with pre-set thermal gradient profile while the power is controlled by single pyrometer at the center point of the wafer.

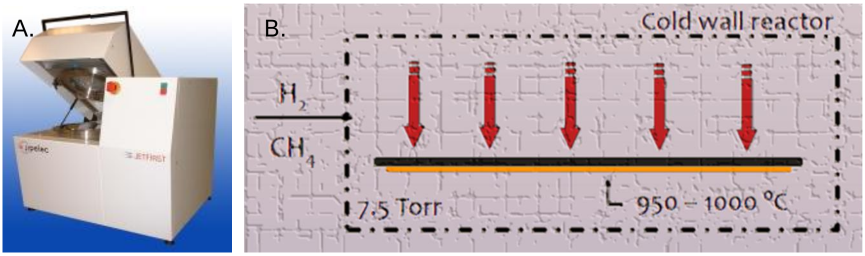

Figure 3.4 a) RTP system modified for graphene PT-CVD and b) the schematics of the process, with black plane presenting the photoabsorbing susceptor and orange the catalytic metal.

The drawback of the photo-thermal heating is the reflection of light from metals, which necessitates the use of absorbing susceptor such as SiC covered graphite or silicon wafer in the case of metallic foil catalysts. Thus the CVD process on silicon wafers with thin sputtered metal or on germanium is rather straightforward, but deposition on metallic foils requires rather tricky instrumentation. In principle, a standard graphite susceptor with bottom and cover could be used, but those are expensive and would suffer from metal evaporation. On the basis of our results [II], Samsung has developed the PT-CVD process further into roll-to-roll graphene CVD.[57] There the copper foil is moved between the lamps that heat susceptor plates on both sides of the foil, without touching it. Naturally the roll-to-roll approach has required also other innovations, for example hydrogen free chemistry for increased process safety. This claim is controversial as methane and methane and other hydrocarbons are equally flammable and generally with higher partial pressure.

3.3.2 PHOTO-THERMAL CVD ON COPPER

Copper has become the most popular catalytic substrate for graphene CVD due to the low carbon solubility (0.001–0.008 weight % at 1084°C) and it has also been the primary catalyst material in our PT-CVD development. Processes have been developed on both sputtered copper films on silicon wafers and on different copper foils. The optimal parameters for the growth of high quality graphene, such as the temperature of the copper surface, pressure and CH_4/H_2 ratio, do not depend on the substrate type, but the practical instrumentation to reach the optimal temperature is not straightforward. Without going into the details, the important facts in selecting the proper growth temperature are that the upper limit is defined by the copper evaporation and the quality of graphene improves with the temperature. Typical method for calibrating the deposition temperature is therefore an experimental procedure where the appropriate level of evaporation is visually determined. In a properly calibrated set-up, this temperature corresponds to 935°C at the standard 20 Torr growth pressure with CH_4/H_2 ratio of 4/1 (12 sccm CH_4 and 3 sccm H_2). [II]

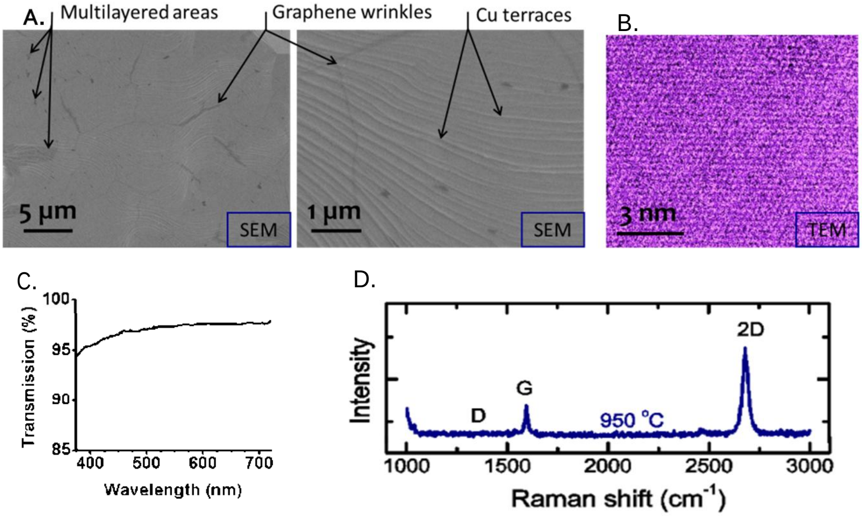

FIGURE 3.5 Graphene grown on copper foil by PT-CVD. A) Graphene on copper foil, showing the typical features of CVD graphene. B) Atomic arrangement of suspended graphene as seen by TEM. C) Large area optical transmission spectrum. > 97 % transmission indicates single layer thickness. D) Raman spectrum, indicating negligible defect density (D/G ratio).

In the PT-CVD process, a continuous graphene monolayer grows rapidly in few tens of seconds as a polycrystalline film. Typically in rapid CVD growth of graphene, the grain size in the µm range and the grain boundaries are of high quality and barely distinguishable in electrical transport measurements.[52] The grain boundary quality has not been confirmed for the PT-CVD graphene, but high mobility devices have been fabricated.[58] The interesting phenomenon is the deposition speed compared to normal RTP growth where the substrate or susceptor is resistively heated. In such tools the graphene growth rate can be an order of magnitude lower for otherwise similar growth parameters. The only difference is the existence of high photon flux from the lamps, which is (i) clearly interacting with methane as the methane incorporation into the chamber immediately induces a significant reduction in the power required to maintain stable substrate temperature and (ii) incident to the catalytic surface during the growth process. Both of these effects increase the temperature the methane molecules at the surface, thus most probably enhancing the catalytic process. If this energy is preserved on, or available to, the carbon atoms diffusing at the surface, it will also increase the quality of crystallization process. It is, however, not to be considered as normal increase in temperature, as that would only be seen as a shift in the optimal deposition temperature.

It is also sometimes claimed that the UV irradiation would destroy graphene and generate defects, but we have not noticed any indication of such problems in the outcome of the deposition process. It may be that as long as the irradiation is present with high flux, there is enough methane and energy in the chamber to fix the possible damage.

The most challenging phase in the graphene CVD on copper, however, is not the CVD process itself, but the preparation of the catalytic copper surface. Both the copper foils and the sputtered copper films on wafers possess significant challenges in terms of the production of homogeneous large area graphene films.

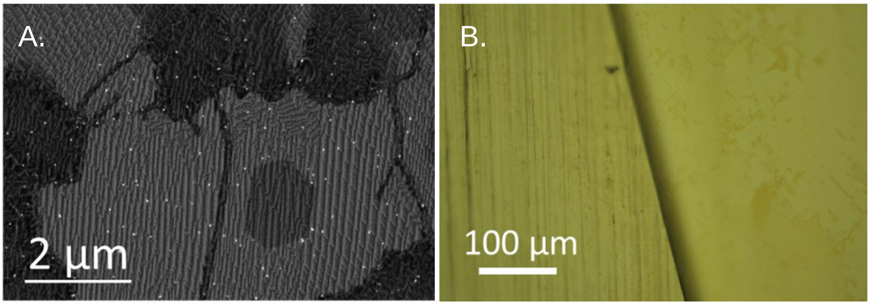

FIGURE 3.6 A) Graphene synthesized on sputtered copper (1 µm) with electroplated copper foils as a support layer. Before graphene deposition the surface was smooth. b) Copper foil (5N) with original and electropolished areas before graphene deposition.

Commercially available copper foils are not smooth and polished, but the surface topology is an image of the wheel used in pressing the foil – at low cost foils (typical 99.8 at. % purity) the grooves can be 20 µm deep and even in the most pure foils the surface corrugations are several microns in depth. All the foils also have impurity particles, not only at the surface but also buried deep into the material. The typical preparation of the foil is initiated with cleaning and etching to flatten the grooves. This is rather easy with low purity copper, but in pure copper the etch rates are highly non-isotropic and etching mostly roughens the surface.

In order to solve this problem and the problems related to the different thermal expansion properties between the substrate and thinner sputtered copper film, we employed electrolytic deposition of copper to generate a macroscopically thick (25 µm) copper foil with smooth sputtered surface for graphene deposition. It seems, however, that this process would require significant optimization procedure before the electrodeposited foil could be applied for graphene deposition. First of all, the sputtered film crystallizes in the graphene growth into a topology with sharp surface features and secondly, the carbon based impurities or other ligand residuals from the electrodeposition process seem to increase the number of graphene layers and introduce white (in SEM) graphitic particles into the film. Similar particles have been identified by Auger spectroscopy as Si-O-Cu agglomerates on a sputtered copper on silicon wafers with different barriers[59] and as Cu-O-Cl agglomerates on copper foils,[60] indirectly indicating that they can possibly originate also from other contaminants in the copper.

Instead of electrodeposition, electropolishing of commercial high purity copper foils was found to provide a satisfactory solution to this problem. Despite the fact that some impurity particles are buried deep into the foil and cannot be removed, the surface is significantly cleaned and smoothened by the removal of 5 µm copper from the top of the film. From the production point of view it is important that this process can also be applied on roll-to-roll production line. It is however to be expected that in the case of copper foils, the market push will motivate the copper foil producers to improve the quality of the foils dedicated for graphene production – provided the copper remains as the preferred catalytic template.

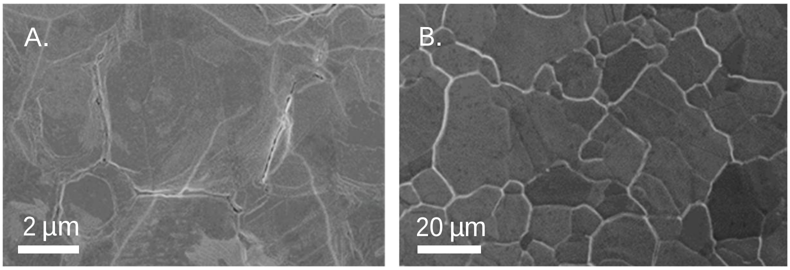

FIGURE 3.7 Graphene on sputtered copper on SiO_2/Si substrate deposited by A) state of the art commercial RTP and B) PT-CVD in Micronova. Continuous copper films, in B) in particular, have wide openings in grain boundaries where graphene tearing can be seen as an additional white glow in SEM images.

In the case of sputtered copper on wafers, the problems originate from the difference in the thermal expansion coefficient of copper and the underlying substrate, typically silicon and from the low evaporation temperature of copper. During graphene growth, the copper film is annealed close to the melting point and it forms a continuous polycrystalline layer on the SiO_2 surface. During the cooling phase, the copper grains shrink more than the underlying substrate, inducing voids between the grains. Unfortunately, this process is also able to tear graphene and majority of graphene samples deposited on copper wafers seem to contain such torn regions. It is expected, however, that if the cooling rate is decreased enough to allow for graphene detachment from the shrinking copper, graphene might remain mostly continuous on top of the void copper grain boundaries. This development work is currently on-going.

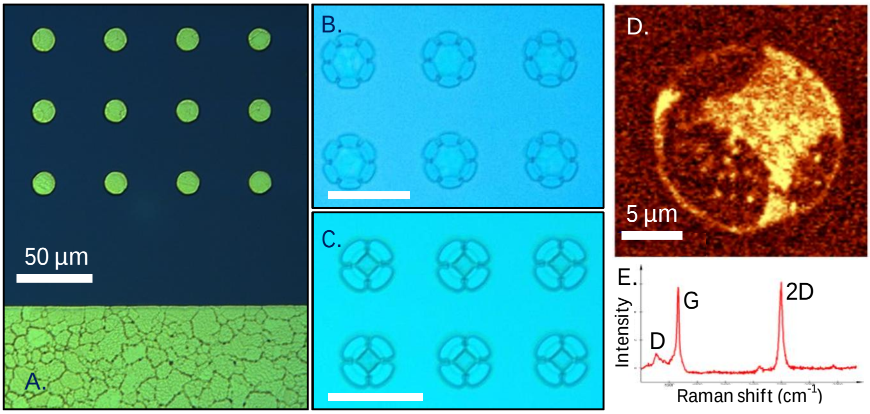

Figure 3.8 Graphene deposition on patterned copper. Optical image of a) Isolated (ϕ = 20 µm) and continuous copper after graphene growth, b) suspended PMMA-graphene islands (ϕ = 30 µm) after Cu etch and c) PMMA-graphene islands (ϕ = 20 µm) after attaching to the substrate. d) Raman map (2D peak) after PMMA removal, showing also some remainings of the bottom layer graphene that grows under the Cu film. e) The low quality of the underlying graphene is also seen in the average Raman spectrum measured from the lowered area, as the spectrum is a superposition from the spectra of the two different graphenes. The films in (c–e) were not transferred, but attached to the original substrate where graphene was grown. Scale bars in optical images 50 µm.

One early attempt to solve the problem was to pre-pattern the copper film into islands as shown in Figure 3.8. Isolated copper islands with diameter below 30 µm were found to remain continuous after graphene deposition and for diameters below 10 µm the islands appear single crystalline. Graphene was grown on top of the copper and an additional low quality graphene was also forming under the Cu islands. After covering the graphene-Cu islands with PMMA, Cu was etched and the released PMMA-graphene structures should have been transferred with the PMMA film to a new substrate and aligned with predefined structures for device patterning. Thermoplasticity of PMMA allows to lower the suspended PMMA-graphene films to the wafer level (anneal at 185 °C) and after PMMA removal, graphene was found to be properly attached to the substrate. The process succeeded with respect to graphene continuity and lowering, but because of the roughening of the SiO_2 surface during the process, the PMMA film could not be released from the oxide substrate in contrast to layer transfer protocols employed in aligned multilayer exfoliation. Also the overall process appeared too complex to be viable from the technological point of view and the development was stopped after these first experiments.

In addition to the grain formation, the low evaporation temperature of copper limits the optimal growth temperature on wafers more severely than with the copper foil, as small variations in the thermal gradient in the chamber may lead to complete evaporation of the copper film at some locations. This sets stringent requirements for the uniformity of the temperature profile, but is possible to control with modern tooling solutions.

Thus the solutions to problems related to the copper films on rigid substrates may be found by careful tuning of the deposition process such as the cooling rate and uniformity. Another approach is to use other catalysts, such as platinum, germanium or metal alloys.

3.3.3 PHOTO-THERMAL CVD ON PLATINUM

As mentioned above, CVD can also produce multilayer graphene if the catalyst has larger carbon solubility, as is the case with most catalytic metals such as nickel (0.6 % in weight) and iron. In the case of copper wit negligible C solubility, graphene grows on the surface with the hydrocarbon decomposition, but when the solubility is high, carbon diffuses into the metal. As the carbon solubility increases with temperature, carbon precipitation from the substrate upon cooling and leads into the formation of graphene on the surface. As the cooling continues, more carbon precipitates under the first graphene layer forming additional graphene sheets. As the crystalline ordering is energy and time dependent process, the quality of the underlying graphene layers decreases with the temperature. The layer thickness can be somewhat adjusted by the cooling rate because the solubility of carbon is rather low at moderate temperatures where the diffusion rate is still high; fast cooling freezes the carbon atoms into the metal lattice and slow cooling produces thick graphite. Optimal cooling rate for nickel has been found to be about 10 ºC per second, which in the best cases produces a mixture of mono- and bilayer graphene, but typically much thicker multilayer films.

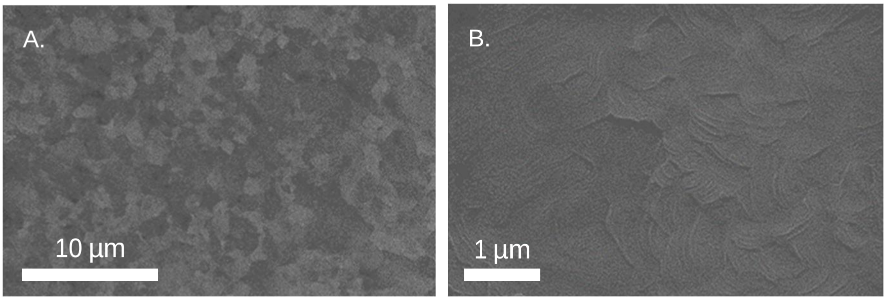

FIGURE 3.9 Scanning electron micrograph on platinum film (100 nm) on 1 µm SiO_2/Si after graphene deposition at 1000 °C. AFM images of the as grown surface can be found in FIGURE 3.13.

The carbon solubility in platinum (0.07 % in weight[61]) is a bit higher than in Cu and the published data is not sufficient to unambiguously determine if the growth mode is based on precipitation or self-limiting catalytic deposition. It may be that both modes coexist and it depends on the process conditions which is more dominant. Platinum is known from its high catalysis activity and is able to decompose methane at reasonably low temperature of 750 °C.[39] On the other hand, due to the high melting point of platinum, the evaporation is not limiting the deposition temperature as with copper. Also, the sputtered film maintains continuity upon the cooling process and even though the surface roughness increases slightly, the topology compared to sputtered copper films is practically planar.

We have deposited graphene on platinum from CH_4:H_2 with and without argon dilution, the Ar flow rate being two orders of magnitude higher than that of the reactive gases. In all the results, the most dominating feature is the improvement of the graphene quality with the reduction of the methane exposure. Especially without argon dilution, the high CH_4 exposure induces micron sized defect agglomerates within otherwise high quality graphene, with density decreasing as a function of the process pressure. This can easily be understood as a result of carbon precipitation. The agglomerates are not seen after argon diluted growth, where the increase in deposition pressure simply increases the overall defect density, which is typical to the lattice growth directly from the gas phase. In all cases the deposition temperature also increases the 2D/D and G/D ratios, but within a range comparable to statistical fluctuations in the quality of different graphene samples grown in identical conditions.

Graphene CVD on platinum has high prospects mainly due to the microscopic properties of wafers with sputtered platinum catalyst and the broader parameter range to produce high quality graphene.

3.4 GRAPHENE TRANSFER & PROCESSING

Graphene transfer is a necessity in most graphene production methods aiming to thin film components. Only in the case of epitaxial graphene on SiC, the growth substrate usually also provides the device template. All processes from Scotch tape exfoliation, stamping, transfer from CVD catalyst to a device substrate to printing of conductive or otherwise functional films from graphene dispersions are facing similar issues with purity, adhesion and doping. These same topics are crucial throughout the process sequence from growth and transfer to final component analysis.

3.4.1 TRANSFER METHODS

The transfer of CVD graphene from copper and platinum catalyst surfaces is typically based on either etching or electrochemical release, also known as the bubbling transfer.[39] In the case of growth on wafers, etching at the interface is very slow, but some groups have also reported successful release based on ultrasound and water to release the metal catalyst from the substrate for faster etching[62] or delamination from the graphene - catalyst interface with hot DI water[63]. In addition to the release, there are several options for the sacrificial support layer (typically PMMA), cleaning procedures for graphene from etch residuals, substrate pre-treatments to ensure proper adhesion and finally for cleaning to remove the residuals of the transfer support layer.

For graphene transfer from copper foils, copper etching in e.g. 0.1 M ammonium persulphate ($(NH_4)_2S_2O_8$) aqueous solution or 1 M iron chloride ($FeCl_3$) is the most common release method. Typically the graphene film grown on the back side of the foil is first removed in oxygen plasma. Different copper etchants have been applied and selection of the etchant can contribute strongly on the contamination and doping of graphene, in particular if not cleaned thoroughly. For platinum, etching is not an option, but the release is based on electrochemical reaction that produced hydrogen bubbles between the platinum and graphene.[39] If done carefully, it also allows reusing the platinum substrate. Bubbling transfer is also a reliable method for copper templates and similarly to the etchants, also the electrolytic solution, e.g. NaOH, needs to be carefully removed. Both of these methods are relatively simple, but require some handcrafting before they can be successfully applied in the transfer.

In the case of larger samples, some additional support structure is generally required. This is particularly important with all sample sizes when the etch residual cleaning is finished in isopropyl alcohol (IPA) to remove water from graphene surface,[64] as the absence of surface tension will otherwise sink the graphene/PMMA sheets that are typically floating on the surface of the liquid. The support will also allow drying the graphene surface before transfer to the final substrate. This is particularly important with transfer to structured substrates where water could be trapped inside voids and/or if graphene is aimed to remain suspended after the transfer. Also in transfer to polymer substrates the IPA cleaning is beneficial due to the thermal limitations in subsequent cleaning steps.

3.4.2 SUBSTRATE & DIELECTRIC

In practice, graphene is not isolated from the environment and due to the single atom thickness, the environment has a significant influence on its electronic properties. In practice, the charge carrier mobility is decreased by impurity scattering due to defects, adsorbed molecules and trapped charges inside the surrounding dielectrics, and by electron – phonon interactions between graphene and the dielectrics. The molecules at the surface, both those adsorbed and those in the substrate also dope graphene and shift the Fermi level. Therefore the properties of graphene are strongly determined by the selection of the surrounding materials and by the processing details.

Theoretically the charge carrier mobility in graphene is limited by the intrinsic acoustic phonon scattering to 200 000 cm^2/Vs.[65] This far, the highest mobilities of 100 000–150 000 cm^2/Vs have been measured from exfoliated graphene, either on *h*BN or suspended in vacuum,[66,67] whereas the mobilities measured from clean high quality graphene on ceramic dielectrics range from 2 000 to 25 000 cm^2/Vs, with the highest values obtained on both exfoliated and CVD graphene.[68,52] Thus the selection and preparation of the substrate are essential for graphene electronics and photonics, but the substrate surface chemistry has to be considered also from the point of view of adhesion.

The traditional method to ensure adhesion, already when the graphene was transferred with scotch tape from graphite to SiO_2/Si substrates, was to increase the surface hydrophilicity by argon plasma activation or chemical oxidation in e.g. RCA1-bath ($NaOH:H_2O_2:H_2O$ 1:1:5 at 60°C). Both of these treatments generate a large concentration of OH^- sites on the surface, which induce polarization in graphene and thus increase the adhesion properties. The drawback of this approach is that the charged OH^- groups at the interface inevitably increase charge carrier scattering in graphene.

In the opposite approach graphene adheres to the substrate via hydrophobic-hydrophobic interaction, where the van der Waals forces are due to spontaneous polarization. When the dielectric surface is inherently non-polar, such as some diamond like carbon (DLC) materials,[69] or covered with a thin layer of non-polar material, like a molecular monolayer of hexamethyl disilazane (HMDS),[70] scattering from the charges, ionic impurities and polarities in the substrate dielectric can be minimized. This leads into much higher charge carrier mobilities in graphene.

The reduction of charged impurities at the interface is essential also in the preparation of the top dielectric. Most commonly the top dielectric is deposited by ALD, but this process required OH, or similar bonds to initiate the growth. Initially the initiation was based on e.g. highly reactive NO_2 molecules that absorb on graphene,[71] but currently the established method is to evaporate a thin layer of metal on top of graphene and allow it to oxidize. The most convincing demonstration of the influence of the charged impurities on the charge carrier mobility in graphene was provided aside the success in using ozone as the ALD initiation layer. In trimethylaluminum (TMA) – H_2O based Al_2O_3 ALD process the first TMA pulse reduces ozone into oxide in Al_2O_3, resulting in a dielectric interface with strongly suppressed ionic impurity concentration, culminating to an increase in the charge carrier mobility in graphene with the addition of the top dielectric from 9000 to 16000 cm^2/Vs.[72]

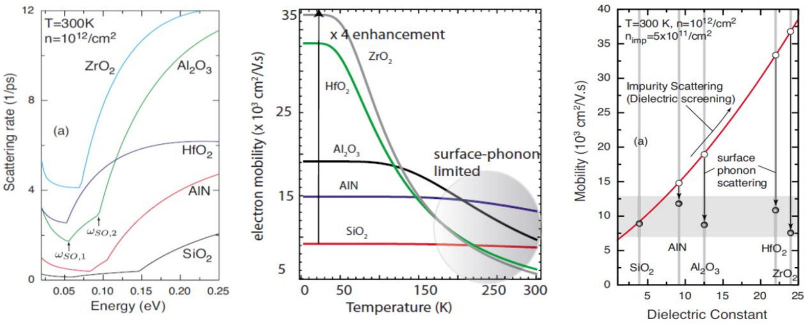

FIGURE 3.10 Theoretical impurity and A) surface phonon (SO) scattering at different graphene – dielectric interfaces with nominal charged impurity concentration of n_{imp} ~10^{11} cm^{-2}. B) High-k dielectrics are able to screen the ionic impurities, but as the electron – SO interaction increases with temperature, C) the net influence can be negative.[74]

In addition to ionic impurities in the vicinity of graphene, the charge carrier mobility is limited by coupling with the phonons in the surrounding dielectrics and topological effects related to the smoothness of the underlying dielectric. Hexagonal boron nitride (*h*BN) is considered as the most favorable dielectric substrate due to the atomic smoothness, absence of dangling bonds in the exfoliated films and high phonon energy,[73] which were also reported as the benefits of DLC with chemical mechanically polished surface[69].

In the selection of the top and bottom dielectric, the interplay between the effects of ionic impurities and electron – phonon interactions is relevant and therefore the optimal dielectric depends on the operation temperature of the devices. High-k dielectrics such as HfO_2 and ZrO_2 are superior in screening the charged impurities, but have low surface optical (SO) phonon energies that significantly limit the mobility in graphene above cryogenic temperatures.[74] For low temperature physics, ZrO_2 is expected to be superior to other oxides, but for room temperature applications, the reduction of ionic impurity concentration or a combination of dielectric with low surface phonon scattering with e.g. HMDS based screening of the ionic impurities are essential for high performance graphene electronics.

The electron scattering from remote surface phonons is additive, so that increasing the materials close to graphene will add the scattering probabilities by adding new frequency ranges subject to scattering. Therefore multilayer dielectrics or the selection of different top and bottom dielectric may not be optimal for the device performance. Though on the other hand, the benefits related to the selection of different top and bottom electrodes can be more dominating, especially when *h*BN or DLC can be used as the bottom dielectric.

3.4.3 GRAPHENE PATTERNING & CLEANING

The most common sacrificial transfer layer is PMMA and in addition, PMMA is also one of the most frequently used resists in graphene patterning. PMMA dissolves in many common solvents and the film can be easily removed with e.g. acetone, but the problem is in the residual layer that is tightly attached to graphene.

The most effective method for PMMA residual removal is to anneal the sample at ~350 °C in vacuum or preferably in forming gas (mixture of H_2 and inert Ar or N_2). In the most extreme, the whole PMMA film can be completely evaporated or sublimated by annealing, which is usually employed in the fabrication of suspended graphene membranes,[75] but more commonly the annealing process is only used for the final cleaning. This is one of the strengths of PMMA in graphene processing, since typical, e.g. novolak based, UV resists cannot be removed by baking but burn tightly into the substrate at temperatures well below 200 °C. For this reason PMMA can also be used as a surface protective layer when working with more contaminating photoresists.

As mentioned above, annealing is not always possible due to low thermal budget of the component. For example, in polymer electronics the common substrate materials, such as poly(ethylene terephthalate) (PET), have glass transition temperatures below 200 °C. Also in 2D hybrid structures, where graphene is combined with other 2D crystalline materials like dichalcogenides (e.g. MoS_2, WSe_2), the thermal budget can be very low. As bulky lubricants, many of these materials have air stabilities in the range of 350–400 °C,[76] so that the safe thermal budget for a monolayer is much less. In addition to PMMA residual removal, annealing process also removes water molecules from the interface between graphene and the substrate, which, as mentioned above, can be overcome by IPA based dry transfer. For the residual removal, several chemical treatments have been tested, including for example long acetic acid[77] and chloroform[78] cleaning. Also the room temperature ozone treatment prior to ALD deposition is expected to clean the graphene surface. [72]

The most common solution to protect graphene from resist and etch residuals after it is cleaned properly, is to grow a thin dielectric protective film on the surface. The requirements are that it should be possible to etch this film selectively to the substrate, resist and other layers in the component, by using etchants that do not contaminate. The same film can also be used as a hard mask in graphene patterning in oxygen plasma and as a replacement for lift-off resist residual plasma etch in contacting. Typical protective films are Al_2O_3 and SiO_2. The SiO_2 protective film is typically formed by evaporation, where as Al_2O_3 is grown by ALD on top of thin evaporated and oxidized Al (< 1 nm).

3.4.4 CONTACTING

Reliable and reproducible contacting is one of the major issues in the graphene technology and several different approaches for the minimization of the contact resistance have been proposed. The contact resistance includes, in addition to the actual dissipation between graphene and the metal, also the losses due to the pn-junction that forms in graphene close to the metal edge due to the doping of the graphene by the metallic contact.[79,80] Therefore the contact resistance not a constant, but a function of the Fermi-level in graphene and it does not scale with the area of the contact. The way the transition segment affects the contact resistance, also depends on the voltage bias and frequency.

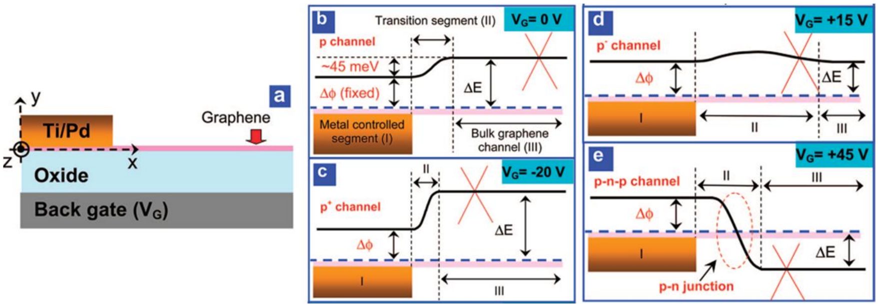

FIGURE 3.11 Surface potential profiles of the graphene transistor in the contact region, with different gate voltages. Metal controls the chemical potential of graphene on segment (I) and gate voltage on segment (III). Depending on the gate voltage, there may even be a pn-junction at the transition segment (II). [80]

The charge transfer between the 2D graphene and 3D metal has also other peculiarities, as it seems that the transport through the edge of graphene is favoured over transport between graphene and parallel contacting metal film. This has been demonstrated by the realization of a 1D contact with graphene edge only, providing total contact resistance at the level of normal planar 2D contacts.[66] Therefore the strategies for contacting include damaging graphene with plasma etching or lithographically, in order to increase the edge areas exposed to the metal. This also helps in reducing the influence and thickness of small residues of polymers that may otherwise prevent the formation of proper 2D contact.

These effects make it practically impossible to make any comparison between different metals or contacting methods analysed in different publications and the reported results are often seemingly contradictory. Usually a thin layer of reducing metal, such as Ti or Cr, is applied between the primary conducting metal, such as gold or palladium, and graphene to clean the junction and to improve the adhesion.

3.5 APPLICATIONS OF CVD GRAPHENE

Graphene has enormous prospects in various different applications, and due to the equally enormous research devotion, the progress of the technology, both in the fabrication and in the application development, has been exceptionally fast. In this chapter, some basics and prospects of the major application areas of CVD graphene are very shortly addressed. At the end, a bit more attention is given to CVD graphene in biosensing and to the related technological challenges.

3.5.1 ELECTRONICS

Graphene is an ambipolar semimetal, in which electric field can be used to tune the high mobility charge carriers continuously between electrons and holes in concentrations as high as 10^{13} cm^{-2}.[35] The transition between n- and p-type conductivity is represented in the electronic band diagram as a point (Dirac point) where the conical valence and conduction bands meet (see e.g. Figure 3a). The theoretical density of states at this point is zero, but some conductivity remains due to the small p-and n-type puddles.[81] Close to the Dirac point the charge carriers in graphene behave as relativistic particles with speed $c/v_F \approx 300$. The resistivity at the Dirac point is high but it decreases rapidly with the increase of charge carriers due to their high mobility.

The most basic device concept in graphene electronics is the graphene field-effect transistor (GFET). It is the basis not only for RF-electronics devices, rectifiers and inverters, but also for most sensor applications, photonics and tunability of MEMS applications. GFET is simply the analogue to the controlled continuous shift of the Fermi-level with external field, inducing a transition from p-type conductor to resistor and further to n-type conductor. GFET is not similar to semiconductor FETs with high on/off ratios of the order of 10^6, but rather a tunable ambipolar conductor as also in the resistive state the conductivity is non-negligible. The GFET on/off ratio is typically only around 5–10, which is a severe limitation for digital applications.

The extraordinary intrinsic properties of graphene allow for functionalities beyond the capabilities of other materials. A good example is ambipolarity, which allows completely new non-linear devices for RF electronics, including full wave rectifiers and inverters; as an efficient inverter operation can be performed in a single graphene device, realization of the same operation would require a complex circuit on silicon electronics.[82] The high mobility and ambipolarity also facilitate terahertz signal mixing and frequency multiplication.[83] Another intrinsic property is the atomic thinness that allows contacting sensitive materials without induced strain, leading to improved performance of otherwise traditional solid state components. And the tunability of the Schottky-contact forming between silicon and graphene can be utilized in solar cells[84] but also form a new type of gate controlled switch, graphene-semiconductor barristor[85].

RF APPLICATIONS

At high frequencies, the low on/off ratio is not a problem as long as there is frequency gain with low noise. Such RF LNA operation has been demonstrated with GFETs up to 155 GHz[69] and in addition to the material and process optimization, the key feature in the design is to optimize the transconductance by short channel lengths (sub µm) and small channel capacitances. CVD graphene is not single crystalline and the grain boundaries inevitably affect the charge transport, but in the wafer scale demonstration of GFET fabrication, the device performance of 155 GHz GFETs was rather uniform across the wafer, with no significant deviations that could have been attributed to grain boundary effects.

Even though the high charge carrier mobility makes GFETs attractive for high frequency applications, the mobility decreases with the carrier concentration and may not be, after all, the most important property. At the current state of the art technologies, the channels are already so short that the major limitations to the device speed are not so much related to the carrier mobility, but in parasitic short channel effects which can be significantly reduced by graphene with thickness well below the channel pattern dimensions.[86] The confinement of the signal into atomically thin sheet allows immediate modulation response without the parasitic delays.

Close to the Dirac point the charge carriers in graphene are ballistic. The mean free paths can be as large as 1 µm at room temperature[67] and over 10 µm at the low temperature regime[66] facilitating ballistic devices such as high frequency transistors with strongly reduced energy consumption. Also the pseudospintronics approach, relying in the room temperature superfluity in graphene bilayers,[87] can lead to new low energy logic devices such as the bilayer pseudospin FET (BiSFET).[88] These device concepts are at the level of fundamental research regarding both the device fabrication and logic circuit design and simulation.

FLEXIBLE APPLICATIONS

The atomic thickness makes graphene were flexible at the length scales of the human perception, even though the structure is rather rigid at the atomic length scales. The carbon-carbon bonds are strong, making the material very tough and the hexagonal atomic cell structure allows for small deformation under tension. Theoretically pristine graphene can withstand >15 % strain without breaking and most grain boundary arrangements have similar characteristics or can withstand at least 10 % strain.[89] Even though the grain boundaries in CVD graphene are not as strong as the perfect lattice, the performance of CVD graphene in devices has not been found to degrade before the surrounding materials have failed at e.g. 6 % strain[41].

The small or moderate influence of the substrate to the performance of the graphene devices allows the adaptation of nearly all graphene devices on flexible substrates. There are, however, some practical limitations due to the surface smoothness and purity of polymer substrates available. Many electronic devices, such as RF transistors and GFET based sensors have already been demonstrated on flexible substrates and their performance after bending has not degraded.

FLEXIBLE TRANSPARENT CONDUCTOR

One of the simplest applications of graphene in flexible electronics and photonics is transparent electrode or conductor. Typically the transparent conductor in user interfaces such as displays and touch screens has been indium-tin oxide (ITO), but as these devices are evolving lighter and flexible, many materials have to be replaced. ITO, for example, is very brittle and it degrades rapidly and drastically with bending. The conductivity of single layer graphene (250–600 Ohm/sq) is already at the level of some commercial flexible ITO films (e.g. TDK's FLECLEAR with R_S = 600 Ohm/sq), but the transmission is much higher (T ~ 97 % for single layer graphene, and 85 % for ITO). Graphene layers can also be stacked on top of each other's to form a multilayer conductor. Each layer from 2 to 4 improves the conductivity and increases the absorption by 2.3 %. The 4-layer graphene can almost reach the performance of the best ITO on a rigid substrate, but in addition it does not degrade with bending. It has to be remembered, however, that graphene is not the only possible successor for ITO, but materials such as carbon nanotube networks, conductive polymers and different metallic grids and fabrics are also developing rapidly.

One of the major issues and benefits of graphene in electrode applications is related to the tunability of the conductivity and work function by doping. The stability of the doping is still under development, though many promising approaches have been reported in addition to unstable HNO_3, such as TFSA,[90] AgCl,[91] $FeCl$,[92] and MoO_3.[93] Even though most of these are susceptible to evaporation, sealing of the devices will increase the durability. Work-function is particularly important in OLEDs, and the ability to tune the work-function of graphene by doping[94] allows direct charge transfer with the organic light emitting materials. For example, MoO_3 doped graphene provided much improved OLED characteristics to ITO, despite the slightly lower sheet resistance.[93]

2D WORLD

Graphene is not the only 2D crystalline material, but the selection ranges from insulators such as *h*BN to semiconductors (MoS_2, WSe_2), allowing high on-off ratios for atomically thin transistors and direct absorption and generation of photons. Like with graphene, the applicability of these materials is not limited to rigid substrates. The range of materials available is tremendous and this research has just begun. The potential becomes even more pronounced as the 2D materials are considered as building blocks of future device architectures.

One of the most promising examples has been vertical graphene – WS_2 – graphene transistors, allowing utilizing the high mobility and tunable chemical potential of graphene with atomically thin WS_2 channel. These devices combine on-off ratio above 10^6 with high flexibility and transparency[37] – and the vertical operation sets no restrictions for lateral miniaturization. The production technologies for most 2D crystals, including WS_2, is however still rather limited, like with graphene still 5 years ago, allowing only experimental device fabrication with exfoliated crystallites. In the future however, vertical stacking of such devices will facilitate packing densities and functionalities far beyond our imagination.

3.5.2 PHOTONICS

In the first demonstrations, the detection of photons with graphene was based on the pn-junction generated by the graphene-metal contact. There the active detector area is a narrow line with length determined by the contact edge and as the absorption of photons incident to a single layer of graphene is 2.3 % at highest, the detector efficiency is rather modest. However, the detector has very high speed, demonstrated up to 40 GHz and predicted to reach over 500 GHz, possibly limited only by the contact resistance.[95]

Since then, the various techniques and phenomena have been developed for increased photon – graphene interaction. One of the simplest ideas is to increase the interaction time by placing graphene detector into a node of an optical cavity or on top of a waveguide, providing an optical mode parallel to graphene. The light-matter interaction has also been enhanced with e.g. multilayer graphene, charge transfer from quantum dots[96] and nanostructure induced plasmon resonance[97]. Another approach is to employ the hot carrier multiplication (Auger processes) by fast separation of the electron – hole pairs.[98] Recently, the wide band absorption efficiency of the detection has been improved by vertical tunnelling structure to extract the hot photogenerated carriers into another graphene layer through a thin insulating barrier.[99]

In the case of integrated photonics, the interaction length is automatically increased when the optical mode and graphene are parallel to each other's with adequate overlap, allowing graphene to absorb the full signal. The ability to tune the graphene absorption with external field allows designing both detectors and modulators based on graphene. The modulator concept and operating principle is illustrated in FIGURE 3.12. An interaction length of a few tens of microns was found to be able to modulate the optical mode with 3 dBm up to 1 GHz.[99] This technology has high prospects in optical signal processing, for example in optical data links, as the current alternatives for fast modulation are far too expensive.

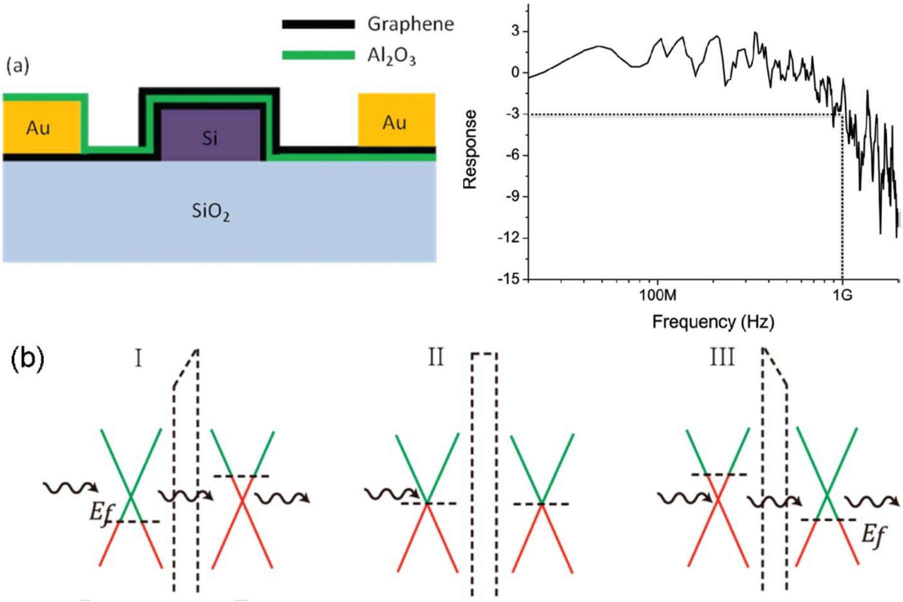

FIGURE 3.12 Dual-layer graphene based optical modulator. The modulator operation is based on shunting the direct band-to-band absorption in graphene for photon energies under modulation threshold energy. With dual-layer graphene, the layers can gate each other into opposite transparent stages, whereas if the other electrode were a metal, it would always absorb. This first modulator at 2012 provided above 3 dBm response up to 1 GHz frequencies.[99]

THz Detection

In addition to THz signal mixing and frequency multiplication on the basis of ambipolarity, graphene has very high prospects in THz detection and several cryogenic and room-temperature detector concepts have been recently demonstrated. The detection of THz photons with graphene FETs is generally based on the behaviour of hot electrons, generated either by direct absorption of the THz radiation or THz oscillations collimated to GET channel by metal antenna. The fast relaxation of excited electrons results in a fast response (10 ps range),[100] whereas the small electron heat capacity and weak electron-phonon coupling efficiently increase the electron temperature[101] and the amount of photogenerated carriers[102].

Room-temperature detection can be based on plasma waves hosted by the 2D electron gas in graphene,[103] relying on the high mobility in graphene at high carrier densities.[102] The plasma waves are launched by modulating the potential difference between the gate and the channel with the incoming THz radiation and the non-linearity of the coupling and transfer characteristics in GFET rectify the signal. The non-linearity between the drain and the source can be achieved e.g. by coupling the antenna with the gate and the source.[102] Another room-temperature detection scheme relies on the electron temperature gradient generated with dissimilar heat sink properties of the source and drain electrodes (Au, Cr)[100] and schemes based on vertical graphene – 2D hybrid structures have also been proposed.[104] The detection in cryogenic temperatures is based on typical bolometric device principles, relying e.g. on the temperature dependent properties of gapped bilayer graphene[101] or superconducting tunnel junctions.[105]

Rapidly developing THz detection applications put high prospects for ultra-fast telecommunications (space satellites, space-to-Earth data links), meteorology and climatology, molecular spectroscopy, public security and medical imaging. There is a need for room temperature ultra-fast THz emitters, detectors, modulators, spectroscopy systems and sensors. For example, the prospects of THz spectroscopy in security are tremendous. THz based security scanners for non-invasive body detection are already in use, but in addition, every explosive and narcotic has a distinct signature in the THz spectra, potentially enabling their identification from the THz transmission spectra of postal packages. The ability of THz wave sensing to detect substances, such as carbon monoxide and other toxic gases, through smoke and even concrete walls, substantially outperforms other detection methods. The wider utilization of THz systems clearly depends on the development of room temperature emitter and detector solutions.

3.5.3 BIO-SENSING

Compared to the complexity most other applications, the operation principles of the GFET in sensor applications are rather simple. Instead – or in addition to – of the external gate voltage, graphene is gated by adsorbed charged molecules and the changes in conductance are recorded as the sensor response. Due to the atomic thickness allowing the local field to influence the full depth of graphene and due to the high dynamic response to the field close to the Dirac-point, graphene FETs are highly sensitive sensor templates. As a drawback, however, also the unspecific response is generally high. The major challenges in the development of graphene sensors are therefore in the selectivity.

Gas sensing with nonfunctionalized graphene demonstrates the extreme sensitivity and at the same time, it is a good example on the importance of selectivity and introduces one typical source of error affecting the performance of selective graphene sensors. In the early demonstrations of GFET sensitivity to gases, the adsorption of gas molecules was detected by the doping induced change in GFET channel resistivity. The doping is not a gate-induced effect, but results from the overlap of the electronic levels of graphene and the adsorbed molecules. The interaction between graphene and HNO_3 is particularly strong and GFET is able to detect the adsorption and desorption of individual molecules. But despite the fact that different molecules generate discrete impurity levels into the density of states of graphene, shift the Dirac peak position and may alter the shape of the IV-curve, the identification of the gases is challenging. The only demonstration of the identification has been based on the different noise spectra generated by different molecules, thereby utilizing the low noise of graphene.[106] In general, selectivity is brought to GFETs with functionalization and the spontaneous adsorption and desorption processes need to be minimized.

In biosensing, the molecules to be detected can be lipids, peptides, proteins or other biomolecules with much larger size than the simple gas molecules. Small biomolecules may contain 20 amino acids, each with usually more than ten atoms and larger biomolecules can be several nanometers in diameter. Their unspecific binding would generate a mixture of different orientations, making their identification from the electrical or noise spectrum even more challenging. The functionalization of GFETs for biosensing is based on receptor molecules that are the same as, or similar to, the receptors that specifically bind to the analyte molecules in living organisms.

The established research method for graphene functionalization is based on linker molecules that attach non-covalently to graphene. In the functionalization process graphene is first covered with the linker molecules (e.g. thiols[107]) which provide sites for the receptors. Then the unreacted linker molecules are passivated to prevent unspecific binding from the analyte sample. This procedure contains multiple steps, with rinsing after each step, and the adsorption times are typically rather long. Also the surface coverage of the receptors can be low.

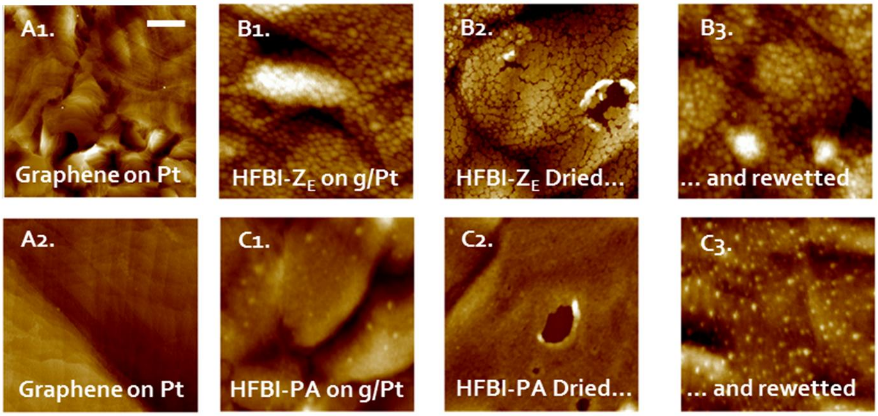

FIGURE 3.13 AFM images of self-assembled receptor module monolayers on graphene. A) Graphene deposited by PT-CVD on Pt(100 nm)/SiO_2(1 µm)/Si wafers. B) HFBI-Z_E and C) HFBI-Protein A after self-assembly, drying and 5 minute rewetting. AFM images B1, C1, B3 and C3 were done in liquid buffer. Scale bar in A1 equals 1 µm, other images are 1 µm in size. The height scale in all images is 15 nm. [I]

We have developed a method to obtain high surface coverage with a single functionalization step, by using receptor modules where the receptor is fused with a hydrophobin protein by genetic engineering. [I] Hydrophobins are a special class of proteins that have evolved to optimize the liquid – air interface in the growth of fungi in nature; or in this case, the hydrophobic graphene – liquid interface. Hydrophobins self-assemble into a dense molecular monolayer, but the structure and density of the monolayer can be affected by the fused receptor, which may induce steric hindrances or electrostatic effects during the self-assembly. For example, when the receptor moiety is larger than the HFBI, as the Protein A receptors, steric hindrance prevents the formation of a dense HFBI monolayer but instead, the packing density is defined by the size of the Protein A.

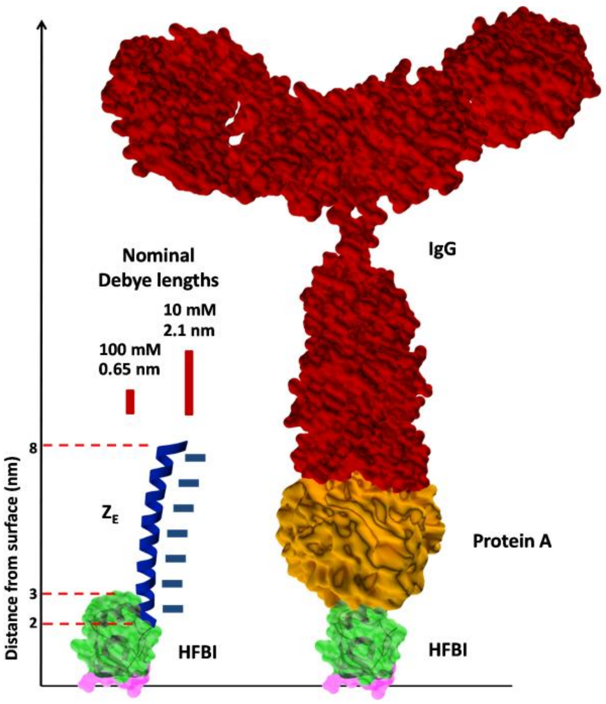

FIGURE 3.14 Schematic illustration of the length scales related to the determination of the effective detection range. [I]

The packing density is important, because the HFBI protein is rather large compared to the ionic screening lengths in typical physiological media such as urine or blood, which have ionic concentrations at the range of 100 mM/ml. This corresponds to a ionic screening length, or Debye length, of 6 Å, whereas the HFBI height is 3 nm. However, the liquid content inside typical proteins has been estimated to be only in the range of 10–30 %.[108] It is not precisely known how the ionic screening evolves in such system, but the confinement and the small density of the water molecules in the proteins most likely reduces the overall polarizability.[109] Therefore the double layer formation by mobile ions in the liquid occurs mainly above the proteins, with much smaller contribution by the volume of mobile liquid inside the proteins. This makes it possible to measure charges also beyond the Debye length from the graphene channel, as demonstrated in our experiments with HFBI – Z_E and HFBI – Protein A receptor modules in the detection Z_R, the counter peptide of Z_E, and immunoglobulin IgG. The densities of the receptor module monolayers are presented in FIGURE 3.13 and the related length scales in FIGURE 3.14.

The biosensor performance was demonstrated with a small strongly charged pair of zipper peptides, Z_E with -7e charge and Z_R with opposite charge at pH 7. The schematic of the sensor measurement set-up is presented in FIGURE 3.15A. The introduction of the negatively charged HFBI – Z_E receptor module layer induces additional negative gating on graphene, as seen from the shift in the Dirac peak position in FIGURE 3.15C. The subsequent biorecognition of the analyte (Z_R) neutralizes the charge and returns the Dirac peak into the original position.

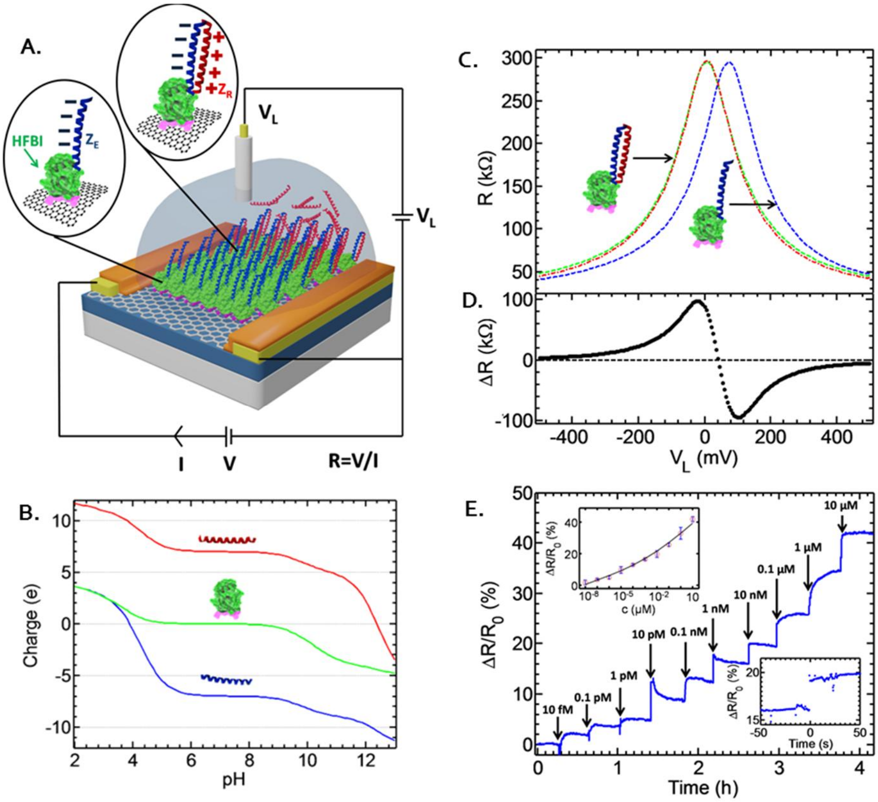

FIGURE 3.15. A) Schematic of the biosensor measurement setup, B) charge states of the biomolecules used in the demonstrator as a function of pH, C,D) biosensor response to the functionalization with charged biomolecules (HFBI – Z_E) and subsequent biorecognition of counter peptide Z_R resulting in a charge neutralization. E) Sensor response as a function of analyte concentration and time. [I]

The initial detector response to the analyte is fast, typically less than 1 s, reflecting the immediate receptor – analyte binding process (see the lower inset in FIGURE 3.15E). After the initial response, stabilization to the biological equilibrium, fluidic curls and mobile charges in the sensor substrate induce transient towards the final resistance value. At very low analyte concentration the association rate is strongly limited by the finite mass transport in the buffer.[110] The dynamic range of the detection was found to extend from 10 fM to 10 μM analyte concentration. Already the extremely low 10 fM analyte concentration induced a saturated response of 2 %, an order of magnitude higher than the noise level in the measurement. Similar response characteristics were measured for the large IgG protein, though with only 30 % change in $\Delta R/R_0$ at the highest analyte concentration.

The emerging trend of preventive health care is directing research towards point-of-care (PoC) diagnostics and quantitative detection of low concentration biological and chemical species such as disease markers.[111] Particular potential is in solutions that are label free and can facilitate integration into portable electronic PoC units or mobile phones. The quantitative electrical detection of the analytes recently demonstrated with carbon nanotube (CNT), graphene and semiconductor nanowire based sensors[112,113] bear high potential in this respect. These novel sensors can provide high sensitivity together with flexibility in both device design and miniaturization, enabling realization of easy operation on low-cost analysis platforms suitable for preventive health monitoring. Electrical sensors will complement the existing label-free techniques such as mass spectrometry and surface plasmon resonance, which require expensive laboratory equipment.

Graphene FET with receptor module based functionalization provides a sensitive platform for quantitative bio detection with electronic readout. The platforms can be disposable pre-programmed PoC sensing units, programmable PoC units or complete lab-on-chip solutions. In the case of disposable units, the important aspects are the ability to dry the receptors and to fabricate the sensors on low-cost polymer sheets with integrated polymer fluidics. For programmable PoC units, the ease of functionalization is the key advantage over other sensor concepts, whereas with Lab-on-Chip applications, there would be no advantage to linker based functionalization until the library of the receptor modules would cover the needs of the required sampling.

Another important aspect in the receptor module self-assembly is the controlled orientation of the receptors, not only providing an optimal surface coverage of active sites for the analytes in biosensing, but also in the framework of bio-solid interfacing in general.

In addition to GFETs, graphene can be utilized in biodetection also as a template for surface enhanced Raman spectroscopy (SERS), allowing to record the chemical fingerprint of biomolecules with low excitation powers. Graphene can increase the SERS activity of typical SERS substrates based on e.g. silver nanoparticles and simultaneously act as a biocompatible barrier between the metal nanoparticles and the biological substance. In this thesis, the enhancement of TiO_2 nanoparticle Raman response was investigated and found to be proportional to graphene defect density. [III]

3.6 PROSPECTS OF GRAPHENE TECHNOLOGY

Despite the short experimental history of graphene, the fabrication technology has already evolved from handcrafting to industrial scale production due to the vast interest and potentials assigned to this material. The processing technologies are proceeding with the understanding of the interaction between graphene and environment and this will eventually turn graphene into a standard material in thin film and semiconductor technology.

The whole class of 2D crystalline materials is currently rising to support the 2D revolution started by graphene. From the fabrication point of view, they are currently on the handcrafting phase, though some large scale deposition methods have already been demonstrated.

As shortly reviewed, numerous applications have already been proposed and demonstrated for graphene in electronics, photonics and sensing. The short term prospects in electronics are mainly in thin, conductive transparent films, whereas the high value applications still require massive efforts and development of other 2D materials. Photonics, THz and sensing device concepts are still new, but can already outperform existing solutions

4 SUMMARY & CONCLUSIONS

Traditional microelectronics processes have not always been traditional. They have evolved both steadily with time and experience and as quantum leaps with new innovations, such as the invention of the microelectronics itself not so long ago. The first solid state transistor was merely a point contact to a semiconductor[114] and for the first integrated circuit; two transistors were bonded together on a germanium wafer.[115] These resemble both the photonic crystals and graphene in their early phases, but whereas photonic crystals have their inspiration in nature, graphene is something that “cannot” exist.

The full utilization of 3D photonic crystals explored in this thesis will remain a challenge for the future generations, as mimicking nature in them is too demanding for the existing fabrication technologies. Integrated 3D PhCs may find applications in bioprocessing already with the current state-of-the-art and with the evolvement of the fabrication technologies in other fields, they may eventually become available also for the integrated photonics in signal processing.

Graphene, on the other hand, can either be part of the progress of microelectronics or an onset for the next quantum leap in technology development – or both. It can boost the development of the current microelectronics as a new functional material and help in transferring some applications into flexible transparent user interfaces. Or it can be the forerunner of the new 2D crystalline technology that completely revolutionizes the microelectronics industry.

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Series title and number

VTT Science 100

Title	**Integration of 2D and 3D nanostructure fabrication with wafer-scale microelectronics** Photonic crystals and graphene
Author(s)	Sanna Arpiainen
Abstract	This Thesis considers different aspects of heterogeneous integration of 2- and 3-dimensional nanostructures with today's microelectronics process flow. The applications in the main focus are integrated 3D photonic crystals on a photonic chip and graphene biosensors, both exploiting directed self-assembly but at different length scales. View point is from the fabrication and integration challenges, but the future prospects of the selected fields of applications are also reviewed. Utilization of new materials and structures in microelectronics and photonics applications typically requires integration with the existing platforms. The fabrication processes are optimized for the established materials and generally require both high thermal budget and elemental purity to avoid contamination, thus the novel elements need to be integrated at the back-end phase and aligned with the pre-existing structures on the substrate. For that, there are basically three alternatives; (i) directed self-assembly, (ii) high precision placement and (iii) methods exploiting thin film growth and lithographic definition of the nanostructures. Whereas the 2D photonic crystals can be conveniently fabricated with advanced nanolithographic methods such as deep-UV lithography and etching, for the 3D photonic crystals the lithographic approach may not be the most efficient method. This Thesis presents a scalable directed self-assembly method for the fabrication of artificial opal photonic crystals on a photonic chip and defines the processing steps required for the inversion of the opal with silicon to obtain full photonic band gap without damaging the underlying chip. The existence of the full photonic band gap in the inverted silicon photonic crystal is demonstrated by measurements via the integrated waveguides. The integration of graphene with microelectronics processes is, in principle, simple due to the sheet-like structure of the material. The atomically thin 2D crystal can be processed in a manner similar to traditional thin films, as soon as graphene is on the substrate. This Thesis presents different methods aiming for scalable production of high quality graphene on different substrates, ranging from mechanical exfoliation based on step-and-stamp printing to rapid chemical vapour deposition with subsequent thin film transfer, which is the most promising method for large area graphene production. From the physical and chemical point of view, however, graphene is not a traditional thin film. Due to the single atom thickness, environment has a significant influence on the electronic properties of graphene. This has to be taken into account in the processing and design of graphene devices, but it also provides means to highly efficient sensing applications. The key issue in graphene based sensors is in the specific recognition, which has to be introduced by functionalization. This Thesis addresses the functionalization of graphene field-effect-transistors with self-assembled bio-receptors, utilizing non-covalent hydrophobic interactions between graphene and hydrophobin proteins.
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Nimeke	**2D ja 3D -nanorakenteiden integrointi kiekkotason mikroelektroniikkaan** Fotonikiteet ja grafeeni
Tekijä(t)	Sanna Arpiainen
Tiivistelmä	Tämä väitöskirja käsittelee 2- ja 3-dimensionaalisten nanorakenteiden integrointia mikroelektroniikan prosesseihin. Sovelluksista keskitytään valokanaviin integroituihin 3D-fotonikiteisiin ja grafeenibioantureihin; molempien valmistuksessa turvaudutaan ohjattuun itsejärjestymiseen, vaikkakin eri mittakaavassa. Aiheita lähestytään valmistuksen ja integroinnin haasteiden näkökulmasta, mutta kirjassa käsitellään sovellusten tulevaisuuden potentiaalia ja näkymiä myös yleisemmällä tasolla. Uusien materiaalien ja rakenteiden tuominen mikroelektroniikan ja fotoniikan sovelluksiin vaatii tyypillisesti niiden integrointia olemassa oleviin sovellusalustoihin. Vakiintuneet valmistusprosessit on kuitenkin optimoitu perinteisesti käytettyjä materiaaleja silmällä pitäen, ja ne vaativat yleensä korkeita lämpötiloja, joissa uusien materiaalien aiheuttama kontaminaatioriski on suuri. Siksi integrointi valmistusprosessin loppuvaiheessa on usein ainoa vaihtoehto, ja haasteeksi muodostuu uusien rakenteiden kohdistaminen valmiisiin elementteihin. Tähän on käytännössä kolme vaihtoehtoa: (i) ohjattu itsejärjestyminen, (ii) korkean tarkkuuden sijoittelu ja (iii) menetelmät, jotka hyödyntävät perinteistä ohutkalvojen kasvatusta ja kuviointia nanorakenteiden valmistukseen. Siinä missä 2D-fotonikiteitä voidaan helposti valmistaa käyttäen kehittyneitä nanolitografiamenetelmiä kuten DUV litografiaa ja etsausta, litografinen lähestymistapa ei välttämättä ole tehokkain menetelmä 3D-fotonikiteiden valmistukseen. Tässä väitöskirjassa esitellään skaalautuva, ohjattu itsejärjestymismenetelmä keinotekoisten opaalien valmistukseen suoraan haluttuihin paikkoihin muiden fotoniikan komponenttien lomaan. Lisäksi määritellään prosessit, joiden avulla opaalit voidaan kääntää piifotonikiteiksi komponentteja vahingoittamatta. Toimivassa piifotonikiteessä on aallonpituusalue, jossa fotonien liike on kielletty, ja tämän alueen olemassaolo todennetaan mittaamalla fotonikiteen läpi kulkevan valon spektri integroituja valokanavia käyttäen. Grafeenin integrointi mikroelektroniikan prosesseihin on periaatteessa yksinkertaista, sillä materiaali on tasaista kalvoa, jota voidaan prosessoida kuten perinteisiä ohutkalvoja, kunhan se onnistutaan saamaan halutulle pinnalle. Tässä väitöskirjassa esitellään erilaisia menetelmiä, joiden tarkoituksena on ollut tuottaa korkealuokkaista grafeenia suuressa mittakaavassa erilaisille pinnoille. Lisäksi esitellään mm. grafiitin mekaaninen atomitasojen suuntainen viipalointi "askella ja leimaa" -painomenetelmällä sekä grafeenin nopea kaasufaasikasvatus metallin pinnalle ja siirto halutulle alustalle, joka on tällä hetkellä lupaavin menetelmä laaja-alaiseen grafeenin tuotantoon. Fysiikan ja kemian näkökulmasta grafeeni ei kuitenkaan ole tyypillinen ohutkalvo. Materiaalin atomäärisen ohuuden takia ympäristöllä on merkittävä vaikutus grafeenin sähköisiin ominaisuuksiin. Tämä on muistettava huomioida komponenttien valmistuksessa ja suunnittelussa, mutta se tekee grafeenista myös erityisen herkän sähköisen anturimateriaalin. Grafeeniin perustuvien antureiden suurin haaste on erilaisten kohdeaineiden tunnistaminen. Tässä väitöskirjassa käsitellään grafeenitransistorien integrointia itsejärjestyvien bioreseptorien kanssa, jolla tavoin saavutetaan herkkä ja valikoiva bioanturi.
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