Department of Applied Physics

Printed and low-temperature-processed indium oxide thin-film transistors for flexible applications

Jaakko Leppäniemi

Aalto University

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Abstract

The convergence of printing and microelectronic technologies, often called printed electronics, is best embodied in printed thin-film transistor (TFT) semiconductor devices. TFTs, that are the key components in displays and flat panel X-ray sensors, are conventionally fabricated on rigid substrates from amorphous silicon (a-Si) using vacuum-processes and a high process temperature (> 250 °C). With the existing market pull for flexible and high-resolution organic light emitting diode (OLED) displays, novel semiconductor materials, such as organic and metal oxide (MO) semiconductors, are being developed to yield TFTs with flexibility and electrical performance beyond that of a-Si. Organic TFTs (OTFTs) can be printed and processed at low-temperature (< 150 °C) on flexible substrates, whereas MO TFTs, that readily provide superior performance to both OTFTs and a-Si TFTs, are either vacuum-processed or require high-temperature processing (> 300 °C) when they are solution-processed.

The thesis work focuses on the fabrication of MO semiconductors using printing processes and includes material, ink, and process development, as well as fabrication, characterization, and modelling of the printed MO TFT devices. We show in **Publication [I]** that thin, printed In_2O_3 layers can be used in enhancement-mode TFTs when the devices are stabilized using a post-contact annealing step at low-temperature. Moreover, we demonstrate, for the first time, that flexography-printed In_2O_3 layers on flexible plastic substrate can be used in TFTs whose performance is beyond that of a-Si TFTs or printed OTFTs. In order to lower the annealing temperature of the MO materials, **Publication [II]** and **Publication [III]** introduce a low-temperature annealing method where low-wavelength far ultraviolet (FUV) exposure and thermal annealing are combined to reach the processing temperature (~150 °C) for an inkjet-printed In_2O_3 semiconductor that is compatible with low-cost plastic substrates. Finally, **Publication [IV]** demonstrates that high-gain depletion-load inverters can be fabricated via inkjet printing by exploiting the thickness-dependent electrical properties of the In_2O_3 semiconductors.

In summary, this thesis demonstrates that MO semiconductors can be deposited using industrially-relevant printing processes and processed at low-temperature on flexible substrates. This could lead, in the future, to the use of printed MO TFTs in flexible applications, such as biosensors, flexible displays, large-area sensors, and integrated and radio-frequency circuits. The potential of these applications is also analysed in this thesis.

Keywords printed electronics, metal oxide thin-film transistors, flexographic printing, inkjet printing, low-temperature annealing, depletion-load inverter

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Tiivistelmä

Painotekniikkaa ja mikroelektroniikkaa yhdistävää tieteenalaa kutsutaan usein painetuksi elektroniikaksi. Painettuja ohutkalvotransistoreita (engl. thin-film transistor, TFT) voidaan pitää näiden teknologioiden yhdistelmän huipentumana. Näytöissä ja digitaalisissa röntgendetektoreissa olevat amorfiseen piihin perustuvat (a-Si) TFT:t valmistetaan perinteisesti käyttäen tyhjiökasvatusmenetelmiä, korkeaa valmistuslämpötilaa (> 250 °C) ja taipumatonta alustaa. Uusien puolijohdemateriaalien, kuten orgaanisten- ja metallioksidipuolijohteiden, kehitystä ohjaavat taipuisien sekä orgaanisiin valodiodeihin (OLED) perustuvien näyttöjen asettamat vaatimukset komponenttien taipuisuudelle sekä puolijohteen suorituskyvylle. Orgaanisia ohutkalvotransistoreita (OTFT) voidaan valmistaa taipuisille alustoille käyttäen painomenetelmiä ja matalaa lämpötilaa (< 150 °C), kun taas metallioksideihin perustuvat TFT:t tarjoavat näitä paremman suorituskyvyn mutta ovat valmistettu joko käyttäen tyhjiömenetelmiä tai liuosprosessia ja korkeaa lämpötilaa (> 300 °C).

Tämä väitöskirja keskittyy metallioksidipuolijohteiden valmistukseen painotekniikoita käyttäen ja sisältää tietoa materiaalien, painomusteiden ja valmistusprosessien kehittämisestä, sekä painettujen TFT:iden valmistuksesta, karakterisoinnista ja mallintamisesta. **Julkaisussa [I]** osoitetaan, että ohuita, painettuja indiumoksidikerroksia (In_2O_3) voidaan käyttää avaustyypin transistoreissa, kun valmiit komponentit stabiloidaan paistamalla niitä matalassa lämpötilassa. Tämän lisäksi osoitetaan ensimmäisen kerran, että fleksopainoa käyttäen voidaan valmistaa taipuisalle alustalle In_2O_3 TFT:itä, joiden suorituskyky ylittää a-Si TFT:t ja painetut OTFT:t. Liuosprosessiin perustuvien metallioksidien korkeaa valmistuslämpötilaa voidaan laskea käyttäen **Julkaisussa [II]** ja **Julkaisussa [III]** esiteltyä menetelmää, joka perustuu matalan aallonpituuden ultravioletti-säteilyn ja lämmityksen yhteisvaikutukseen. Tätä menetelmää käyttämällä osoitetaan, että mustesuihkutulostettuja In_2O_3 puolijohteita voidaan valmistaa matalassa lämpötilassa taipuisille ja edullisille muovialustoille. **Julkaisussa [IV]** osoitetaan, että sulkutyyppisillä TFT:illä kuormattuja, korkean vahvistuksen omaavia yksipolaarisia inverttereitä voidaan valmistaa mustesuihkutulostusta ja In_2O_3 puolijohteen sähköisten ominaisuuksien paksuusriippuvuutta hyödyntämällä.

Yhteenvetona voidaan todeta, että metallioksidipuolijohteita on mahdollista valmistaa taipuisille alustoille matalaa lämpökäsittelylämpötilaa ja teollisen mittakaavan painomenetelmiä käyttäen. Tulevaisuudessa painettuja metallioksidiohutkalvotransistoreita voidaan mahdollisesti käyttää sovelluksissa, kuten esimerkiksi bio- ja suuren pinta-alan antureissa, taipuisissa näytöissä ja integroiduissa sekä analogisissa piireissä, joiden ominaisuuksia on analysoitu tässä väitöskirjassa.

Avainsanat painettu elektroniikka, metallioksidi-ohutkalvotranistorit, fleksopaino, mustesuihkutulostus, matala toivutuslämpötila, sulkutyyppiseen transitorikuormaan perustuva invertteri

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Preface

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First of all, I would like to thank my supervisor Dr. Ari Alastalo for sharing the fascination in printed metal oxides – I'm truly grateful that your door was always open for discussion and guidance, Prof. Esko Kauppinen for having me as a part-time PhD student and showing your interest in this topic, and Dr. Himadri Majumdar for your enthusiasm, guidance, and support. I would also like to thank all my other co-authors at VTT, Mr. Kim Eiroma, Mr. Kimmo Ojanperä, Dr. Terho Kololuoma, and Mr. Olli-Heikki Huttunen, who all lent their expertise to make this possible. I'm thankful to Mrs. Pirjo Hakkarainen, Mrs. Jaana Marles, and Mrs. Ulla Sarajärvi for the technical assistance, team leader Dr. Maria Smolander for her support, and to other current and former colleagues at VTT, especially Dr. Tomi Mattila, Dr. Mark Allen, Dr. Mikko Aronniemi, Dr. Juuso Olkkonen, Dr. Marja Vilkman, Dr. Tapio Mäkelä, Dr. Henrik Sandberg, Mr. Mika Suhonen, and Mr. Liam Gillian. I appreciate all the helpful discussions with our collaborators, especially Dr. Kal Banger (UCAM), Dr. Pedro Barquinha (FCT-UNL), Dr. Kazuhiro Murata, and Dr. Nobuko Fukuda (AIST). I'd like to express my gratitude towards my pre-examiners, Prof. Heli Jantunen and Prof. Gerwin Gelinck, for their useful comments, and Prof. Thomas Anthopoulos for serving as the honored opponent.

My studies wouldn't have taken me this far without the possibility to acquire years of hands-on experience at the cleanroom throughout my M.Sc. studies at University of Jyväskylä. I'm thankful to all my colleagues from those times and, most of all, to my fellow students from all the way from the freshman year in physics: Dr. Janne-Petteri Niemelä, Dr. Olli Herranen, and Dr. Mikko Leskinen.

Thank you, Petteri, Aapo, Juho, and Antti for your lasting friendship, and my in-laws, Masa, Sirpa, and Kaisa, for your love and invaluable help. I'm grateful to my parents, Heikki and Sirkka, and my sister Henriikka for always supporting and believing in me. Most of all, without the years of patience, understanding, and love from Hanna, I would not be writing this. And Onni – you're the sunshine of my life.

-Jaakko Leppäniemi, 4th of May 2017

Contents

List of Publications

This thesis is based on the following original publications, which are referred to in the text as [I]–[IV].

I J. Leppäniemi, O.-H. Huttunen, H. Majumdar and A. Alastalo, “Flexography-printed thin In_2O_3 semiconductor layers for high-mobility thin-film transistors on flexible plastic substrate,” *Advanced Materials* **2015**, vol. 27 (44), pp. 7168-7175

II J. Leppäniemi, K. Ojanperä, T. Kololuoma, O.-H. Huttunen, J. Dahl, M. Tuominen, P. Laukkanen, H. Majumdar and A. Alastalo, ”Rapid low-temperature processing of metal-oxide thin film transistors with combined far ultraviolet and thermal annealing,” *Applied Physics Letters* **2014**, vol. 105 (11), p. 113514

III J. Leppäniemi, K. Eiroma, H. Majumdar and A. Alastalo, “Far-UV Annealed Inkjet-Printed In_2O_3 Semiconductor Layers for Thin-Film Transistors on a Flexible Polyethylene Naphthalate Substrate,” *ACS Applied Materials and Interfaces* **2017**, vol. 9 (10), pp. 8774-8782

IV J. Leppäniemi, K. Eiroma, H. Majumdar and A. Alastalo, “In_2O_3 Thin-Film Transistors via Inkjet Printing for Depletion-Load NMOS Inverters,” *IEEE Electron Device Letters* **2016**, vol. 37 (4), pp. 445-448

Author's Contributions

I The research plan was designed by the author together with the co-authors. O.-H. Huttunen and the author coordinated the sample preparation with the author also contributing to the fabrication work. The author performed all measurements, except the TEM and TGA/DTA/MS measurements that were subcontracted from Nanolab Technologies, Milpitas, CA, USA and University of Oulu, Oulu, Finland, respectively. Dr. M. Vilkman and Dr. T. Kololuoma helped with the FTIR measurements and Dr. H. Jussila with the GIXRD measurements. The author did all analysis and wrote the first version of the manuscript, which was finalized together with the co-authors. (Author contribution 60 %)

II The research plan was designed by the author together with H. Majumdar, K. Ojanperä and A. Alastalo. The inks were developed by T. Kololuoma and O.-H. Huttunen. The author, K. Ojanperä and H. Majumdar fabricated the TFT samples. J. Dahl, M. Tuominen and Dr. P. Laukkanen performed the XPS measurements. The XRD measurements were subcontracted from Dr. P. Kostamo of SiruTech Oy, Espoo, Finland. The author performed electrical characterization and, together with H. Majumdar, analyzed the XPS and XRD measurements. The author wrote the first version of the manuscript, which was finalized together with K. Ojanperä, H. Majumdar and A. Alastalo. (Author contribution 40%)

III The research plan was designed by the author together with H. Majumdar and A. Alastalo. The inkjet-printing process was developed and the samples fabricated by the author and K. Eiroma. The author planned, performed the experiments, analyzed the data and wrote the first version of the manuscript, which was finalized together with the co-authors. (Author contribution 80%)

IV The author was responsible for the depletion-load inverter idea and for the research plan. The samples were prepared by the author and K. Eiroma. The author performed all measurements, analysis and wrote the first version of the manuscript, which was finalized together with the co-authors. (Author contribution 80%)

List of Other Publications

The author has contributed to the following related publications that are cited in the text as [1]–[4].

[1] H. Majumdar, J. Leppäniemi, K. Ojanperä, O.-H. Huttunen, and A. Alastalo, “Effect of UV light and low temperature on solution-processed, high-performance metal-oxide semiconductors and TFTs,” *Proc. 5th Electron. Syst. Technol. Conf.*, pp. 14–16, 2014.

[2] A. Alastalo, J. Leppäniemi, K. Ojanpera, and H. Majumdar, “Modelling of printable metal-oxide TFTs for circuit simulation,” *Proc. 5th Electron. Syst. Technol. Conf.*, pp. 1–5, 2014.

[3] T. Kololuoma, J. Leppäniemi, and A. Alastalo, “Gravure-printed sol-gel derived hybrid aluminum oxide dielectric films fabricated for TFT applications,” in *Proceedings of LOPE-C*, 2012, pp. 88–92.

[4] T. Kololuoma, J. Leppäniemi, H. Majumdar, R. Branquinho, E. Herbei-Valcu, V. Musat, R. Martins, E. Fortunato, and A. Alastalo, “Gravure printed sol–gel derived AlOOH hybrid nanocomposite thin films for printed electronics,” *J. Mater. Chem. C*, vol. 3, no. 8, pp. 1776–1786, 2015.

Other publications including contributions from the author, which are more broadly related to the field of the thesis, namely on printed nanoparticle memories [5]–[10], and on electrical and chemical sintering of printed metal nanoparticle conductors [11]–[14], are cited in the text accordingly.

List of Abbreviations and Symbols

2-ME	2-methoxyethanol
a-Si:H	Hydrogenated amorphous silicon
a-IGZO	Amorphous indium gallium zinc oxide
ACE	Acetone
AFM	Atomic force microscope
ALD	Atomic layer deposition
Al_2O_3	Aluminum oxide
ATR	Attenuated total reflection
BE	Binding energy
CB	Conduction band
CMOS	Complementary logic
CNT	Carbon nanotube
D	Drain terminal
D_2	Molecular deuterium
DIW	De-ionized water
DoD	Drop-on-demand
dpi	Dots-per-inch
DTA	Differential thermal analysis
EHD	Electrohydrodynamic
EG	Ethylene glycol
FTIR	Fourier-transform infrared
FUV	Far ultraviolet
FUV+T	Combined far ultraviolet exposure and thermal annealing

G	Gate terminal
GIXRD	Grazing incidence x-ray diffraction
H^*	Elemental hydrogen (radical)
IAD	Ion-assisted deposition
IC	Integrated circuits
IBZO	Indium barium zinc oxide
IGO	Indium gallium oxide
IGZO	Indium gallium zinc oxide
In_2O_3	Indium oxide
IPA	Isopropanol
IZO	Indium zinc oxide
IZTO	Indium zinc tin oxide
L/S	Line-space
LCD	Liquid crystal display
LTPS	Low-temperature polysilicon
Low-T	Low-temperature
MIS	Metal-insulator-semiconductor
MO	Metal oxide
MOSFET	Metal-oxide-semiconductor field-effect-transistor
MS	Mass spectrometry
nMOS	n-type metal oxide semiconductor logic
NP(s)	Nanoparticle(s)
OLED	Organic light emitting diode
OH^*	Hydroxyl radical
OTFT	Organic thin-film transistor
PCB	Printed circuit board
PDMS	Polydimethylsiloxane
PEDOT:PSS	Poly(3,4-ethylenedioxythiophene) polystyrene sulfonate
PEI	Polyethylene imine
PET	Polyethylene terephthalate

PEN	Polyethylene naphthalate
PI	Polyimide
PLD	Pulsed laser deposition
PV	Photovoltaics
PVP	Polyvinylpyrrolidone
R2R	Roll-to-roll
RF	Radio-frequency
RFID	Radio-frequency identification
RH	Relative humidity
RT	Room temperature (here 25 °C used)
rpm	revolutions per minute
S	Source terminal
S/D	Source-drain electrodes
SEM	Scanning electron microscope
SnO_2	Tin oxide
TGA	Thermogravimetric analysis
TEM	Transmission electron microscope
TFT	Thin-film transistor
UV	Ultraviolet
VB	Valence band
VTC	Voltage transfer characteristics
wt%	Percentage by mass
XPS	X-ray photoelectron spectroscopy
ZnO	Zinc oxide
ZTO	Zinc tin oxide

c	Concentration
C	Capacitance
C_{chan}	Channel capacitance
C_i	Areal capacitance of insulator

C_{gd}	Gate-drain overlap capacitance
C_{gs}	Gate-source overlap capacitance
d_x	Thickness of material x
d_{avg}	Average crystallite size
E	Electric field or energy
f	Frequency
f_T	Unity-gain frequency
$gain$	Current gain (ratio of output current to input current)
$\hbar$	Reduced Planck's constant
i	Imaginary unit ($i^2 = -1$)
I_d	Drain current
I_g	Gate leakage current
I_{gs}	Gate-source current (in quasi-static model)
I_{in}	Input current
I_{out}	Output current
J	Current density
L	Channel length
L_{gd}	Gate-drain overlap length
L_{gs}	Gate-source overlap length
m^*	Effective mass
m_e	Free electron mass
$n_\#$	Sample number
n_e	Charge carrier concentration
n_x	Refractive index of material x
q	Elementary charge
R_a	Average roughness
R_{bulk}	Bulk/surface back-channel resistance
R_{chan}	Channel resistance
R_d	Drain contact resistance
R_s	Source contact resistance

SS	Subthreshold swing
ΔP	Laplace pressure
p_{anilox}	Anilox pressure
P_{eq}	Vapour pressure in thermal equilibrium
p_{nip}	Nip pressure
T_{ann}	Annealing temperature
t_{ann}	Annealing time
T_{bp}	Boiling point
T_{max}	Maximum thermal tolerance
T_{vis}	Optical transparency in the visible region ($390 - 700$ nm)
v_d	Drift velocity
V_d	Drain voltage
V_{dd}	Operation voltage
V_g	Gate voltage
V_{hyst}	Voltage hysteresis
V_{in}	Input voltage
V_o^{n+}	Oxygen vacancy (at *n*th ionization state)
V_{on}	Turn-on voltage
V_{out}	Output voltage
V_T	Threshold-voltage
W	Width
w_{EG}	Ethylene glycol co-solvent ratio
Z	Impedance
β	Roughness parameter for mobility
γ	Surface tension
η	Viscosity
θ	Bragg angle
θ_c	Static contact angle
μ_{avg}	Average mobility

μ_d	Drift mobility
μ_{eff}	Effective mobility
μ_{FE}	Field-effect mobility
μ_{inc}	Incremental mobility
μ_{sat}	Saturation mobility
ρ	Density or resistivity
σ	Conductivity
$\langle\tau\rangle$	Mean free time
ω	Incident angle
ω_f	Angular frequency

1. Introduction

The ways of spreading of information have changed radically after at least two major technological discoveries, namely, the invention of the letterpress printing between the 11th and 15th centuries and the birth of the transistor at the 20th century. Printing was used to store and spread information for thousands of years before the letterpress printing, but it was only after this innovation, that printing became capable of producing copies of books at high-throughput and low-cost when compared to manual copying. The discovery of the transistor led to silicon-based semiconductor technology and integrated circuits (IC) that allowed efficient electronic data storage with an unceasing increase in the data storage density, and, eventually, in the globalization of information. Nowadays, silicon (Si) can be processed with photolithography at such a high resolution that the cost of single bit is well below 10^{-9} €-cent [15].

The merging of the two aforementioned technologies, commonly referred as printed or flexible electronics, has been actively pursued for various applications in recent decades [16]. When compared to the conventional, vacuum-based batch processes of electronics manufacturing, the key benefits of high-throughput printing include: (i) large area coverage; (ii) low cost per unit that is particularly attainable with continuous, roll-to-roll (R2R) fabrication; (iii) the possibility to use low-cost flexible substrates; and (iv) additive manufacturing processes for low material consumption and chemical waste. Although printed electronic devices cannot compete directly with the conventional Si-based electronics, either in price per bit or computational power [15], the benefits of printing can be anticipated in several applications. Printed thin-film solar cells and lighting panels based on organic light emitting diodes (OLED) benefit from the readily attainable large area coverage [17], OLED display manufacturing from the low material consumption of inkjet-printing [18], radio-frequency-identification (RFID) tags and embedded sensors from the low-cost-per-unit aspect of the R2R production [19], [20], and novel flexible systems such as flexible audio modules [21], flexible displays [22], [23], and artificial tactile skin from the possibility to use a wide range of flexible substrates [24].

However, the benefits in manufacturing are not a guarantee of success and in many cases the conventional, well-established processes have advanced to meet and outperform their upcoming rivals. In this respect, a host of electronic devices on flexible Si have already been demonstrated [25]. The hybrid approach, where

Si-based chips are assembled on flexible substrates, may well be the winner for flexible electronics [15]. Printing will likely find its place among the electronics manufacturing processes. But most certainly, printing will keep pushing the conventional processing technologies to advance even further to meet the competition.

1.1 A Brief History of Thin-Film Transistors

The concept of a thin-film-transistor (TFT) was invented separately by both J. Lilienfeld and O. Heil in the 1930s [26], [27]. TFTs were investigated intensively by several laboratories during the 1960s and during that time, the first working TFTs and ICs were reported by Weimer *et al*. [28], [29]. The first attempts to print active electronic components also date back to the 1960s, when researchers at companies such as RCA and Texas Instruments experimented with silk-screen printing of CdS and CdS:CdSe transistors [30], [31]. By that time, screen printing was used for printing thick-film passive components, such as capacitors and printed circuit board (PCB) wirings. The cost-effectiveness of printing was seen, as early as that, as the driving force for printing of active components, as Sihvonen *et al*. from Texas Instruments state in their paper [31]:

"The envisioned payoff for such a successful coalescence of printing disciplines with semiconductor concepts would be high volume production of components and networks attractively competitive costwise with components and networks manufactured by other means." [1]

After these initial attempts, the printing of active electronic components was not pursued in research for a long time. Meanwhile, TFTs were suppressed by metal-oxide-semiconductor field-effect-transistors (MOSFET) that were based on familiar semiconductors such as Si and Ge [32]. The time for TFTs would come later with the birth of active-matrix backplanes for liquid crystal displays (LCD) [33]. The adaptation of TFTs in products was accelerated by the discovery of hydrogenated amorphous Si (a-Si:H) TFTs, which had properties that met the demands of active-matrix applications and allowed reproducibility that made the mass production of TFTs possible [34].

The second advent of printed electronics got its birth during the late 1970s with the discovery of chemical doping-induced conductivity in conjugated polymers by Shirakawa *et al*. [35] which led to the development of conductive polymers — the workhorse of printed electronics [36], [37]. After the pioneering work performed by R. Friend *et al*. at the Cavendish Laboratory on solution-processing of organic materials during the 1990s [38], the new processing scheme led to fully screen-printed organic TFTs (OTFTs) on plastic substrates [39], and to inkjet-printed *p*-type semiconductor devices, such as OTFTs and OLEDs [40]–[42]. When solution-processed pentacene-based OTFTs demonstrated inverter gains > 1 and,

[1] Reproduced by permission of The Electrochemical Society.

therefore, could be utilized in circuits, OTFT-based circuits emerged as an alternative to conventional Si-based circuits in low-cost, low-performance applications [43].

The charge carrier mobility (μ) is a parameter that describes the current output capacity of the semiconductor material. μ of organic semiconductors was long limited to well below 1 cm^2/(Vs), and was thus inferior to the μ of the state of the art a-Si:H TFTs ($0.5 - 1$ cm^2/(Vs)) which were used in flat-panel LCD display applications [44], [45]. The driving force behind the research on novel TFT technologies beyond a-Si:H has been to find a technology that is capable of driving OLED pixel current in next-generation high-resolution displays[2] with a fabrication process that is compatible with current a-Si:H processes (~ 250 °C for a-Si:H) used in flat-panel LCD display manufacturing. Low-temperature (low-T) polycrystalline silicon (LTPS) TFTs can deliver enough current with $\mu > 50$ cm^2/(Vs), however, the high processing temperature of > 500 °C, device non-uniformity, manufacturing complexity, and manufacturing cost beyond that of a-Si:H have limited the use of LTPS in OLED displays.[44], [46]

The research on metal oxide (MO) TFTs took off in 2003 with the development of transparent semiconducting *n*-type MO from sputtered ZnO by Hoffman *et al*. [47], Masuda *et al*. [48], and Carcia *et al*. [49], which collectively showed that ZnO TFTs could enable $\mu > 1$ cm^2/(Vs) and good switching properties while retaining reasonable optical transparency that could be of benefit in active-matrix display applications. Hosono *et al*. reported the fabrication of transparent TFT devices from a novel quaternary MO, crystalline InGaZnO (IGZO), with a record-high mobility of ~ 80 cm^2/(Vs) [50]. Many of the early examples of MO TFTs utilized high post-deposition annealing temperatures $T_{ann} > 500$ °C to enhance the crystallinity and the charge carrier properties of the MO films. The fabrication of amorphous IGZO (a-IGZO) TFTs by pulsed laser deposition (PLD) by Hosono *et al*. [51], and the nanocrystalline ZnO TFTs by RF magnetron sputtering by Carcia *et al*. [49] and Fortunato *et al*. [52] further indicated that MO TFTs could be fabricated at room temperature (RT) on low-cost flexible plastic substrates.

During the course of the previous 10 years, MO TFTs have been shown to exhibit suitable properties for the OLED display application as they deliver high-enough mobility for the task with $\mu > 10$ cm^2/(Vs). a-IGZO became the semiconductor material of choice over ZnO due to (i) large-area device uniformity enabled by the amorphous state, (ii) the possibility of low-T processing, (iii) the operational stability beyond that of a-Si:H, (iv) the processing compatibility with current flat-panel LCD display manufacturing processes, and (v) the low charge carrier concentration that allowed the fabrication of TFTs with low off-state current ($\sim 10^{-13}$ A) [53]. The research work on MO TFTs has focused on finding the optimal multi-component MO composition, optimizing the TFT device stack, and the fabrication processing conditions which allow a high operational stability that is manifested as

[2] This would require μ in excess of ~ 1.5 cm^2/(Vs) for a pixel technology without compensation circuitry and $\sim 5 - 10$ cm^2/(Vs) for an architecture with compensation circuitry that is required for countering any threshold-voltage shift during continuous operation.[45]

a low threshold voltage (V_T) shift during a current bias stress under illumination, that is relevant for display applications [46], [53].

Solution-processing is considered as a low-capital cost alternative for the conventional vacuum-processing of TFTs. The pioneering work on solution-processed MO TFTs was performed at the Oregon State University and Hewlett Packard labs. The first report on high-performance, solution-processed ZnO TFTs by Wager *et al*. utilized a high $T_{ann} > 600$ °C for the precursor-to-metal oxide conversion and to enhance the charge carrier concentration (n_e) of the devices [54]. Ever since, the research focus of solution-processed MO TFTs has been on developing high-performance MO TFTs that are processed at low-T on low-cost plastic substrates, mostly targeting the next generation of flexible displays [46], [55]–[57].

The display application-driven approach has brought the vacuum-processed MO TFTs from lab-to-market for high-resolution flat-panel displays in record-breaking time. IGZO backplanes have been used in commercial products such as smartphones, tablets and ultra-high resolution displays by Sharp [58]. The next-generation of flexible display prototypes employing MO TFTs have been demonstrated by several display manufacturers since 2009 [46], [53]. As a recent stand-out research result, a flexible active-matrix OLED display has been demonstrated on low-cost polyethylene naphthalate (PEN) substrate driven by sputtered a-IGZO — a result where all processing was done at a maximum temperature of 150 °C [59]. On the other hand, pursuing this single goal without considering the possibilities and the requirements set by other applications has resulted in the application space of MO TFTs only very recently being expanded towards novel applications such as TFT-based flexible biosensors [60], [61], flexible flat-panel X-ray detectors [62], [63], light sensors [64], [65], complementary logic (CMOS) circuits when combined with *p*-type OTFTs [66], or carbon nanotube (CNT) TFTs [67], radio-frequency (RF) applications, such as rectifiers and low-power RFID tags [68], [69], as well as MO-based Schottky diodes for ultra-high frequency (UHF) energy harvesters and gigahertz communications [70], [71].

1.2 Motivation

The ultimate cost-efficiency for printed electronics applications can be achieved via direct high-throughput printing of all components of the electronic systems on a single substrate without the assembling steps of the individual components. Therefore, the enabling goal for printed electronics is developing a process for all-printed, high-performance TFTs on low-cost plastic substrates.

The remaining key challenges in the fabrication of high-performance, all-printed MO TFTs and circuits on flexible plastic substrates are summarized in Figure 1. Clearly, all layers of the TFT device stack have their unique demands, which require focused research efforts to overcome them. In this thesis, the focus is on the processability of the semiconductor layer. For obtaining impurity-free MO films, the required T_{ann} and its duration (t_{ann}) are currently incompatible with the thermal tolerance of low-cost plastic substrates (< 150 °C), the slowest, reasonable R2R-

line speeds (e.g. > 1 m/s), and oven lengths (< 5 m), respectively. So far, the work with printed MO layers has been performed on rigid substrates, thus giving no information on the processability and performance of the materials on real flexible substrates. In addition, the performance of all oxide-based circuits is poor due to the low μ of *p*-type oxide semiconductors for CMOS-type approach [46].

1.3 Objectives and Scope of the Thesis

As stated above, organic materials have been utilized in printed electronics research for a long time and they have reached a level of maturity where they can be processed with high-throughput R2R-methods [17]. This thesis aims to demonstrate that (i) inorganic MO materials can be printed using mass-production-capable printing technologies, and (ii) the resulting printed films can be processed at low-T as semiconductor layers for TFT devices, whose electrical performance is beyond their current, printed organic or vacuum-processed a-$\mathrm{Si{:}H}$ counterparts.

The work in this thesis focused on the key challenges regarding the printed semiconductor layer. In **Publication [I]**, we show that thin $\mathrm{In_2O_3}$ semiconductor layers can be used as enhancement-mode TFTs when the devices are treated with a low-temperature post-contact annealing. In addition, we show, for the first time, that thin $\mathrm{In_2O_3}$ layers can be processed with well-established printing methods, such as flexographic (**Publication [I]**) and inkjet printing (**Publication [III]**), for realizing high-performance TFTs on flexible substrates. Moreover, in **Publication [II]** and **Publication [III]** we demonstrate that the required T_{ann}, or alternatively t_{ann}, for the precursor-to-metal oxide conversion can be lowered with the help of concurrent low-wavelength far ultraviolet (FUV) exposure. Finally, as an alternative to all-oxide CMOS technology, we show in **Publication [IV]** that the thickness-dependent characteristics of $\mathrm{In_2O_3}$ semiconductors can exploited via inkjet-printing to realize unipolar nMOS-type depletion-load inverters with high inverter gain.

The thesis is arranged as follows. In Chapter 2, the materials, inks and printing methods typically used in printed electronics are reviewed. Chapter 3 presents the background for MO semiconductors and the relevant TFT models. The state of the art in low-temperature annealing methods for the solution-processed MO TFTs and printed MO TFTs are reviewed in Chapter 4. Chapter 5 presents the materials and the experimental methods used in this work. The key results of **Publications [I]–[IV]** are presented in Chapter 6. The results are compared to the scientific literature, the applications of printed MO TFTs are analyzed, as well as the suggestions for future work are discussed in Chapter 7. Finally, the conclusions are made in Chapter 8.

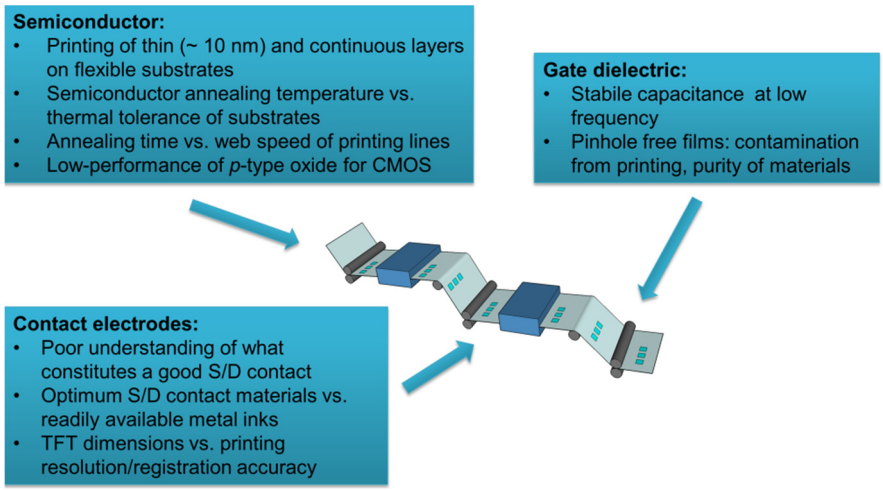

Figure 1. The main challenges in R2R-printed MO TFTs on flexible substrates.

2. Printing of Electronic Components

In this chapter, an overview of the materials for printed electronics is followed by an introduction to the characteristics of the printing inks and their behavior on substrates. The last part contains a description of the different coating and printing techniques used in the fabrication of electronic devices.

2.1 Materials for Printed Electronics

The minimum requirement for the printability of organic and inorganic electronic materials is a liquid vehicle: the materials need to be either liquids, soluble or dispersed in organic solvents or water. Organic materials that can be dispersed in organic solvents or H_2O provide solution-processed films with properties ranging from insulating polymers and semiconducting small molecules, to conjugated polymers that can be semiconducting or conducting. The main advantages of organic materials in printed devices are the low-T processing that gives compatibility with low-cost plastic substrates, and the inherent flexibility of the organic materials [44].

Polymers are often regarded as insulating materials. Insulating polymers, such as polyvinyl pyrrolidone (PVP) and poly(methyl methacrylate) (PMMA), which are widely used in the chemical and electronics industry can be printed as dielectric layers in electronic devices. In a simplified picture, the remarkable conducting or semiconducting properties of conjugated polymers arise from the alternating single and double bonds of the C backbone, which leaves one non-bonding *p*-electron to form a valence band from the delocalized π-orbitals. The backbone polymer is then chemically doped with polymers having electron accepting groups that create holes in the valence band and, thus, lead to *p*-type conductivity [36]. The most common conductive polymer is polystyrene sulfonate-doped poly(3,4-ethylenedioxy-thiophene), also known as PEDOT:PSS, which can be dispersed in H_2O and printed using various printing methods for obtaining transparent, conducting structures, where the conductivity (σ) of ~ 500 S/m can be reached [72]. Semiconducting thiophene-based conjugated polymers, such as poly-3-hexyl thiophene (P3HT), can be dispersed in organic solvents due to their alkyl side-chains (C_nH_{2n+1}) and used as printed semiconductors for OTFTs [44]. Much of the improvements obtained on the μ of the thiophene-based *p*-type semiconductors

have been grounded on the arrangement of the polycrystalline polymer chains, such that the solubility-improving side-chains interfere as less as possible with the current-carrying π-orbitals, resulting in $\mu \sim 1$ cm^2/Vs in solution-processed OTFT devices [44], [45]. In addition to polymers, semiconducting small organic molecules, such as pentacene and other acene-based molecules can also be dispersed in organic solvents with the help of suitable side chains. Tri-isopropylsilylethynyl (TIPS) side-groups in pentacene allow the material to be solution-processed with $\mu \sim 1$ cm^2/Vs [44], [45]. Again, the crystallinity and the structural arrangement of the molecules greatly affect the μ of the OTFT devices based on small molecules. The highest μ reported in OTFTs are $\mu > 10$ cm^2/Vs for small molecules that are crystallized *in situ* with the help of inkjet-printing [73]. The solution-processed organic semiconductors are mostly *p*-type, although progress has been made in developing materials for solution-processed *n*-type OTFTs, with electron mobility up to 0.8 cm^2/Vs [74].

CNTs are another promising organic material for flexible electronics, which can be printed or transferred as CNT networks to plastic substrates for transparent conductors and *p*-type semiconductors for high-performance TFTs [19], [75]–[78]. Although CNTs are intrinsically ambipolar, when exposed to air they are readily doped by oxygen molecules adsorbed on the CNT to be only *p*-type. However, they can be doped to be only *n*-type with the help of electron donating polymers, such as polyethylene imine (PEI), that replace the adsorbed oxygen [79]. Recently air-stable *n*-type doping of printed CNT TFTs has been demonstrated with SU-8 epoxy-resist acting both as the encapsulation and the dopant [78].

Inorganic materials such as metal nanoparticles (NP) and MO sol-gel precursors can provide superior electrical performance to their organic counterparts in terms of σ, μ, and the relative permittivity (ε_r) for conductors, *n*-type semiconductors and insulators, respectively [72]. Despite their enhanced electronic properties when compared to organic materials, inorganic materials typically require a high-temperature processing step that limits their usability on low-cost plastics. In addition, they are often argued to be of limited flexibility. This mantra is challenged by the recent developments in stretchable MOs fabricated on thin (~1 μm) plastic substrates [80].

Metal NPs, such as Ag, Au, Cu, and Sn can be synthesized in sizes ranging between $1-100$ nm and used as printed conductor structures. Stabile NP ink dispersions are obtained by dispersing the NPs in organic solvents or in $\mathrm{H_2O}$ either electrostatically in an electrolyte solution, or by encapsulating the NPs sterically (bulky molecules) or electrosterically (molecules with ionic side groups) with capping agents, such as polymers, thiols and amines [81]–[83]. After the printing and drying steps, the inks typically require a heating step at $T > 150$ °C to remove the encapsulation, and to allow the coalescence of the metal NPs to form an interconnected network by particle necking and grain growth (sintering) that enables a high σ. Novel sintering methods, such as photonic, electrical, laser, IR, microwave, plasma and chemical sintering, have been developed for the rapid sintering of metallic NPs at low-T on low-cost plastic substrates [12]–[14], [81]. After sintering, the Ag NP-based conductors have a clearly higher σ than for example PE-

DOT:PSS, with σ up to $\sim 3 \cdot 10^6$ S/m ($\sim$50 % of bulk Ag) [14]. µm-sized metal flakes can be dispersed in solvents with a lower encapsulation content that already allows a high σ after drying, however, this results in thick layers with high roughness [72].

The majority of inorganic MO semiconductors, such as ZnO, In_2O_3, IGZO, and their derivatives, are *n*-type. Although some *p*-type semiconductor materials, such as Cu_xO and SnO_x, exist, they exhibit a lower performance than the *n*-type MO semiconductors [46]. NPs can be also synthesized from MOs: ITO for transparent conductors, In_2O_3, ZnO and IGZO for *n*-type semiconductors, and Al_2O_3 and SiO_2 for dielectric, to name a few. However, the isolated MO NPs have poor electrical properties and they require sintering at an even higher temperature ($T > 500$ °C) than metallic NPs to a create a continuous, but porous network structure [56]. Therefore, in the recent years, most of the work on solution-processed MO materials has focused on sol-gel precursors that provide a low-T route (< 300 °C) for homogenous and uniform MO films that can be either amorphous, nano- or polycrystalline. Precursors from metal alkoxides and metal salts, such as halides, nitrates and acetates, have been utilized to create conductors, semiconductors and dielectric MO layers [81], [84]–[88]. For multicomponent MO semiconductors, such as ZnSnO (ZTO) and IGZO, the precursor route allows a facile method for already mixing the precursors in the liquid phase [85], [89]. A great amount of progress has been made in further lowering the T_{ann} of the precursors to be compatible with low-cost plastic substrates [56], [57]. For example, novel ultraviolet (UV) light-assisted annealing methods have allowed the fabrication of high-performance IGZO TFTs at $\sim$150 °C [90].

Table 1 summarizes some of the characteristics of the printable TFT technologies discussed in this section [45], [46], [75].

Table 1. Characteristics of the printable TFT materials and the current a-Si:H technology as a reference.

Parameter	a-Si:H	OTFTs	CNT TFTs	MO TFTs
Semiconductor type	*n*-type	*p*-type	*p*-type	*n*-type
Mobility (cm^2/(Vs))	< 1	$\sim 0.1 - 10$	$\sim 1 - 100$	$\sim 1 - 100$
Process temperature (°C)	~ 250	RT – 150	RT – 150	> 150

2.2 Inks, Substrates and Their Interactions

Some of the most important parameters of printing inks are determined by the solvent-base of the ink whose viscosity (η), surface tension (γ), equilibrium vapour pressure (P_{eq}), and boiling point (T_{bp}) affect the printability of ink and its behavior on the printing substrate.

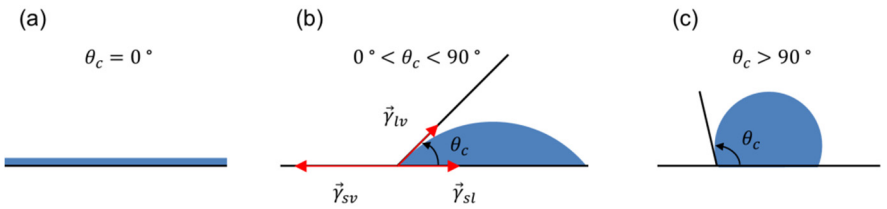

Figure 2. Schematic images of wetting regimes: (a) full wetting, (b) partial wetting, and (c) non-wetting. The surface tension forces acting on the triple-point are shown in (b) for Young's relation.

In printing, the general rule of thumb is that ink of low γ will wet substrate of high γ (surface energy). Liquid materials will tend to minimize their surface area due to γ. However, on a solid surface, liquid droplets will interact with the surface and wet it such that the total free surface energy is minimized, as shown in Figure 2. The static contact angle between the droplet and the substrate (θ_c) is given by Young-Laplace relation

$$\gamma_{sv} - \gamma_{sl} = \gamma_{lv} \cos\theta_c = \frac{\Delta P}{(R_1^{-1} + R_2^{-1})}, \tag{1}$$

where γ_{sv}, γ_{sl} and γ_{lv} are the surface energies of the solid-air, solid-liquid and liquid-air interfaces, respectively, and are obtained from the respective capillary forces acting on the triple-point or the contact line of the droplet, as shown in Figure 2 (b). Further, ΔP is the Laplace pressure, i.e. the pressure difference between the interior and outside the droplet, R_1 and R_2 are the orthogonal radii of curvature for the droplet. In a more complex representation, the γ can be further broken down into their non-polar (dispersive) and polar components $\gamma = \gamma^D + \gamma^P$, arising from dispersive van der Waals forces (London dispersion) and various polar dipole interactions and hydrogen bonding, respectively [91].

Plastics have a generally low γ arising from their lower chemical binding energy whereas solid inorganic surfaces, such as SiO_2 and Al_2O_3, have a high γ due to their covalent nature. Wetting of the printing inks can be improved by increasing the γ of the substrate, for example by a corona or O_2 plasma treatment. In O_2 plasma treatment, the surface is subjected to bombardment with energetic oxygen ions and oxygen radicals generated from the O_2 in the plasma chamber. These clean the surface by decomposition of adsorbed organic molecules, induce cross-linking in polymers, and temporarily increase the γ of the receiving surface by introducing polar OH^- groups [91], [92]. The polar groups at the substrate surface will especially enhance the affinity of polar inks.

The γ of the inks can also be reduced by incorporating surfactants, which will adsorb onto all the interfaces (liquid-air, liquid-solid and solid-air) and work to decrease γ_{sl} and γ_{lv}, while increasing γ_{sv}. As a result, they promote a lower free

energy of the system [93].[3] However, surfactants adsorbed at the layer interfaces can be detrimental in TFT applications, where the channel is formed at the interface between the dielectric and the semiconductor. The remnant surfactants could cause deteriorating charge carrier properties by charge trapping.

The solutes of the ink, such as NPs, polymers and solvated molecules in sol-gel precursors, also affect the print quality. When structures are printed on the substrate surfaces, the solutes can redistribute inside the liquid structure during the drying phase. In low-viscosity inks such as ink-jet inks, where $\eta < 10$ mPa·s, the contact line of the printed area is fixed by solute adsorption and surface interactions [94]. As the droplet form is retained by the γ during the drying phase, the enhanced evaporation of the solvent at the droplet edges leads to a radial outward flow to compensate for the evaporated volume. This flow carries the solutes to the perimeter of the printed area, leading into uneven deposition of the solutes during the drying phase. As a result, so-called "coffee-ring" patterns are formed that have a higher layer thickness at the edges of the printed area.[94] The effect can be controlled by introducing a co-solvent with a high T_{bp} and a low γ that enhances the inward (Marangoni) flow due to a gradient in the γ that is induced by a concentration gradient [95].[4]

Solutions and dispersions have different printing properties in terms of inkjet printing. Solutions in general do not clog the nozzle, whereas dispersions can obstruct the ink flow if the solute size of the dispersion is too large, or if the solvent evaporates too quickly at the nozzle and increases the solid content locally.

When considering device fabrication on substrates using printing methods, the maximum thermal tolerance (T_{max}), the coefficient of thermal expansion (CTE), the surface roughness (R_a), and the optical transparency in the visible region (T_{vis}) of the substrates are the key parameters. T_{max} will limit the temperature that can be used for the drying and the annealing/sintering steps, which are required, especially for the inorganic materials. During thermal cycling, a high CTE can lead to films with large stress, to the formation of cracks, and to plastic deformations of the substrate, which will affect the overlay accuracy of multilayer structures [96]. If the R_a of the substrates is very large, such as with uncoated paper, the printing quality will be poor with non-continuous films. T_{vis} is important for some applications, such as optoelectronic components or transparent conductors. Besides the parameters above, the chemical compatibility between the ink and the substrate is one additional aspect to consider. Depending on the case, the chemical reaction between the ink and the substrate is either avoided, as in the degradation of the substrate by the solvent system of the ink, or preferred, as for example in the bond formation for improved adhesion [91] or in the removal of the encapsulation of NPs in chemical sintering [13].

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[3] Free energy of the system is $G = \gamma_{lv}A_{lv} + \Delta PV + \pi R^2(\gamma_{sl} - \gamma_{sv})$, where A_{lv} is the surface area of the liquid-vapor interface, ΔP the Laplace pressure of the droplet, V and R the volume and radius of the droplet, respectively [93].

[4] The evaporation rate is dependent on the T_{bp} (and P_{eq}) of the solvent. Therefore, the solvent with lower T_{bp} evaporates at the edge faster than the solvent with higher T_{bp}. This leads to a concentration gradient.

The substrate surfaces can be divided into open and closed surfaces, where an open surface, such as paper, readily absorbs the solvent of the ink, and on a closed surface, such as plastics, glass or SiO_2, the solvent absorption is limited. On closed surfaces the ink behavior is mostly determined by γ of the substrate, as well as the solvent evaporation and the solute redistribution phenomena, whereas on open surfaces, the ink spreading is less affected by these. In general, the pore size of an open substrate must be larger than the average size of the solutes to avoid absorbing the solutes inside the substrate [97].

Table 2 summarizes the most important parameters for some of the most common substrates used in printed electronics, as well as for some more specialized flexible substrates with good thermomechanical properties such as Xenomax polyimide (PI) and flexible glass. [72], [98] Si is shown as a reference.

Table 2. Characteristics of selected substrates used in printed electronics research. The data can vary significantly between different film types and brands.

Substrate	T_{max} (°C)	CTE (ppm/ °C)	R_a (nm)	T (%)
Paper (uncoated)	~ 260	$\sim 5-15$	> 1000	Opaque
Photo paper (coated)[5]	$\sim 100-120$	Large	$\sim 30-100$	Opaque
PET (Melinex)	~ 150	> 15	~ 1	> 85
PEN (Teonex)	~ 180	$\sim 10-30$	~ 1	~ 85
PI (Kapton)	> 350	$\sim 30-60$	> 100	Amber
PI (Xenomax)[6]	> 500	Same as Si	Low	Amber
Flex. glass (Corning)[7]	~ 700	~ 3	< 0.5	~ 90
Si (reference)	> 1000	~ 2.5	~ 0.1	Opaque

2.3 Printing Techniques

In conventional four-color cyan-magenta-yellow-key (CMYK) printing used in newspaper and magazine printing, the halftoned color images consist of isolated pixels made of CMYK subpixels. The optimized graphic inks contain printability improving additives such as binders to improve the adhesion of the ink and surfactants to improve the wetting. In contrast, printed electronic layers are desired to be

[5] The values are dependent on the surface coating of the paper. During heating at $T < 100$ °C, the photo papers exhibit severe curving due to escaping moisture or induced stress.

[6] http://www.toyobo-global.com/ir/data/annual/pdf/2013/p16-17.pdf (accessed on 11.12.2016). The R_a of the substrate is not publicly available.

[7] https://www.corning.com/media/worldwide/cdt/documents/Willow_2014_fact_sheet.pdf (accessed on 11.12.2016).

homogeneous, continuous, and of uniform thickness, as well as free from remnant additives that can have a detrimental effect on the electronic properties of the layers.

In this section, an overview is given of the coating and printing techniques utilized widely in printed electronics research. The coating techniques can be differentiated from the printing techniques as coating yields un-patterned layers, whereas printing produces a patterned surface. Only a qualitative description of each method is given as the actual configurations of the systems vary widely. Vacuum processes that can be performed in a continuous R2R-fashion are also presented.

Coating techniques

Spin-coating is the most common, low-cost coating method utilized in research and in the electronics industry, for example in the deposition of photoresist. In the process shown in Figure 3 (a), liquid is first dispensed on to the surface of a sample. By then accelerating the sample to a desired rotation speed, the centripetal force acting on the liquid can be controlled. At the beginning of the process, most of the liquid is flung off from the sample and the remaining film undergoes evaporative drying during the rest of the spinning. When the process is completed, a desired thickness (d) of the semi-dry film remains on the sample. The method produces a highly reproducible d of the film, where d is mostly dictated by the η and the solid content of the liquid, and is related to the revolutions-per-minute (rpm) of the spinner by $d \propto (rpm)^{-1/2}$ [99]. With the conventional spin-speeds of $1 - 10$ krpm, only a threefold variation of d can be obtained for a set liquid. Spin-coating is a batch process with a limited sample size and wastes most of the liquid material.

Several contact coating methods, such as bar, slot-die, doctor blade and gravure coating can be used to provide a full-coating of liquid films of desired d on samples. In doctor blading, an excess amount of ink is first deposited on to the substrate after which a sharp blade is passed over the sample at a defined height, which scrapes off the excess ink and defines the d of the liquid [99]. The rotary version, called knife-over-edge coating, is shown in Figure 3 (b). In bar coating, ink is first applied in excess onto the substrate surface and then a rod, called the Meyer bar, with a cylindrically coiled wire of defined diameter is rotated over the substrate. The opening between the wires provides an accurate control of the d of the ink layer. For example, bar coating has been used to create semiconductor and gate dielectric layers in OTFTs [100] and MO TFTs [101].

Different from the other coating methods, spray coating provides a non-contact large-area coating method where the ink is ejected from a small orifice in a nozzle by pressurized gas or by ultrasonic excitation. The plume of the formed aerosol is carried by the gas on to the substrate. In spray pyrolysis, the substrate is held at an elevated temperature which allows chemical reactions to occur directly in the coated film. The technique has been used to create various MO TFTs [102]–[105].

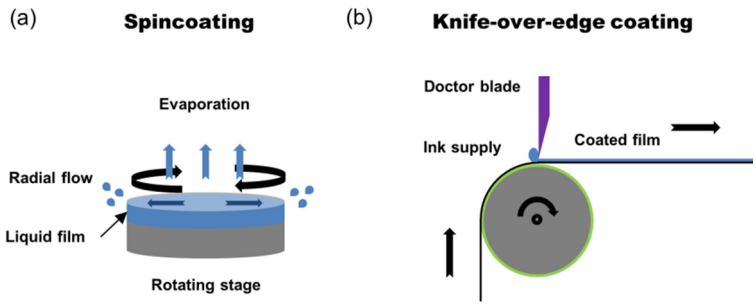

Figure 3. Schematic images of (a) spin-coating (batch process) and (b) knife-over-edge coating (continuous process).

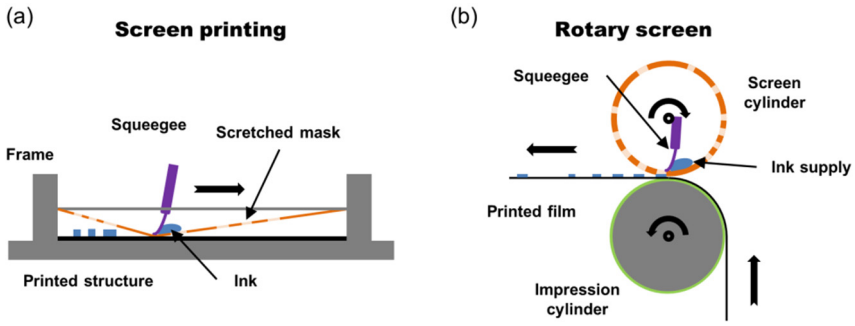

Figure 4. Schematic images of (a) non-contact screen printing (batch process) and (b) rotary screen printing (continuous process).

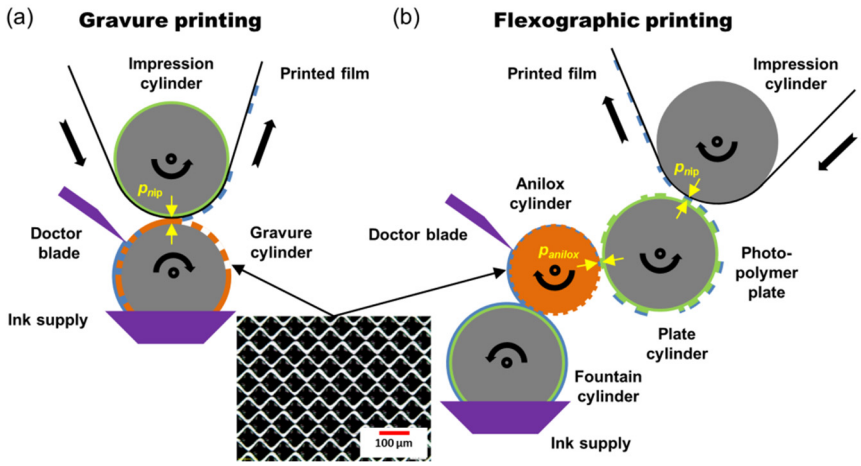

Figure 5. Schematic images of (a) rotary direct gravure and (b) flexographic printing units. Inset shows a cell pattern of the gravure and anilox cylinders.

Contact printing methods

In the most common, high-throughput, contact printing processes, such as screen, gravure, and flexographic printing known from fabric, newspaper, magazine, book, and cardboard printing, the ink is transferred from a patterned image plate or roll on to the receiving substrate under controlled pressure.

In non-contact screen printing shown in Figure 4 (a), ink is squeezed through a mesh of steel or polyester known as the screen, where the line density is low at the image area and high outside the image area. The ink is pushed with a squeegee through the area of low line density on to the substrate, which is held slightly below the screen. In rotary screen printing in Figure 4 (b), the ink is inside a cylinder which also houses the squeegee. Screen printing requires the ink to have high viscosity and thixotropic properties.[8] The method provides a wide range of d, good line definition on a wide range of substrates, and it is relatively low-cost to set up. Screen printing is the most common printing method utilized in the conventional electronics industry, for example in the printing of passive electronic components, etching masks for PCBs, and in Si PVs manufacturing. Nowadays, it is one of the most common techniques utilized in printed electronics research for the printing of OPVs [17], [106], OLEDs [107], [108], and OTFTs [109], [110], as well as RFID antenna structures [111], memory capacitors [112], and Si NP TFTs [113].

In a gravure printing system, an engraved metal image plate is attached to a gravure cylinder. The image area of the image plate, as shown in Figure 5 (a), contains a vast amount of engraved cups of defined geometry. The cups determine the theoretical transfer volume of the ink. The plate is inked in an ink supply and the excess ink is removed with a doctor blade.[114] The doctor blade is kept lubricated by small, deliberate roughness outside the engraved areas. This is, however, observed to let NPs slipping under the blade [8], [115]. The ink is transferred from the engraved cups to the flexible substrate under the nip pressure (p_{nip}) between the gravure cylinder and the impression roll, which is covered by a rubber of defined hardness. Gravure printing can be performed in a direct or indirect fashion with the help of an offset roll [114], [116]. The advantages of gravure printing include a consistent high-quality print result, high-throughput, and durable printing rolls. Disadvantages are that the method requires a smooth substrate surface with a suitably high γ along with a high p_{nip} to attain a good pattern transfer. In addition, cell design and ink optimization are required to avoid visible cell patterns in the printed structures.[114] Gravure printing has been widely used for OPVs [17], [117], OLEDs [118], and OTFTs [17], [74], [119], as well as conductors [120]–[122], antennas for RFID [19], [123], diodes [124], memories [8], [125], and MO TFTs [126].

[8] Thixotropic inks exhibit a shear-thinning behavior, where the apparent viscosity of the ink decreases with increasing shear rate. This allows the initially viscous ink to flow through the opening of the mesh as the ink experiences high shear induced by the squeegee. When the ink then attaches to the substrate surface, the ink settles quickly as the ink returns to its initial highly viscous state.

In flexographic printing, shown in Figure 5 (b), the ink is transferred to the flexible substrate in a rotary fashion using two cylinders, namely the anilox and the plate cylinders. The ceramic anilox cylinder, similar to a uniformly engraved gravure coating cylinder, is used to determine the theoretical transfer volume of the ink. The anilox is inked by the ink supply and the excess ink is scraped off by a doctor blade or a doctor roll. The printed image is defined by a relief pattern on a flexible plate that is made out of a photopolymer of a defined hardness and wrapped around the plate cylinder. The ink is transferred from the anilox to the plate cylinder under pressure (p_{anilox}) and the inked image to the substrate under the p_{nip} between the plate cylinder and an impression cylinder.[127] In principle, flexographic printing separates the ink metering and the printing steps, which enables more control of the printing process and allows a lower p_{nip} than in gravure. A disadvantage is that the method produces an inferior print quality than gravure printing as the flexible plate can distort under pressure [127]. The photopolymer printing plates are low-cost, but not as long-lived as the gravure plates. Flexographic printing has been utilized in the printing of OTFTs [74], [128], CNT-FETs [76], and MO TFTs [129, I].

Reverse offset is a novel contact printing method, which is capable of forming high-resolution patterns with ~ 1 µm L/S-resolution [96]. In reverse offset, shown in Figure 6, a uniform coating of a semi-dry ink on a polydimethylsiloxane (PDMS) blanket is subjected to a relief pattern (cliché) on glass or metal consisting of a negative image of the desired pattern. The high γ of the relief removes the ink from the areas outside of the desired pattern (off-step) on the PDMS blanket with low-γ (~ 20 mN/m). The patterned blanket is then used to print the desired pattern onto the final flexible substrate (set-step).[96] The method has been used to print OTFTs [96], [130], contact electrodes for MO TFTs [131], and fuse-type write-once-read-many memories [10].

Non-contact digital printing techniques

In drop-on-demand (DoD) inkjet printing, a printhead moves over the substrate and a low-viscosity liquid ink is ejected as droplets onto digitally defined locations. The droplet is formed by forcing the ink through a small orifice in a printing nozzle with either a thermal or a piezoelectric pulse. A schematic image of both types is shown in Figure 7. In thermal inkjet, the ink is boiled with a heater element located in the ink chamber of the printhead. The bubbles created on the surface of the heater expand rapidly and provide a pressure that forces the ink through the nozzle orifice. The bubble bursts and the volume once occupied by the bubble is filled with ink from the ink reservoir. In piezoelectric inkjet, the pressure pulse is provided by an expanding piezoelectric film in the ink chamber. In both types, an electrical signal is provided to the element and by changing the waveform (i.e. the duration, shape, and amplitude of the electrical pulse) the acoustic resonances occurring in the nozzle chamber change. This allows the drop formation dynamics and the droplet in-flight speed to be digitally controlled.[132]

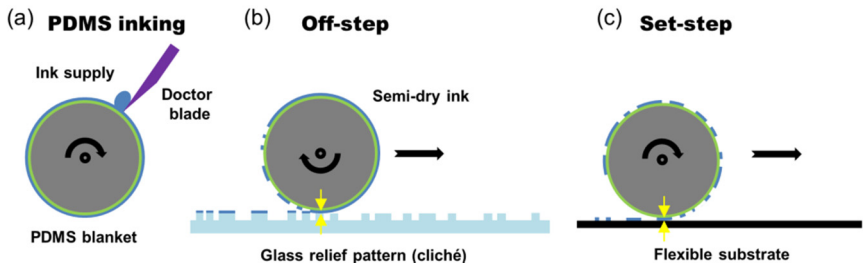

Figure 6. Schematic image showing the main steps of the reverse offset printing.

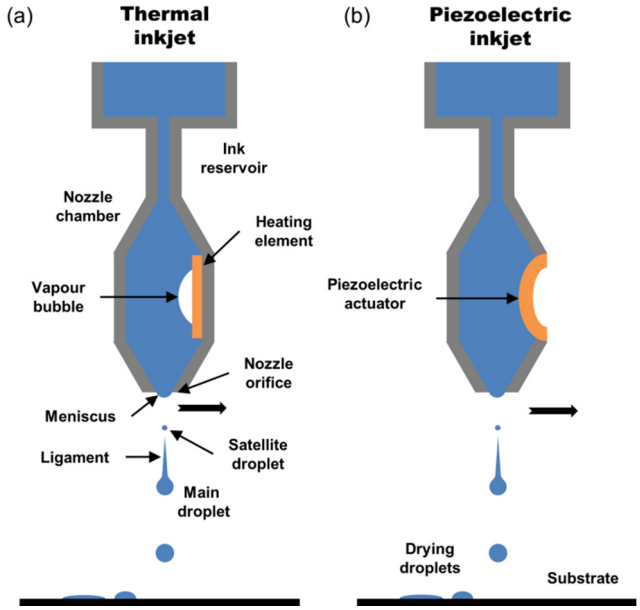

Figure 7. Schematic image of the nozzle of (a) a thermal and (b) a piezoelectric inkjet system.

A short column of liquid ejected at the nozzle orifice forms a main droplet due to surface tension. The size of the main droplet is roughly determined by the diameter of the nozzle orifice. The main droplet is followed by a thin ligament that can break into small satellite droplets tailing the main droplet as shown in Figure 7. In order to retain a good printing quality, the satellite droplets need to have a straight trajectory and catch the main droplet before they impact the substrate.[132]

The droplet formation is dependent on the physical properties of the ink. Several parameters have been used to describe the behavior of the liquid droplets. The inverse of the Ohnesorge number, the so-called Z-value, is shown to give an estimate for stabile droplet formation.[132] The Z-value is defined as

$$Z = \frac{\sqrt{\gamma \rho a}}{\eta}, \tag{2}$$

where γ is the surface tension, ρ the density, and η the viscosity of the ink. a is the characteristic length, such as the diameter of the nozzle orifice. Stabile droplet formation is obtained at $1 < Z < 10$: when $Z < 1$, the ink has generally too high η for stabile jetting, and when $Z > 10$, the ink forms unstable satellite droplets [132].

The droplet volume for the DoD inkjet is typically $1 - 10$ pl, which sets the limitation for the smallest achievable L/S-resolution to be ~ 30 µm.[9] In addition to the high resolution, the benefits of DoD ink-jet printing include low material consumption, high overlay accuracy (~ 10 µm), and digital patterning without printing plate manufacturing. Inkjet printing is of benefit in applications requiring dense structures, where the movement of the printhead, that ultimately limits the throughput, is limited. Inkjet printing is the most widely used printing method in printed electronics research and is utilized in creating OLEDs [40], [41], OPVs [17], and OTFTs [42], [73], [74], [125], [133], as well as sensors [134], memories [6], Si TFTs [135], and MO TFTs [III], [IV], [55], [85]. As a testimony to the general applicability of inkjet printing, it has been upscaled for large-area printing of RGB subpixels in OLED displays. The application-case requires demanding process conditions, such as contamination-free operation, an inert atmosphere, and reproducible droplet characteristics [18].

Novel inkjet-type printing methods where the droplet volume is reduced by external electric fields have been developed to improve the L/S-resolution. Super inkjet (SIJ) printing provides droplets in the $1 - 10$ fL range and leads to an ultimate resolution of ~ 1 µm.[10] The nozzle consists of a capillary tube with a ~ 1 µm diameter orifice, a hydrophobic outer coating, and a thin conductor wire inside the tube. A fL-droplet is ejected with the help of a pressure pulse, and the electric field is used to charge the ink.[136], [137] SIJ has been used to create, e.g. Cu wiring [138], and top-contacts for OTFTs with ~ 1 µm channel length [137]. A variation of the method is electrohydrodynamic-jet (EHD) printing, where a thin capillary tube nozzle is coated on the outside and near the orifice with Au and a hydrophobic coating. A DC electrical field is formed between the charged nozzle and the grounded substrate holder. As a result of the opposing forces, namely the surface tension and the electrostatic attraction, ions present in the ink will be driven to form a cone of liquid at the nozzle orifice, which will release a fL droplet when the electric field is large enough.[139] EHD has been used to fabricate OTFTs with ~ 1 µm channels lengths [139], and MO TFTs [140]–[142].

[9] 1 pL gives an ink droplet diameter of 12 µm, which typically spreads on the substrate, depending on the γ of the substrate and the ink, to at least 3 times it's diameter.

[10] 1 fL yields an ink droplet diameter of ~ 1 µm, which does not typically spread on the substrate, as it dries in-flight or on impact [136], [137].

Conventional vacuum-processes compatible with flexible substrates

Several vacuum-processes known from the conventional electronics industry, such as sputtering, evaporation, and atomic layer deposition (ALD), can be used to deposit thin films on flexible substrates in a continuous R2R-process. The vacuum-deposited layers require patterning, which can be performed in R2R-environment using R2R-photolithography [143], lift-off with printed resist [144] or wet etching using printed etchants [109]. As an example of the recent advances in the most conventional patterning method, overlay accuracy of ~ 2 µm has been achieved in R2R-photolithography on 125 µm thick PET substrate [143]. Sputtering has already been used for decades in the R2R-fabrication of transparent conductors on plastic substrates [145], [146], and, recently, in the fabrication of MO TFTs [147]. R2R-vacuum evaporation with shadow masks was already used by Brody *et al.* for the fabrication of CdSe TFTs on plastic substrates in the 1960s [32], and the technique is still pursued for flexible display backplanes [148]. ALD has been used with plastic substrates in various R2R-processes [149]–[151]. Notably, suitable growth conditions can even be obtained without vacuum through spatial ALD technique, where a moving gas head has a sequence of slits for the inert gas inputs ($\mathrm{N_2}$), precursor gases, and exhausts [149]. ALD-grown MO layers have been patterned via inkjet-printed growth inhibitor polymers [152].

Novel fabrication methods have also been developed that lead to TFTs on flexible substrates. In a roll-transfer method, functional IGZO TFTs were fabricated on rigid substrates with a sacrificial etch layer. After etching, the TFTs were transferred onto flexible substrates by sequential roll stamping and placing [153].

Summary of the most common printing methods for printed electronics

The most common printing methods in printed electronics research are summarized in Table 3 [72], [96], [99], [108], [114], [116], [127], [136], [137], [139], [154]. The selection of the most suitable printing method is often made based on the parameters listed in the table, such as the required linewidth of printed features and the desired thickness of the final layer. As a reference, the values for the overlay accuracy and for the qualitative estimation of the layer thickness control are given for the combination of a generic R2R-vacuum-process and R2R-photolithography [143].

Table 3. Characteristics of the most common printing methods used in the printed electronics research. For linewidth, the minimum reported linewidth is in brackets. SC = semiconductor, SD = source/drain electrodes, and GD = gate dielectric.

Method	**Linewidth (μm)**	**Overlay (μm)**	η **(mPa·s)**	**Wet layer** d **(μm)**	**Layer** d **control**	**Optimal in TFTs for**
Gravure[11]	$\sim 50\ (\sim 2)$	> 30	$50 - 200$	$0.1 - 10$	OK	SC/SD/ GD
Flexography	~ 75	> 30	$50 - 500$	$0.1 - 10$	OK	SC/GD
Screen[12]	$\sim 100\ (\sim 30)$	> 10	$100 - 10^5$	$\sim 0.1 - 100$	Poor	-
Reverse offset[13]	~ 1	< 10	$< 10 / \sim 10^7$	$0.05 - 1$	Good	SC/SD/ GD
Inkjet	~ 30	~ 10	$1 - 40$	$0.1 - 10$	OK	SC/SD
SIJ & EHD	~ 1	~ 1	$\sim 1 - 10^4$	$\sim 0.01 - 10$	Good	SD
R2R-vacuum & photolith.	≤ 4	~ 2	-	-	Very good	SC/SD/ GD

[11] The minimum linewidth is obtained with inverse gravure printing [122].
[12] The minimum linewidth is obtained with screen offset printing [154].
[13] The viscosity is given both for the PDMS coating and the semi-dried offset phases [96].

3. Thin-Film Transistor Operation and Characteristics

Electrical current is carried by charge carriers which are electrons in metals and *n*-type semiconductors and holes in *p*-type semiconductors, respectively.[14] These are accelerated when placed in an external electric field ($\vec{E}$). At low electric fields, this leads to the movement of the electrons towards the higher potential with a collective drift velocity given by $\vec{v}_d = \mu_d \vec{E}$, where μ_d is the drift mobility of the charge carriers (in cm^2/(Vs)). In bulk materials, the movement of the charge carriers is hindered by collisions with the imperfections of the crystal lattice, such as ionized impurities, and the vibrations of the lattice, phonons. μ_d is then defined as $\mu_d = q\langle\tau\rangle/m^*$, where q is the elementary charge, $\langle\tau\rangle$ the average mean free time between the scattering events of the charge carriers and m^* the effective mass.

In thin films, the mobility is further limited by charge trapping in grain boundaries and other structural imperfections that are present, especially in nano- or polycrystalline materials. Also, scattering from the surface roughness of the thin films limits the mobility. The total mobility (μ) for thin-films written with Mathiessen's rule is

$$\mu^{-1} = \sum_i \mu_i^{-1} = \mu_{is}^{-1} + \mu_p^{-1} + \mu_{gb}^{-1} + \mu_s^{-1}, \tag{3}$$

where μ_{is}, μ_p, μ_{gb}, and μ_s are the mobility limited by the ionized impurities, phonon scattering, grain boundaries and other structural imperfections, and the surface roughness, respectively [155]. In thin semiconductor films with a low charge carrier density (n_e, given in cm^{-3}), the μ_{gb} and μ_s are much smaller than μ_{is} and μ_p, and, thus, they dominate in μ.

The current density (J given in A/m^2) is given by Ohm's law $E = \rho J$, where ρ is the resistivity of the material (in Ω·m), which is dependent on the n_e, such that

$$\rho = \sigma^{-1} = (q n_e \mu_d)^{-1}. \tag{4}$$

The ρ can be calculated from the sheet resistance $R_s = \rho/d$, where d is the thickness. R_s can be obtained, e.g. with van der Pauw or four-point collinear probe measurements [155], and n_e can be obtained from Hall-measurements [156].

[14] As all the devices in this work are with *n*-type majority carrier semiconductors and metals, we restrict to the *n*-type and omit any *p*-type minority carrier conductivity.

3.1 Ideal Square-Law Model and Deviations from the Ideal Model

The current-voltage (I-V) operation of an *n*-type TFT is based on the capacitor formed at the metal-insulator-semiconductor (MIS) interface, whose valence band (VB) and conduction band (CB) are bent by the voltage at the gate electrode (V_g). A schematic energy band diagram of an ideal *n*-type MIS interface is shown in Figure 8. In the absence of any voltages, i.e. at the equilibrium flat-band conditions, the Fermi-levels align in the metal and in the semiconductor, which resides close to the CB of the semiconductor due to donor doping. When $V_g < 0$ is applied, the semiconductor is depleted of electrons at the MIS interface and the bands bend upward. The width of the formed depletion layer (w_d) is given by

$$w_d = \left(\frac{2\varepsilon_{sc}\varepsilon_0\varphi_s}{qN_D}\right)^{1/2}, \tag{5}$$

where ε_{sc} and ε_0 are the relative permittivity of the semiconductor and vacuum permittivity, φ_s is the surface potential, and N_D the donor density (in cm^{-3}) [156]. Electrons are accumulated at the interface when $V_g > 0$ is applied. At large enough positive V_g, the Fermi-level aligns with the edge of the CB at the interface. The electrons are carried in the formed accumulation layer from the source contact kept at ground to the drain contact held at higher potential. The trap density of the interface (N_t) affects the gate potential required for the band bending by proving charge traps that need to be filled before the accumulation condition can be achieved, or alternatively, which need to be emptied before the depletion is complete.

All the TFTs in this work are, as shown in Figure 9, bottom-gate top-contact type, which is also known as staggered top contact type. The channel dimensions are defined by the width (W) and the length (L) of the semiconductor area between the S/D electrodes. The operation of the TFTs is divided into cut-off, linear, pre-pinch-off, and saturation operation regimes as shown in Figure 10, which is obtained from a simulation using the ideal square-law model.

In the cut-off regime where $V_g < V_t$ holds, where V_t is the threshold voltage, the semiconductor is at depletion and ideally $I_d = 0$. The semiconductor is at accumulation when $V_g > V_t$ holds. In the linear regime where $V_d \ll V_{d,sat}$ holds, the I_d is linear in terms of V_d. By increasing V_d further, I_d becomes sub-linear in the pre-pinch-off regime due to the diminishing voltage difference between V_d and V_g at the vicinity of the drain. Finally in the saturation regime, the onset of saturation occurs at $V_d = V_{d,sat} = V_g - V_t$ and the channel is pinched-off, where $\partial I_d/\partial V_d = 0$ ideally holds. The equations for the ideal I-V characteristics of TFTs, as derived in Appendix A using the ideal square-law model [156], [157], are:

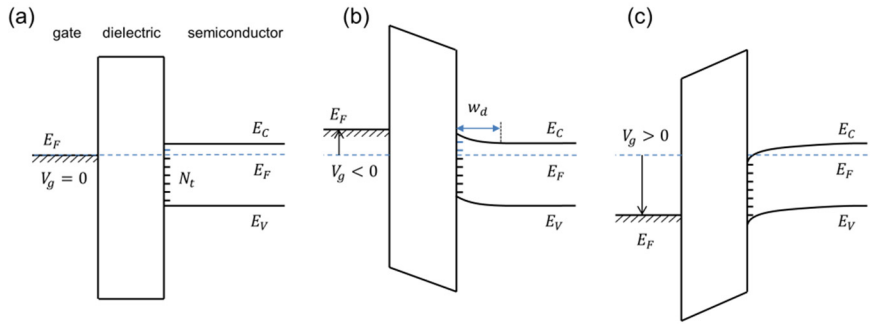

Figure 8. Schematic figure of the energy bands at the gate-dielectric-semiconductor interface of an ideal *n*-type TFT with $V_t = 0$ V (a) at equilibrium, (b) at depletion, and (c) at accumulation conditions. E_C, E_V and E_F are the energy levels of the CB, VB and the Fermi-level, respectively. N_t denotes the interface trap density shown as blue (empty traps) or black (filled traps) lines in the semiconductor gap, which affect the gate potential required for the band bending.

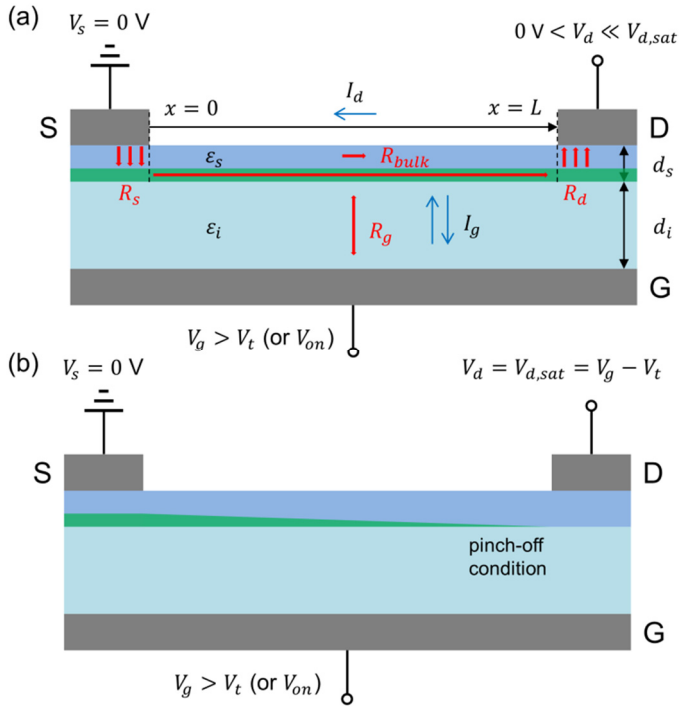

Figure 9. Schematic image of a TFT structure, where the accumulation channel condition is shown in green (a) at pre-pinch-off operation, and (b) at saturation (pinch-off). Red arrows denote the additional parameters to the ideal square-law model of the system, such as the contact resistances (R_s, R_d), gate leakage resistance (R_g), and bulk and/or surface leakage resistance (R_{bulk}).

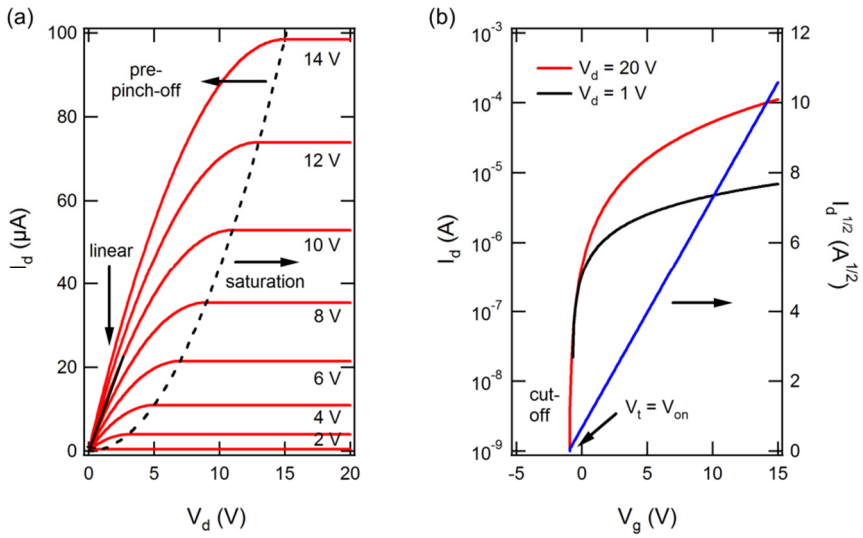

Figure 10. I-V characteristics simulated using the ideal square-law model with $C_i = 35$ nF/cm^2, $W/L = 12.5$, $V_t = -1$ V, and $\mu = 2$ cm^2/(Vs). (a) Output curve for varied V_g. The dashed and solid black lines denote the saturation and linear regimes (for $V_g = 10$ V), respectively. (b) Transfer curve at the linear (black), saturation (red) and cut-off regimes ($V_g < V_t$). $\sqrt{I_d}$ (at saturation) is shown on the right.

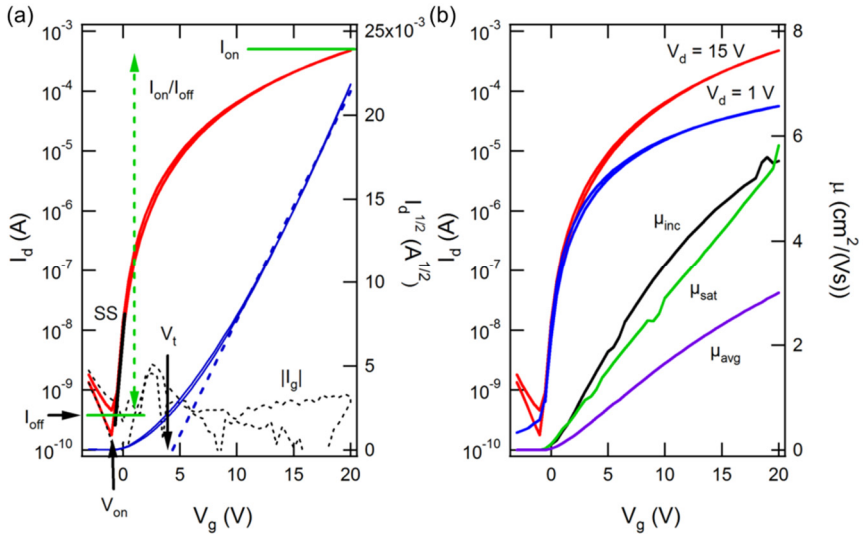

Figure 11. (a) TFT parameters obtained from transfer characteristics measured at saturation ($V_d = 15$ V). The dashed black line denotes the gate-leakage. (b) The V_g-dependent mobility values used in this work. The figures are modified from [I].

$$\begin{aligned}
\text{Cut-off:}\quad & I_d = 0, \text{ at } V_g < V_t \\
\text{Linear:}\quad & I_d = \frac{W}{L}\mu C_i\left(V_g - V_t\right)V_d, \text{at } V_g > V_t \text{ and } V_d \ll V_{d,sat} \\
\text{Pre-pinch-off:}\quad & I_d = \frac{W}{L}\mu C_i\left[\left(V_g - V_t\right)V_d - \frac{V_d^2}{2}\right], \text{at } V_g > V_t \text{ and } V_d < V_{d,sat} \\
\text{Saturation:}\quad & I_d = \frac{W}{2L}\mu C_i\left(V_g - V_t\right)^2, \text{ at } V_g > V_t \text{ and } V_d \geq V_{d,sat}.
\end{aligned} \tag{6}$$

The common parameters that are used to describe the performance of TFTs are shown in Figure 11 (a). The device mobility (μ) is an important parameter in determining the maximum current driving capability and operation speed of TFTs. The mobility parameters used in this work and shown in Figure 11 (b) will be discussed in the next section. The turn-on voltage (V_{on}) gives the V_g when the I_d starts to increase on a logarithmic scale and, thus, it denotes the V_g when the transition initiates from the off- to the on-state. Similarly, the threshold voltage (V_t) roughly estimates when appreciable I_d starts to flow on a linear scale. Several methods exist for determining the V_t, however, they can lead to differing results [155]. V_{on} is a more useful metric than V_t for the operation of TFTs as switches, such as for pixel driver TFTs. As V_t can't be unambiguously determined, V_{on} is often preferred in the literature for MO TFTs [158]. The drain current on-off-ratio (I_{on}/I_{off}) denotes the maximum difference between the on- and off-state current of the device. Whereas I_{on} is limited by the parameters in Equation (6), I_{off} is limited either by (i) the gate leakage current (I_g), as shown in Figure 11 (a), (ii) the bulk/surface leakage due to large n_e of the semiconductor (see below), or (iii) the noise floor of the instrument. The subthreshold swing (SS) is defined as the minimum voltage required to increase I_d by one decade and is obtained at the maximum slope of the transition:

$$SS = \max\left[\left(\frac{d\log I_d}{dV_g}\right)^{-1}\right]. \tag{7}$$

The SS can be used to estimate the interface trap density (N_t) of the MIS interface. Decrease in SS indicates a reduction in the N_t, which can be calculated from

$$N_t = \left(\frac{SS\cdot\log e\cdot q}{k_B T} - 1\right)\frac{C_i}{q}, \tag{8}$$

where q is the elementary charge, k_B the Boltzmann constant, T the temperature and C_i the capacitance density of the gate dielectric, respectively [53]. As the interface traps have to be filled before the accumulation layer can be formed, a higher swing in V_g is required for increasing N_t.

Real TFTs have several non-idealities that can be taken into account by introducing additional parameters to the ideal square-law model [157], [159]. As shown in Figure 9 (a), those include (i) contact resistances R_s and R_d that are in series with the channel resistance (R_{chan}) and can be measured, e.g. via transfer-length method, (ii) gate leakage as R_g that is in parallel to R_{chan} and calculated typically

from the measured $I_g(V_g)$, (iii) bulk and surface leakage as R_{bulk} that are in parallel to R_{chan} and can be obtained at saturation from $R_{bulk} = (\partial I_d/\partial V_d)^{-1}$, (iv) discrete charge traps (acceptor or donor type) that affect the sub-threshold characteristics (V_t and V_{on}) [155], [159], and (v) overlap capacitances between the gate and source/drain electrodes that affect the operation frequency of the TFTs, as discussed further in Chapter 3.3.

The bulk/surface leakage of the TFTs can lead to poor gate modulation and is important to the operation of TFTs with thin In_2O_3 semiconductor with possibly high n_e, as discussed later in the Chapters 4.3 and 6.2. The bulk leakage is manifested as follows: when the thickness of the semiconductor is larger than the depletion width given by Equation (5) ($d_s \gg w_d$), the unmodulated part of the semiconductor, called the back-channel, will contribute to the charge carrier conduction, depending on n_e of the semiconductor [159]. For bottom-gated TFTs without encapsulation, gas molecules, such as O_2, H_2O, and CO, adsorbed on the exposed semiconductor surface can undergo a partial charge transfer between the molecules and the semiconductor. Depending on the molecule, this leads to changes in the back-channel: O_2 leads to a surface depletion region and H_2O and CO to a surface accumulation region that gives rise to surface leakage [160]–[164]. These effects are especially amplified for porous nano- and polycrystalline semiconductors due to their large surface areas [160].

3.2 Models with Gate-Voltage-Dependent Device Mobility

The gate voltage-dependent mobility of the MO TFT devices leads to a large deviation from the ideal TFT model, where μ is constant. The calculation of the gate-dependent μ is preferred over a single, maximum μ value to give valuable information on the device physics [46]. The gate-dependent mobility equations based on the ideal model are derived in Appendix A and listed here:

$$\begin{aligned}
\mu_{FE} &= g_m(V_g)\Big/\Big(\frac{W}{L}C_iV_d\Big) = \frac{\partial I_d(V_g)}{\partial V_g}\Big/\Big(\frac{W}{L}C_iV_d\Big) \\
\mu_{eff} &= g_d(V_g)\Big/\Big[\frac{W}{L}C_i(V_g - V_t)\Big] = \frac{\partial I_d(V_g)}{\partial V_d}\Big/\Big[\frac{W}{L}C_i(V_g - V_t)\Big] \\
\mu_{sat} &= \left[\frac{\partial\sqrt{I_d(V_g)}}{\partial V_g}\right]^2\Big/\Big(\frac{W}{2L}C_i\Big).
\end{aligned} \tag{9}$$

The field-effect mobility (μ_{FE}) and the average mobility (μ_{avg}) are defined from the gate-dependent transconductance ($g_m(V_g) = \Delta I_{out}/\Delta V_{in} = \partial I_d(V_g)/\partial V_g$, where I_{out} and V_{in} are the output current and input voltage) and drain (or output) conductance ($g_d(V_g) = \Delta I_{out}/\Delta V_{out} = \partial I_d(V_g)/\partial V_d$, where V_{out} is the output voltage) at the linear region, respectively, whereas the saturation mobility (μ_{sat}) is obtained at saturation. As μ_{sat} is measured at large V_d, it is less affected by R_s or R_d than μ_{FE} or μ_{avg}, but it is calculated at the pinch-off conditions, where the effective L of the channel is not well known [46].

At a large V_g range, the accumulated channel is drawn closer to the semiconductor-insulator interface and the device mobility can become limited by the increased scattering from the interface roughness. This can be taken into account by introducing a V_g-dependent parameter (β) to the mobility such that

$$\mu(V_g) = \frac{\mu_0(V_g)}{1 + \beta(V_g - V_{on})}, \tag{10}$$

where μ_0 is the mobility without the interface roughness degradation [155], [159].

Alternative, physically-based mobility values were introduced by Hoffman to replace μ_{FE} by μ_{inc}, and μ_{eff} by μ_{avg} for non-ideal TFTs such as polycrystalline ZnO [158]. These are obtained at low V_d from

$$\begin{aligned} \mu_{inc} &= \frac{\partial g_d(V_g)}{\partial V_g} \Big/ \left(\frac{W}{L} C_i\right) \\ \mu_{avg} &= g_d(V_g) \Big/ \left[\frac{W}{L} C_i (V_g - V_{on})\right]. \end{aligned} \tag{11}$$

μ_{inc} is the mobility of the charge carriers incrementally added to the channel, whereas μ_{avg} gives the average mobility of all charge carriers in the channel and is more useful for estimating device operation in circuits. Notably, μ_{avg} is similar to μ_{eff} where the V_t is replaced with the V_{on}, which is more readily determined. To ease the calculations, the drain conductance can be approximated with conductance at low V_d, giving $g_d(V_g) \approx G_d(V_g)$ [159].

The charge transport in polycrystalline TFTs has been modeled with the help of charge traps at the grain boundaries by Levinson *et al.* for CdSe and poly-Si TFTs [165], and Hossain *et al.* for ZnO TFTs [166]. In short, the trapped (negative) charge residing at E_T energy below the Fermi-level induces a depletion-region at the grain boundaries, as shown in Figure 12. This leads to the formation of a potential barrier E_B in the CB that the charge carriers need to surmount with thermionic emission. The height of E_B is modulated by the charge density in the channel and is V_g-dependent. The I-V characteristics are derived in Appendix A based on the Levinson model in ref. [165]. The model predicts a gate-dependent mobility in the form of $\mu = \mu_{gb} e^{-E_B/k_B T}$, where μ_{gb} is the grain-boundary mobility and $E_B \propto V_g^{-1}$. I_d at the linear region can be obtained for low V_d and large V_g from

$$I_d \approx \frac{W}{L} \mu_{gb} C_i V_g V_d e^{-(q^3 N_t^2 d_s)/(8\varepsilon_{sc}\varepsilon_0 C_i V_g k_B T)}, \tag{12}$$

where N_t is the sheet density of the grain boundary traps, d_s the semiconductor thickness, ε_{sc} the semiconductor relative permittivity, ε_0 the vacuum permittivity, k_B the Boltzmann's constant and T the temperature. The most important insight from the model is that nano- and polycrystalline semiconductors with moderately high n_e can still show effective gate-modulation due to the presence of the depletion-regions at the grain boundaries.

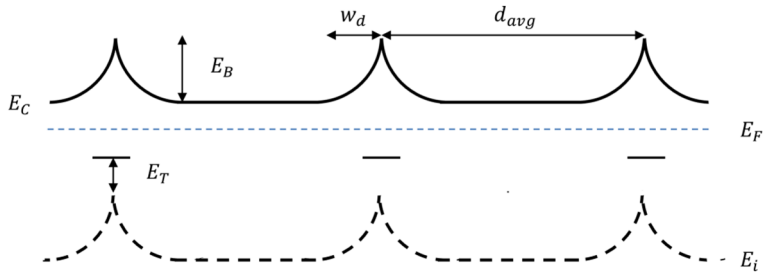

Figure 12. Schematic energy band diagram of a poly- or nanocrystalline semiconductor with grain boundary traps at energy of E_T and energy barriers E_B at the CB. d_{avg} is the average crystallite size.

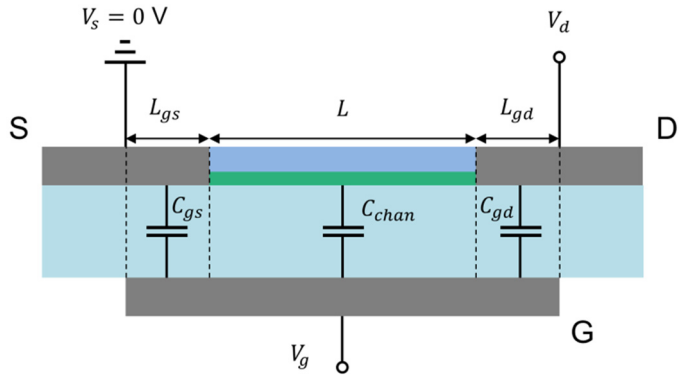

Figure 13. Overlap capacitances of a real TFT device that affect the operation frequency of the TFT.

For amorphous IGZO, the I-V characteristics have been modelled by Abe *et al.* using a simple power law, where μ depends on V_g [167]. At the V_g-range when $E_F < E_C$ holds, the current is trap-limited by sub-gap states, whereas at higher V_g-range, when $E_F > E_C$ holds, the current becomes percolation-limited over potential barriers at the E_C-level caused by local disorder [168]. The V_g-dependent average mobility is derived in Appendix A based on ref. [167] and is in the form of

$$\mu_{avg}(V_g) = \alpha(V_g - V_{on})^{\beta}. \tag{13}$$

where α and β are the fitting parameters.

3.3 Quasi-Static Maximum Operation Frequency

In addition to the channel capacitances between the gate and the accumulation layer, real TFTs have an overlap capacitance between the gate-electrode and the source/drain electrodes, as shown in Figure 13. This affects the maximum operation frequency of the TFTs. We can consider the total gate-capacitance as a sum of the capacitances in parallel and write $C_{gate} = C_{chan} + C_{gs} + C_{gd} = C_i W(L + L_{gs} + L_{gd})$, where C_{chan}, C_{gs}, and C_{gd} are the channel, gate-source, and gate-drain capacitances, and L, L_{gs}, and L_{ds} the channel, gate-source overlap, and drain-source overlap lengths, respectively. In a quasi-static estimation (instantaneous voltages) for the maximum operation frequency of a TFT, the unity-gain frequency[15] f_t is given by $f_t = 1/T_c$, where T_c denotes the time required to empty and fill the capacitor C_{gate} by swinging the gate-field. The unity-gain frequency at saturation region ($V_d = V_g - V_t$) is derived in Appendix A based on ref. [69] and is given by

$$f_t = \frac{\mu_{sat}(V_g - V_t)}{2\pi L(L + L_{gs})}. \tag{14}$$

[15] f_t is the frequency when the ratio between the output and the input current (gain) is unity.

4. Metal Oxide Semiconductors for Solution-Processed Thin-Film Transistors

The first part of this chapter provides an overview of the general properties of transparent semiconducting MOs. As In_2O_3 was selected as the semiconductor material for the printed and low-T processed MO TFTs developed in this thesis, the properties of In_2O_3 and its prior use as a TFT semiconductor channel are reviewed first. Then, the solution-processing of MO semiconductors and their low-T annealing methods are introduced, where special focus is given to the UV-assisted annealing methods also utilized in this thesis. The state of the art printed MO TFTs are reviewed in the last part of the chapter.

4.1 Transparent Semiconducting Metal Oxides

Undoped semiconducting MOs, such as In_2O_3, ZnO, and SnO_2 are transparent, wide band-gap *n*-type semiconductors due to their large optical band gap of > 3 eV [159], [169], [170].[16] The CBs of these ionic materials are built mostly of metal *ns* orbitals ($4s$ for Zn and $5s$ for In and Sn)[17] with a minor contribution from oxygen 2p orbitals, whereas the relatively flat VB arises from oxygen 2p orbitals. The CBs are parabolic, free-electron-like with large dispersions, i.e. high curvature of the energy band. For the energy of the parabolic CBs and for their curvature we can write:

$$E(\vec{k}) \propto \frac{\hbar^2 k^2}{2m^*} \rightarrow \frac{\partial^2 E}{\partial k^2} = \frac{\hbar^2}{m^*}, \tag{15}$$

where $\vec{k}$ is the momentum of the electrons in the reciprocal space, $\hbar$ is the reduced Planck's constant, and m^* is the effective mass. Based on Equation (15), the large CB dispersion leads to small m^*, which for In_2O_3 is in the range of $\sim 0.2 - 0.3 m_e$, where m_e is the free electron mass [170]. When recalling that the drift mobility is given by $\mu_d = q\langle\tau\rangle/m^*$, this further leads to a high electron drift mobility for the discussed MO materials.

[16] Throughout this chapter, the focus is on *n*-type MOs.

[17] In^{3+} cations have an electronic configuration of $[Kr](4d)^{10}(5s)^0$.

When these MOs are degenerately doped,[18] they can exhibit high *n*-type conductivity while maintaining a good level of transparency. The conductivity arises from a large charge carrier concentration with n_e up to 10^{21} cm^{-3} and a charge carrier mobility of $\gg 1$ cm^2/(Vs).[19] The transparency in the visible spectrum is retained for doped materials due to both the large bandgap and the low density of states near the CB minimum that leads to an upward shift of the Fermi-level from the CB minimum (Burstein-Moss shift) [169]. The properties allow the doped materials to be used as transparent conductors in solar cells, displays and IR-transmission blocking windows. In the best case, the conductivities can reach up to $\sigma \sim 10^6$ S/m [159], [170].

High n_e can be achieved with donor doping of the MOs, using In_2O_3 as an example, by: (i) intrinsic point defects such as In interstitials (In_i^{3+}) or non-stoichiometric conditions via oxygen deficiency In_2O_{3-x} (oxygen vacancies) or (ii) by extrinsic doping, such as substitutional doping in Sn-doped In_2O_3 (ITO)[20] or H-doping of In_2O_3, where the hydrogen acts as a shallow dopant and occupies an interstitial site (H_i^+) [169], [170]. The oxygen vacancy (V_o) is considered to be stable, but non-conductive (or a deep donor) when in the double-ionized state (V_o^{2+}). When the oxygen vacancy is photo-excited, or partially compensated to the single-ionized state (V_o^+), a meta-stable but conductive (or a shallow donor) state is reached. However, the role of the charge state of the V_o in the charge carrier generation is still under discussion [170].

As the CB of the MO semiconductors consists mainly of spherical metal *ns*-orbitals, the dependence of the charge carrier conduction is relaxed on the inter-atom bond angles (*ns*-*ns* and *ns*-2*p* orbital overlaps) for the network of atoms taking part in the charge conduction. Therefore, the materials can exhibit comparable carrier mobility even in the disordered amorphous phase that lacks a long range order.[51], [169] This is in contrast to the covalently bonded a-Si:H, which possesses a highly directional sp^3-hybridized CB and, as a result, shows limited mobility in the amorphous phase (~ 1 cm^2/(Vs)) when compared to polycrystalline Si (> 50 cm^2/(Vs)) [51]. Binary oxides, such as In_2O_3, ZnO and SnO_2, are typically nano- or polycrystalline, although they can also be fabricated as amorphous films [171]–[173]. The amorphous phase offers some advantages over nano- or polycrystalline phases for MOs used in TFT applications: amorphous MOs (i) provide a greater uniformity over large areas [53], (ii) exhibit a mobility that is not limited by charge trapping at the grain boundaries but by small potential barriers in the CB that are caused by the local disorder [46], [53], (iii) generally show a lower film roughness, and (iv) can be processed at lower substrate temperature during sputtering. Typically, the as-grown, sputtered MO films have non-optimal TFT operation characteristics and require annealing treatments to stabilize a good TFT oper-

[18] In degenerate doping, the localized impurity or dopant states broaden into a continuous band and shift the Fermi-level of the material into the CB.

[19] Hall mobility values up to ~190 cm^2/(Vs) have been reported for bulk crystalline In_2O_3 [170].

[20] Sn^{4+} substituted at In^{3+} site contributes a single electron to the conduction band of In_2O_3 and a 1 % atom concentration of Sn yields $n_e \sim 10^{20}$ cm^{-3}.

ation [53], [174]. The amorphous phase can be retained during such heating steps by incorporating dopants with large enough cation radii that distort the lattice formation of the polycrystalline host oxide, such as Ga, Ba, or Sr for IZO, while carefully controlling the material composition of the multicomponent MO.[174], [175] Similarly for the solution-processed MO films, the aforementioned doping scheme leads to amorphous multicomponent MO films. However, these multicomponent MO films often require a higher temperature to complete the precursor-to-metal conversion and to reach impurity-free MO films than is required by the MO host oxide. Recently, polymers, such as PVP or PEI, have been used in retaining the amorphous phase of In_2O_3 during low-T annealing of the precursor films [176], [177].

In TFT applications, a low n_e of the semiconductor channel is a necessity for an efficient gate modulation and for the realization of a low I_{off}. For MO semiconductors, this can be reached (i) with films that are close to stoichiometric, i.e. by limiting the creation of V_O, (ii) by limiting the d of exposed semiconductor layer, which allows the formation of a back-channel depletion region with adsorbed oxygen molecules, and, (iii) for nano- and polycrystalline materials, by the compensating effect of the depletion regions formed at the grain boundaries that lower the charge carrier density available at the CB [46], [159]. It is generally noted, that the main method for limiting the n_e of the sputtered or solution-processed MOs is to reduce the concentration of V_O by introducing dopant metals that form stronger oxygen bonds than the MO host oxide. This is manifested as a more negative Gibbs free energy of oxidation per mole of O_2 for the dopant oxides than the MO host oxide. Al, Ba, Ga, Si, Sr and Ti have been successfully used as such oxygen-binding dopants for In_2O_3, or IZO-based semiconductors [46], [87], [175], [178]–[180].

4.2 Solution-Processed Metal Oxide Thin-Film Transistors

The low-cost solution-processing approach has now been pursued for over a decade for the fabrication of MO semiconductor films. MO layers can be processed from sol-gel-type precursor and nanoparticle routes. Generally, the MO NPs are stabilized with organic ligands and they require a three-step heating process: (i) drying of the solvent, (ii) removal of the encapsulation, and (iii) necking and sintering of the NPs for the formation of a connected network. Even if the last step is performed at high temperature, abundant grain boundaries and pores remain in the polycrystalline films, which affect the transport properties of the NP-derived semiconductor films [56]. As a notable exception, polycrystalline IGZO NPs synthesized at high temperature and pressure could be processed from an aqueous dispersion for dense semiconductor films at 95 °C processing temperature [181]. Also, chemical removal of the encapsulating polymers of In_2O_3 NPs has been performed at RT [182] using a process that resembles the chemical sintering of metallic NPs [13]. In the work, successful TFT operation was demonstrated only with a solid electrolyte-gate that can be understood to effectively gate the porous,

NP-derived In_2O_3 film but, as a drawback, lead to highly f-dependent operation characteristics [182].

In sol-gel-type MO precursors, the metal cations are coordinated by organic or inorganic ligands or counter ions. Metal alkoxides [84], [175], metal ammine-hydroxo complexes ($M(OH)_x(NH3)_{y^{(2-x)+}}$) [183], as well as metal salts, such as metal halides ($M\text{-}Cl_x$) [85], metal acetates ($M\text{-}(CH_3COO)_x$) [88], and metal nitrates ($M\text{-}(NO_3)_x$) [86]–[88], have been successfully used as precursors for MO semiconductors in TFTs. The precursors can be deposited on the substrate as discrete molecules in an inert solvent that doesn't react with the alkoxides or the salts [84], [85], or in a solvent that dissociates and reacts with the metal cations, however, this often requires avoiding the precipitation or gelling of the sol by incorporating stabilizers [184].

The precursors are converted to dense and homogenous MO films via heat treatment at sufficiently high temperature. The exact precursor-to-metal-oxide conversion is a complex process with many intermediates and reaction products. In an oversimplified picture, the synthesis of the metal salt precursor, the thermal decomposition, and the formation of impurity-free MO films proceed typically through the following steps: (i) hydration/solvation, (ii) hydrolysis, (iii) condensation, (iv) MO network re-arrangement, impurity removal and film densification, and, depending on the T_{ann} used and the MO material, (v) partial crystallization [56], [180].

In the hydration/solvation step that occurs in a dissociating solvent, the metal complex containing the metal cation and the counter anions (denoted here as $M\text{-}X$) is broken as shown in the schematic Figure 14. This occurs in the metal nitrate salts when they are dissolved in 2-methoxyethanol ($H_3COCH_2CH_2OH$, 2-ME), as used in this thesis. The metal cation is then coordinated by aqua ligands (hydration) or solvent molecules (solvation). In hydrolysis, the metal cation is partly hydrolyzed to $M\text{-}OH$ (hydroxo ligand) by the aqua ligand or to $M\text{-}OR$ (alkoxide) by a protic polar solvent.[21] The hydrolysed metal then proceeds through the generation of oxo-bridges $\text{-}M\text{-}OH + OH\text{-}M\text{-} \rightarrow \text{-}M\text{-}O\text{-}M\text{-} + H_2O$ with the liberation of H_2O in progressive condensation reactions [56]. After the formation of metal oxide networks, further annealing is required to (i) remove impurities, such as the cationic counter ions, condensation products and the remnant hydroxyl groups, (ii) rearrange the film for highly connected $\text{-}M\text{-}O\text{-}M\text{-}$ networks, (iii) densify the film from porosity generated by escaping gaseous reaction products, and (iv) generate a necessary V_o-concentration for *n*-type doping [56].

The hydrolysis and condensation processes are speculated to already start in the liquid phase during the mixing of hydrated metal nitrates at elevated temperature, already yielding partial $\text{-}M\text{-}O\text{-}M\text{-}$ networks prior to deposition [90], as shown in the schematic Figure 14. This is expected to aid in the precursor-to-metal-oxide conversion to occur at low-T [90], [185].

[21] The metal salt is dissolved by the protic solvent that donates a proton:
$M\text{-}X + R\text{-}OH \rightarrow M\text{-}OR + H\text{-}X$.

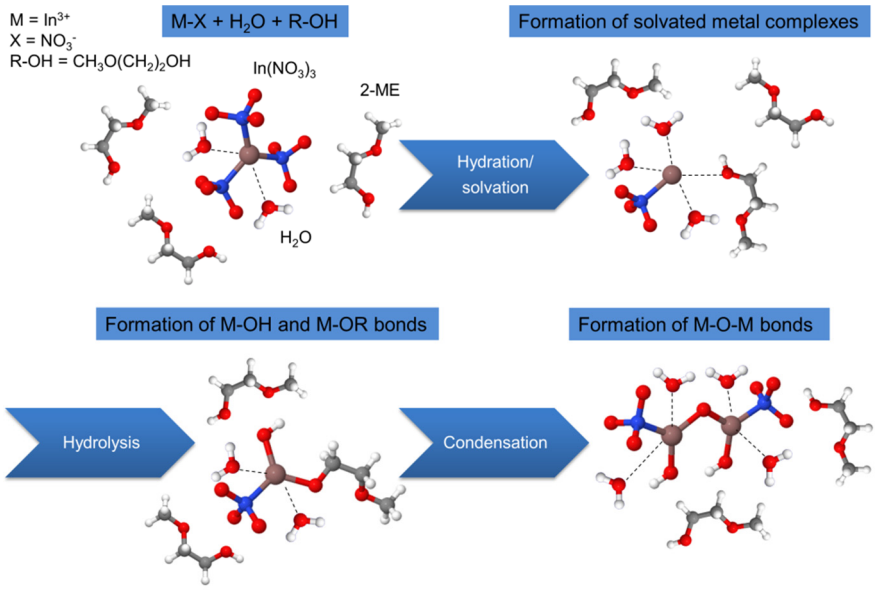

Figure 14. Schematic image of the hydration/solvation, hydrolysis and condensation processes in the synthesis of the precursor solution that are suggested to proceed during the mixing performed at elevated temperature.

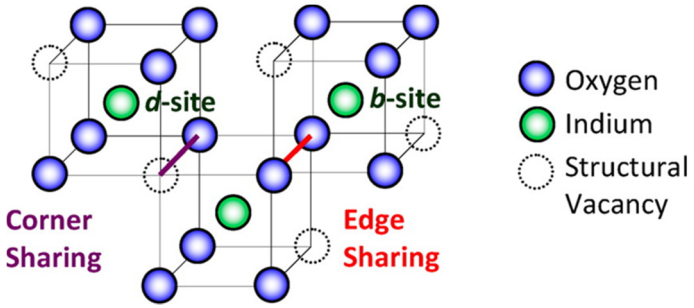

Figure 15. Bixbyite crystal structure of In_2O_3 with two In-sites and two connections of adjacent polyhedra. Reprinted with Permission from [171]. © 2014 American Chemical Society.

4.3 In_2O_3 as *n*-type Semiconductor Material for Thin-Film Transistors

We now focus on the In_2O_3 material that is used in this thesis. In_2O_3 crystallizes in the cubic bixbyite lattice, as shown in Figure 15. The In-atoms are octahedrally coordinated by six oxygen atoms in the InO_6 polyhedra with two structural vacancies at two different sites. The *d*-site and *b*-site vacancies are either face diagonal-

ly or body diagonally located, respectively. These two sites result in different connections between the adjacent polyhedra, namely the corner-sharing and edge-sharing with one or two shared oxygen atoms between the adjacent polyhedra, respectively.[171]

As thin films, the crystallinity of In_2O_3 ranges from amorphous to nano- and polycrystalline films.[22] The structure-electrical property relationship of the amorphous phase of In_2O_3 has been studied in-depth by Buchholz *et al*. [171]. In their work, they show that the Hall mobility for pulsed-laser-deposited (PLD) In_2O_3 thin films is dependent on the crystal-to-amorphous ratio, i.e. the degree of nanocrystalline inclusions in an amorphous matrix, or amorphous inclusions in a crystalline matrix. The presence of inclusions will enhance charge scattering and reduce the mobility. Moreover, amorphous In_2O_3 was observed to have a maximum of μ_H near the onset of the crystalline inclusions in tandem with a reduced degree of edge-shared InO_x polyhedra. This leads to large metal-oxygen-metal (M-O-M) bond angles and allows the formation of highly connected networks of InO_x polyhedra. The networks promote a high μ in the amorphous phase before they condense as nanocrystalline inclusions that limit the μ by the enhanced scattering.[171] Even for the a-IGZO, the CB has been reported to be predominantly made of a connected network of InO_x polyhedra, which indicates that the high mobility of > 10 cm^2/(Vs) observed for a-IGZO is facilitated by the In_2O_3 phase [186].

Both the conventional vacuum-processing and varied solution-processing methods have been used to create In_2O_3 semiconductor layers for TFT applications. For the vacuum-processes, ion-assisted deposition (IAD) of In_2O_3 produced polycrystalline semiconductor films, which allowed TFTs with $\mu \sim 10$ cm^2/(Vs) on SiO_2 gate insulator layers. The highlight of the work was the processing performed at RT and the good $I_{on}/I_{off} \sim 10^5$ of the devices [187]. Reactive thermal deposition of In in the presence of O_2 gas yielded polycrystalline In_2O_3 films where a highly thickness dependent mobility was reported [188]. For sputtered In_2O_3 films, the semiconductor films are argued to have a too high a charge carrier concentration ($n_e \sim 10^{18}$ cm^{-3}) for successful TFT operation [46]. However, by controlling the semiconductor thickness, thin sputtered In_2O_3 films with $d_s = 8$ nm have been shown to exhibit excellent switching properties with $\mu \sim 15$ cm^2/(Vs) and $V_{on} \approx 0$ V, which allows unipolar operation of the In_2O_3 devices [189].

In_2O_3 films with d_s below 10 nm are also easily obtained with solution-processing. Spin-coating is the most frequently used solution-processing method and numerous spin-coated In_2O_3 TFTs have been reported with varying μ and V_{on}, which depend on the precursor annealing method and temperature, and on the d_s [I], [86], [90], [176], [177], [185], [190]–[194]. Spray pyrolysis has been used to deposit thin ($d_s < 10$ nm) polycrystalline In_2O_3 layers with large lateral crystallite dimensions of $30 - 60$ nm that resulted in TFTs with a high mobility of $\mu \sim 15 - 20$ cm^2/(Vs). However, these devices required negative V_g for completely turn-off the devices, thus indicating a high n_e.[103] Inkjet-printed, nano- or polycrystalline

[22] In this context, we denote a material with crystalline inclusions of ≤ 10 nm in average size in an otherwise amorphous matrix as nanocrystalline.

In_2O_3 films on Si/SiO_2 substrates yielded TFTs with mobility in the range of $\sim 3-4$ $cm^2/(Vs)$, depending on the processing conditions of the printed films [195].

The as-fabricated, vacuum-processed In_2O_3 thin films are nano- or polycrystalline when the process temperature is RT or higher [171], [187]–[189]. With solution-process, amorphous In_2O_3 films have also been obtained from In-precursors [190]–[192]. However, the crystallization of the amorphous films into nano- and polycrystalline In_2O_3 can occur even at the relatively low temperature of ~ 200 °C during the precursor annealing process [191], [195]. Therefore, for the solution-processed In_2O_3 films, the selection of the T_{ann} is a balance between the onset of a significant degree of the crystalline inclusions that can limit the μ and the minimum T_{ann} required for attaining a successful precursor to metal-oxide conversion and impurity-free In_2O_3 films. The comprehensive effects of the precursor properties, annealing conditions, underlying surface properties, and layer thickness on the crystallinity of the solution-processed In_2O_3 films still need further studies.

4.4 Low-Temperature Annealing Methods

The minimum decomposition temperature of the precursors is dependent on the precursor chemistry and on the processing conditions. The electronic transport properties of the solution-processed MO TFTs are greatly affected by the oxygen vacancy, hydroxide, and impurity concentrations of the semiconductor films. Several low-T annealing methods have been developed that focus on either improving the condensation process or the impurity removal steps at low-T. In this section, the principles of the low-T annealing methods are briefly reviewed. For the sake of brevity, only the μ obtained at the lowest external temperature is noted. Special attention is given to UV-assisted annealing utilized in the thesis.

Metal nitrates are promising precursor candidates for the fabrication of printed and low-T-processed MO films: (i) they are readily soluble in H_2O or alcohols, (ii) they allow processing in ambient conditions, (iii) they have been generally shown to enable processing at lower temperatures than corresponding chloride or acetate-based precursors, and (iv) they can be processed using an environmentally-friendly process from aqueous solutions [191], [194]. The reduced annealing temperature possibly results from the enhanced decomposition of the nitrate anion when compared to chloride and acetate anions [87], [88], [180]. Metal acetates require stabilizers for fabricating stable solutions [184], whereas dilute metal nitrate precursors have been dissolved in 2-ME as stable solutions without the use of stabilizers [90]. Metal alkoxide precursors prepared and deposited in inert conditions have been shown to lead to high-performance MO TFT devices via a controlled hydrolysis step performed at low-T where the μ and the operational stability of the devices was comparable to sputtered MO TFTs [84]. From a printing perspective, special attention would be required to realize printing at inert conditions, or, alternatively, tuning of the metal alkoxide inks for increased stability in air to avoid premature hydrolysis during the printing step.

Table 4. Low-T annealing methods for solution-processed MO TFTs at $T_{ann} \leq 230$ °C in ascending order of T_{ann}. ↑ denotes enhanced and ↓ depressed effect.

SC	Sol-gel type	Annealing method	Main process mechanism	μ (cm^2/Vs)	T_{ann} (°C)	t_{ann} (min)	Ref.
IGZO	NPs from nitrate	laser annealing	↑ crystallinity	7.65	95	10	[196]
ZnO	ammine-hydroxo	inert annealing	high-reactivity of precursor	1.2	100	60	[197]
In_2O_3	aqueous nitrate	vacuum post-annealing	↑ condensation & ↓ hydroxide	2.4	125	270	[191]
ZnO	ammine-hydroxo	microwave-assisted anneal	↓ hydroxide & ↑ crystallinity	1.75	140	30	[198]
ZnO	ammine-hydroxo	annealing in flowing N_2	high-reactivity of precursor	0.4	150	120	[183]
IZO	nitrate	HNO_3 catalyst + vacuum anneal.	↑ hydrolysis & ↓ impurity	~3.4	200	180	[199]
In_2O_3	nitrate	spray pyrolysis combustion	↓ porosity	1.44	200	< 10	[104]
IZO	nitrate	high-pressure NO_2 annealing	↓ impurity & ↑ crystallinity	1.0	200	60	[200]
In_2O_3	nitrate	local heating via combustion	↓ impurity	~0.81	200	30	[86]
IZO	nitrate	high-pressure O_2 annealing	↓ impurity & ↑ density	2.43	220	N/A	[201]
IGZO	nitrate	high-pressure O_2 annealing	↓ impurity & ↑ density	1.81	220	N/A	[201]
ZTO	nitrate/ chloride	high-pressure O_2 annealing	↓ impurity & ↑ density	0.85	220	N/A	[201]
IBZO	alkoxide	controlled hydrolysis + UV	↑ hydrolysis & ↓ impurity	~4	225	N/A	[175]
IZO	nitrate	spray pyrolysis combustion	↓ porosity	0.52	225	< 10	[104]
ZTO	nitrate	local heating via combustion	↓ impurity	~0.4	225	30	[86]
IGZO	nitrate	spray pyrolysis combustion	↓ porosity	0.18	225	< 10	[104]
IZO	alkoxide	controlled hydrolysis	↑ hydrolysis & ↓ impurity	~10	230	120	[84]
IZO	acetate	microwave post-annealing	↓ impurity	6.9	230	N/A	[202]
In_2O_3	halide	O_2/O_3 annealing	↓ hydroxide & ↑ V_o	~1	230	120	[190]

Novel low-T annealing methods have been developed to allow the precursor-to-metal-oxide conversion of the metal salt precursors below the T_{max} of the common, low-cost flexible substrates. These are summarized in Table 4 for MO TFTs where the annealing is performed at $T_{ann} \leq 230$ °C. The first group contains chemical methods where the constituents of the precursor solution are tailored for high reactivity,[183], [197] or to enhance the condensation process and to reduce the remnant $\mathrm{M\text{-}OH}$ content, for example, via the use of controlled hydrolysis of alkoxides [84], [175] or via the addition of condensation catalysts [199]. Also, by combining organic fuels and nitrates as oxidizers, exothermic combustion reactions are expected to lead to high local temperatures for the conversion of various MO semiconductors at low external thermal input [86], [104]. The second group contains methods where the low-T conversion has been performed using an annealing environment that promotes the MO formation, such as ozone [190], high-pressure [201], [200], or vacuum annealing [191]. In the third group, several methods have been explored where electromagnetic radiation energy, such as laser [196], microwaves [198], [202], [203], pulsed light [204], or UV-light [90], is used in addition to thermal energy to convert the precursors into MO films. The UV-assisted annealing, which is used in this thesis, is discussed in detail in the next section.

4.4.1 UV-assisted Annealing

The UV-assisted annealing method of dielectric MO sol-gel films had already been proposed by Van de Leest and Boyd *et al.* two decades ago using Hg vapor and excimer low-wavelength UV lamps, respectively [205], [206]. Recently, Park *et al.* exploited the approach using deep UV-irradiation (DUV) from low-pressure Hg lamps and achieved precursor-to-metal oxide conversion of IGZO at $T_{ann} \approx 150$ °C for high-performance MO TFTs and circuits on glass and plastic substrates [90].

The energy of UV photons, given by $E = hc/\lambda$, where h is the Planck's constant, c the speed of light and λ the wavelength of the UV photons, is used to break chemical bonds in the precursor film via photodissociation. The rate of the photodissociation reaction is dependent on the absorption cross-section of the molecules and the quantum yield of the dissociation reaction at the UV wavelength used. The bond energy gives a rough estimate of the energy required to dissociate the molecular species, however, the actual minimum energy can be larger as some of the energy is stored in the excited state of the products [207], [208].

Several sources of UV light exist which produce light of different spectra and intensity, which can be utilized to target the dissociation of selected bonds in the precursor film [206]. The most commonly used UV source is a low-pressure Hg lamp that produces DUV peaks at $\lambda = 185$ nm, and $\lambda = 254$ nm with ~10 %, and ~90 % of the optical power, respectively [90]. Through the radiative decomposition of excited unstable gaseous dimers, excimer lamps produce, depending on gas pressure, both intense resonance peaks, such as an Xe_2^* peak at $\lambda = 172$ nm, and UV continuum where λ ranges from 110 up to 350 nm [206]. Molecular deuterium

(D_2) lamps provide UV continuum in the far UV (FUV) range where λ ranges from 115 nm up to 400 nm with a radiant intensity peak at ~ 160 nm [209].

The strategy for the UV-assisted annealing of metal oxide precursors can be either: (i) enhanced impurity removal, for example by the scission of the carbonic species that mostly originate from organic solvents and can hinder the condensation reaction of the precursors [210]–[212], (ii) enhanced condensation via *in situ* radical generation such as hydroxyl radicals (HO^*) [185], [205], [197], [II], [III] or (iii) the creation of strong oxidants such as O_3, oxygen radicals or HO^* from the photodissociation of the surrounding gas molecules [210], [213]. For example, O_3 is generated from O_2 when UV exposure with $\lambda < 200$ nm wavelength is performed in ambient air. Table 5 collects the results obtained in this work and reported in the literature on MO TFTs processed with the UV-assisted annealing where the external thermal input is kept at $T_{ann} \leq 250$ °C. These also contain results where a UV exposure pre-treatment is followed by the thermal annealing at T_{ann}.

Table 5. UV-assisted annealing for solution-processed MO TFTs at $T_{ann} \leq 250$ °C in ascending order of T_{ann}. All results are from devices on an Si/SiO_2 substrate.

SC	Sol-gel type	UV-lamp type and gas atmosphere	Main process mechanism	μ (cm^2/Vs)	T_{ann} (°C)	t_{ann} (min)	Ref.
ZnO	ammine-hydroxo	low-pressure Hg + IR in air	HO^* from hydroxide	~ 1	~ 100	> 120	[197]
In_2O_3	nitrate	D_2 lamp (~ 160 nm) in N_2	photocleavage & HO^* from H_2O	4.3	150	180	[III]
In_2O_3	nitrate	low-pressure Hg in N_2	photocleavage & radical reactions	3.6	~ 150	120	[90]
IGZO	nitrate (aqueous)	low-pressure Hg in N_2	photocleavage & radical reactions	3.0	~ 150	120	[214]
ZnO	ammine-hydroxo	medium-pressure Hg	increased dehydration	2.9	150	3	[215]
IGZO	nitrate/ acetate	low-pressure Hg in N_2	photocleavage & radical reactions	2.3	~ 150	120	[90]
IZO	nitrate/ acetate	low-pressure Hg in N_2	photocleavage & radical reactions	1.2	~ 150	120	[90]
In_2O_3	nitrate	D_2 lamp (~ 160 nm) in N_2	photocleavage & HO^* from H_2O	3.2	180	15	[II]
In_2O_3	nitrate + H_2O_2	low-pressure Hg (pre-treat.)	HO^* from H_2O_2	~ 1.6	240	240	[211]
IZO	nitrate	D_2 lamp (~ 160 nm) in N_2	photocleavage & HO^* from H_2O	3.5	250	30	[II]
IZO	acetyle-acetonate	low-pressure Hg (pre-treat.)	O_3 generation & less C impurities	0.4	250	120	[212]

Metal-nitrate precursors have been shown to provide efficient precursor conversion via the generation of *in situ* radicals during DUV exposure from low-pressure Hg lamps [90], [185]. In **Publication [II]** and **Publication [III]**, the precursor conversion is expected to be catalyzed by HO^* generated by a $\mathrm{D_2}$ lamp that leads to an enhanced rate of the condensation reaction, and to lower T_{ann} and t_{ann} [185], [205]. Several photodissociation routes exist for the *in situ* generation of HO^* from the constituents of the nitrate precursor inks, such as:

- photolysis of $\mathrm{H_2O}$ at $145\ \mathrm{nm} \leq \lambda \leq 185\ \mathrm{nm}$ [208], [216]:
$$\mathrm{H_2O} + h\nu \rightarrow \mathbf{HO^*} + \mathrm{H^*}$$
- photolysis of $\mathrm{NO_3^-}$ in aqueous solution at $\lambda \geq 195\ \mathrm{nm}$ [217], [218]:
$$\mathrm{NO_3^-\,(aq)} + h\nu \rightarrow {}^*\mathrm{NO_2} + \mathrm{O^{*-}} \xrightarrow{\mathrm{H_2O}} {}^*\mathrm{NO_2} + \mathbf{HO^*} + \mathrm{OH^-}$$
- photolysis of 2-ME at $\lambda < 195\ \mathrm{nm}$ [219]:
$$\mathrm{H_3COCH_2CH_2\text{-}OH} + h\nu \rightarrow \mathrm{H_3COCH_2CH_2} + \mathbf{HO^*}$$

The absorption coefficient for $\mathrm{H_2O}$ is heavily dependent on the wavelength. The absorption maxima is observed at $\lambda = 165$ nm, that is close to the intensity maxima of $\mathrm{D_2}$ lamps, whereas the absorption coefficient is several orders of magnitude lower for $\lambda = 185$ nm present in the spectrum of the low-pressure Hg lamps [207], [216]. The processes involved in the photolysis of $\mathrm{NO_3^-}$ in aqueous solutions are complex and the reaction above was detected at quantum yield of ~ 0.04 for $\lambda = 254$ nm wavelength [217], [218]. The remnant organic solvent molecules in the precursor films, such as 2-ME, can also take part in the HO^* generation [219].

Although the source of the radicals is not easily determined, their presence and effect on the precursor conversion process has been confirmed with several indirect measurements. Park *et al*. performed in-depth studies on the UV-assisted annealing process where they show that the radicals formed by DUV light take part in the bond cleavage of the impurities, as confirmed by the evaporating small molecules during the annealing process [185]. In addition, the radicals were observed to rapidly reduce the $\mathrm{M\text{-}OH}$ content in the films, thus indicating enhanced condensation reactions [185].

In **Publication [II]** and in Chapter 6.4, we show that functional IZO and $\mathrm{In_2O_3}$ TFTs could be obtained with short annealing times ($5 - 15$ min) and at $180 - 250$ °C temperature when annealed using combined FUV exposure and thermal annealing (FUV+T). The UV exposure was provided by a $\mathrm{D_2}$ lamp at ~ 160 nm wavelength. Moreover, in **Publication [III]**, we show that $\mathrm{In_2O_3}$ TFTs could be processed at a maximum temperature of 150 °C and on low-cost plastic substrates when the annealing time was prolonged to 180 min.

4.5 Printed Metal Oxide Thin-Film Transistors

The first study utilizing printing techniques for the deposition of MO precursors for TFTs was published in 2007, where Chang *et al*. reported inkjet-printed IZO films for MO TFTs with $\mu \sim 7.4$ cm^2/(Vs) [85]. Ever since, inkjet-printing has been the

most widely exploited printing method for the fabrication of various MO semiconductor films for TFTs: ZnO [183], In_2O_3 [195], [220], [III], [IV], SnO_2 [221], [222], $InGaO$ (IGO) [89], IGZO [223]–[227], ZTO [228]–[232], and $InZnSnO$ (IZTO) [233], [234]. In addition to the precursor route, TFTs based on inkjet-printed ZnO nanowires [235], and on In_2O_3 NPs have been reported [182], [236]. EHD-jet printing has also been used to fabricate TFTs from IZO [140], ZTO [141], and IGZO precursors [142]. The performance of the MO TFTs fabricated with digital printing techniques ranges widely and depends on the chemistry of the ink, the processing conditions and the gate dielectric layer. In broad terms, the methods have been shown to allow a comparable performance to the TFT devices produced with spin-coating methods. In **Publication [III]** and in Chapter 6.4.2, we show that the inkjet-printing process of the precursor solution, In-nitrate in 2-ME, can be stabilized by using ethylene glycol (EG) as a high-boiling point co-solvent. Moreover, the high boiling point of the co-solvent does not hinder the low-*T* processing of the printed In_2O_3 films when an extended duration (180 min) is used for the FUV+T annealing at 150 °C to attain In_2O_3 TFTs with $\mu \approx 4.3$ cm^2/(Vs).

Simple coating processes, which generally enable good thickness-control, have been used for the realization of MO TFTs in conjunction with novel patterning methods. IGZO TFTs obtained from a simple bar coating process on bar-coated Al_2O_3 layers yield mobility of $\mu \sim 5$ cm^2/(Vs) [101]. In the process, the patterning of the semiconductor was performed by defining the non-wetting areas with SAM monolayers that were selectively removed by an O_2 plasma treatment performed through a shadow mask. In a novel method, dubbed as rheology printing, the viscoelastic softening of a semi-solid MO precursor gel is utilized for defining the patterns by thermal-imprinting [237]. By a careful, thickness-dependent design of the imprinting mold, spin-coated MO semiconductors could be patterned for TFTs by using the rheology-printed MO S/D-contacts (e.g. ITO) as a dry-etching mask. The resulting In_2O_3 and IZO TFTs with channel lengths of $L = 0.5$ µm allowed mobility of $\mu \sim 10$ cm^2/(Vs) and $\mu \sim 13$ cm^2/(Vs) on Si substrate, respectively. The hygroscopic properties of aqueous nitrate-based precursors allowed patterning of spin-coated semi-dry IGZO films using a simple tape removal technique and IGZO TFTs with $\mu \approx 2.9$ cm^2/(Vs) were reported [238]. However, all of the novel patterning methods listed here utilize some of the batch-type processing.

Contact-printing processes, such as gravure and flexographic printing, where a printing template is used to directly pattern the printing area have also been used to print MO TFTs. Although the methods can deliver higher throughput than the digital printing techniques, only a couple of reports exist in the literature. Gravure printing has been used to create IGZO TFTs on glass-substrates [126]. In the work, increasing printing pressure was found lead in decreasing R_a and reduced layer porosity, which resulted in improved electrical characteristics. However, even the optimized devices gave a low mobility of $\mu < 1$ cm^2/(Vs), possibly due to the used precursor solution. Dilfer *et al*. performed in-depth studies on flexographic printing of alkoxide precursors where the effect of the printing parameters, such as the pressures (p_{nip} and p_{anilox}), printing speed and transfer volume, were correlated with the electrical performance of the IZO TFTs [129]. However, as a result,

the IZO TFTs flexographic printed on rigid Si-substrates showed lower performance with $\mu \approx 2.4$ cm^2/(Vs) than the spin-coated reference devices with $\mu \approx 4$ cm^2/(Vs) due to more inhomogenous layers obtained with flexographic printing. In **Publication [I]** and in Chapter 6.3, we show, for the first time, that flexographic-printing can be used to print continuous In_2O_3 layers on flexible plastic substrate from the nitrate-precursor route in 2-ME and that the resulting nanocrystalline In_2O_3 TFTs exhibit a high-mobility of $\mu \approx 8$ cm^2/(Vs), thus beyond the current a-Si:H technology.

5. Materials and Experimental Methods

The materials, the device fabrication processes and the characterization methods used in this thesis are reviewed in this chapter.

5.1 Metal Oxide Thin-Film Transistor Fabrication

All the MO TFTs processed in the work are bottom-gate top-contact type and without any passivation layer, if not otherwise specified. Figure 16 shows the main processing steps for the spin-coated TFTs and Figure 17 for the flexographic- and inkjet-printed TFTs. The details of the steps are discussed in the following sections.

Precursor Materials and Ink Preparation for the In_2O_3 Semiconductor Layer

As described earlier, the rationale behind selecting the metal nitrate precursor route consists of air-stability, storage-stability, low precursor-to-metal oxide conversion temperature, and the ready availability of alternative low-T processing methods. Indium nitrate ($In(NO_3)_3{\cdot}xH_2O$) metal salt precursor powders were used without any purification.[23] The indium nitrate was dissolved in 2-ME (99.8%, Sigma Aldrich) in 0.2 M concentration, mixed under heavy stirring at ~75 °C for more than 12 h and filtered using a 0.45 µm pore size filter for obtaining a transparent solution. No coloring of the solution was observed during storage in the dark.

In the work, the indium nitrate precursor solution was used without printability-improving additives such as surfactants or stabilizers. This approach is favored to leave fewer remnant impurities in the semiconductor and at the semiconductor-dielectric interface after the precursor-to-metal-oxide conversion. In **Publication [III]**, the inkjet-printing process was optimized by the addition of ethylene glycol (EG) (99.8 %, Sigma Aldrich) as a co-solvent to the solution. The co-solvent weight-ratio (w_{EG}), the molarity (c), the measured viscosity (ν), and surface tension (γ) of the inks are shown in Table 6.

[23] Obtained from Sigma-Aldrich > 99.9% [II] and I.G. Catalyst Ltd / Epivalence Ltd. 99.99%. [I],[III]-[IV] Also zinc nitrate ($Zn(NO_3)_2{\cdot}6H_2O$, >98%) obtained from Sigma-Aldrich was used in [II] for obtaining the IZO ink, where the component solutions were mixed in 7:3 In:Zn atomic ratio.

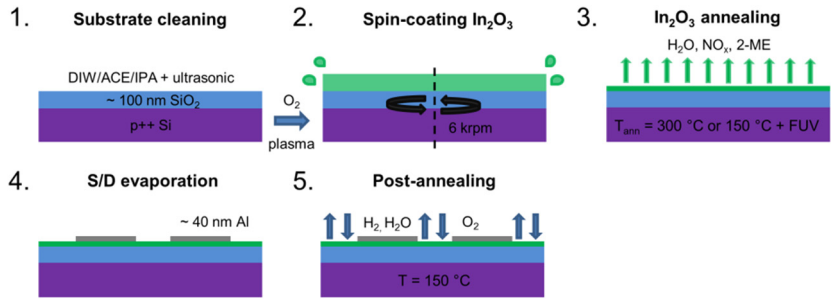

Figure 16. The processing steps for the spin-coated In_2O_3 TFTs on Si/SiO_2 substrate.

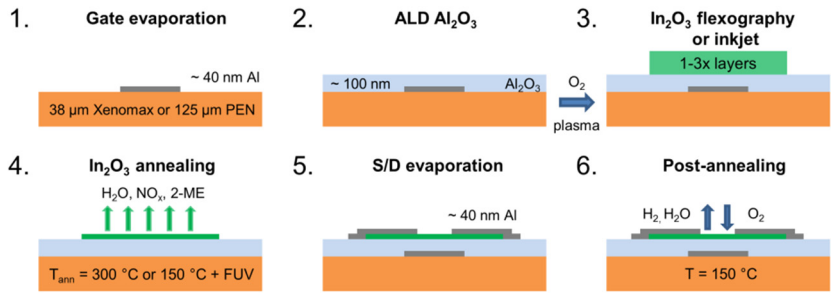

Figure 17. The processing steps for the printed In_2O_3 TFTs on plastic substrate.

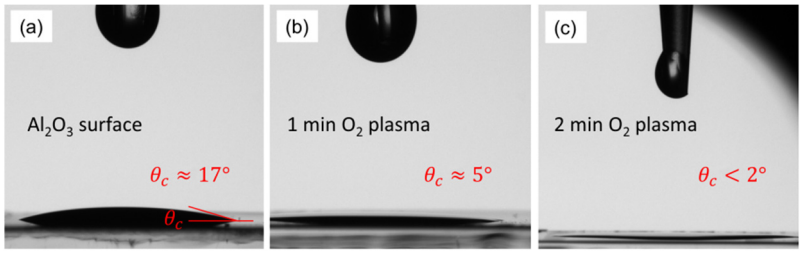

Figure 18. Static contact angle (θ_c) of In_2O_3 ink on ALD-grown Al_2O_3 surface measured with a goniometer (a) for untreated surface, (b) after 1 min O_2 plasma, and (c) after 2 min O_2 plasma pre-treatment. The figure is modified from [I].

Table 6. Characteristics of In_2O_3-precursor inks used in the thesis.

w_{EG} (%)	c (M)	ν (mPa·s)	γ (mN/m)	Publication
0	0.20	~2.4	~31.6	[I],[II],[IV]
10	0.19	~3.7	~32.2	[III]

Substrates, Cleaning, Gate Dielectric, and Substrate Pre-Treatments

Spin-coated and inkjet-printed TFT devices were processed on Si/SiO_2 substrates with a 100 nm thermally oxidized SiO_2 layer as the gate dielectric and p++ doped Si acting as the gate electrode, yielding $C_i \approx 35$ nF/cm^2 [I–IV]. $6''$ wafers were pre-cut into ~ 13 mm x ~ 13 mm chips, which were then cleaned in a sequential bath of ACE/IPA/DIW for > 10 min in an ultrasonic bath and dried with N_2. In addition, spin-coated TFT devices were made on alkaline earth boro-aluminosilicate display glass with low-alkaline content (Corning Eagle) and similarly cleaned [I]. For the flexographic-printed devices, flexible, 38 µm thick PI (Xenomax®, Toyobo Japan) plastic film was used as the substrate [I]. The substrate had a smooth surface and low CTE,[24] which allowed for the use of high temperature annealing without the cracking of the MO or the metal gate layers due to thermally generated stress. Inkjet-printed devices that were annealed with the FUV+T annealing were fabricated on a 125 µm thick PEN (Teonex Q65HA, Dupont Teijin Films) [III].

On the substrates other than Si/SiO_2, ALD-grown Al_2O_3, whose thickness varied from $75 - 120$ nm, was used as the gate dielectric. The Al_2O_3 was grown using a conventional batch process at 300 °C or 150 °C with trimethylaluminum (TMA, $Al_2(CH_3)_6$) and DIW as the precursors [239]. 100 nm thick Al_2O_3, grown at 300 °C, was measured to have a capacitance density of ~ 73 nF/cm^2 and a dielectric constant of ~ 8.3 [I], whereas for the devices on the PEN plastic, the ALD-layer grown at 150 °C had a dielectric constant of ~ 9 [III]. TFTs were processed using a thermally vacuum evaporated bottom gate made of Al or Au, where the top surface of the electrode contributed to the roughness of the Al_2O_3 layer [I].

The MO precursor solutions were deposited after O_2 plasma pre-treatment ($1 - 2$ min, 200 W Diener Nano). The O_2 plasma helped to improve the wetting of the semiconductor ink by decreasing the static contact angle (θ_c) on the receiving surface, as shown in Figure 18 for the In_2O_3 ink on an Al_2O_3 surface. In addition, the polar solvent of the ink can possibly allow improved adhesion between the substrate and the ink after the increased polar component of the γ [91]. θ_c was measured using a goniometer (CAM 200 KSV) and a software-performed Young/Laplace-fitting. The accuracy of the goniometer is limited at $\theta_c < 5°$.

Solution-Processing Methods for the In_2O_3 Semiconductor Layer

A two-step routine was used for the spin-coating of the MO precursors, where a 5 s spreading at 500 rpm was followed by a ~ 45 s step at 6 krpm [I,II] or 8 kprm [III].

Flexographic printing of the precursor solution ($w_{EG} = 0$ wt%) was performed using a RK Flexiproof 100 table-top printing machine that simulates printing in a R2R-environment [I]. Flexographic printing is typically used to create patterns that have µm-range thickness using inks whose η is $50 - 500$ mPa·s [127]. In this work, a thin In_2O_3 semiconductor layer with thickness in the ~ 10 nm range is necessary to attain a satisfactory gate modulation and to avoid bulk leakage in the

[24] Close to the CTE of Si, by manufacturer specifications.

TFT operation. Therefore, the aim was to utilize printing conditions that promote the formation of thin, continuous layers: low solid content of the ink (6.8 wt% of solids), low viscosity of the ink (~ 3 mPa·s), anilox rolls with low transfer volume ($3-5$ ml/m^2), high printing speed (50 m/min), and good wetting due to the high γ obtained through the O_2 plasma pre-treatment. p_{anilox} and p_{nip} were controlled by adjusting the inter-axial distance of the cylinders of the printing unit and the settings were optimized to obtain continuous, homogenous layers on PET test substrates. The layer amount was varied from one to three layers by printing the precursor ink sequentially with ~ 3 s delay between each layer, as shown in Figure 19 (a)–(c). An intermediate drying step was found to lead to poor wetting, as shown in Figure 19 (d).

Inkjet-printing was performed with a Fujifilm Dimatix Materials Printer DMP-2831 with 10 pl nozzles (DMCLCP-11610 cartridge) at 75 µm drop spacing [III]. Inkjet-printing using the pure precursor solution ($w_{EG} = 0$ wt%) resulted in non-optimal droplet formation as shown in Figure 20 (a). In order to improve the repeatability of the inkjet-printing process, the addition of co-solvent (EG) was explored by varying the percentage-by-mass w_{EG} of EG [226]. The addition of EG resulted in clearly improved jetting characteristics, as shown in Figure 20 (a), where the diminishing length of the trailing ligament and the absence of debris in the nozzle plate were accompanied with increased consistency between nozzles and faster nozzle recovery after idle periods. The improvements were driven by the slight increases in the γ and η as well as the lowered P_{eq} of the ink (6 mmHg for 2-ME and 0.06 mmHg for EG). The stability of the printing result was estimated by printing a droplet matrix, as shown in Figure 20 (b)–(d), whose inter-droplet distances and their standard deviation were calculated.

Due to the digital material deposition of inkjet-printing, the average thickness of the In_2O_3 semiconductor layer could be tuned by adjusting the inkjet-printing strategy of the precursor solution ($w_{EG} = 0$ wt%). Two different strategies were followed in this work for varying the average d_s of the In_2O_3 channel: (i) multi-nozzle multilayer printing and (ii) single-layer directional printing using a single nozzle [IV]. For the multi-layer printing, an industrial scale Pixdro LP50 inkjet-printer with 128 nozzles was used with $8-10$ adjacent nozzles at 200 dpi resolution. For the directional, single-nozzle printing, the printing was performed using a Fujifilm Dimatix Materials Printer DMP-2831 with a single 10 pl nozzle.

As shown in Figure 21 (a), a single droplet spreads on the substrate and produces ~ 15 nm thick edges and uniform $\sim 3-5$ nm thick center due to solvent evaporation-induced material flows, i.e. the “coffee-ring” effect [94]. When printing a larger area using a single nozzle and multiple sweeps of the printhead, a striped pattern of alternating peaks and valleys is obtained as shown in Figure 21 (b). The striped pattern could be exploited to control the effective thickness of the In_2O_3 semiconductor by performing the inkjet-printing in parallel ($d_{parallel}$) as in Figure 21 (c), or perpendicular (d_{perp}) as in Figure 21 (d) to the current flow in the channel,[25] where $d_{parallel} \gg d_{perp}$ results.

[25] Current flow in/out of the paper direction or current flow in the left-to-right direction.

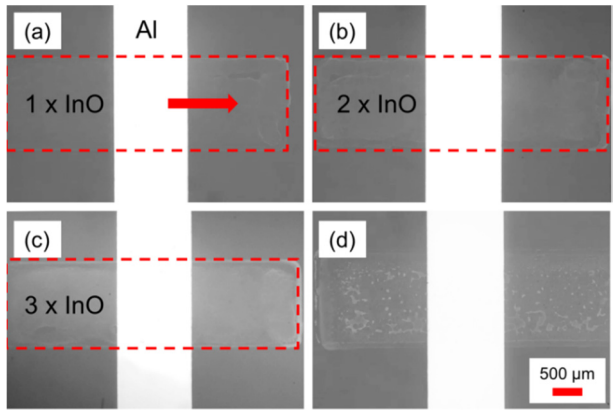

Figure 19. Optical microscopy images of flexographic printing of In_2O_3 ink on top of an ALD-grown Al_2O_3 surface as (a) one, (b) two, and (c) three successive layers. (d) Poor wetting on surface after intermediate drying step at 90 °C. The figure is modified from [I].

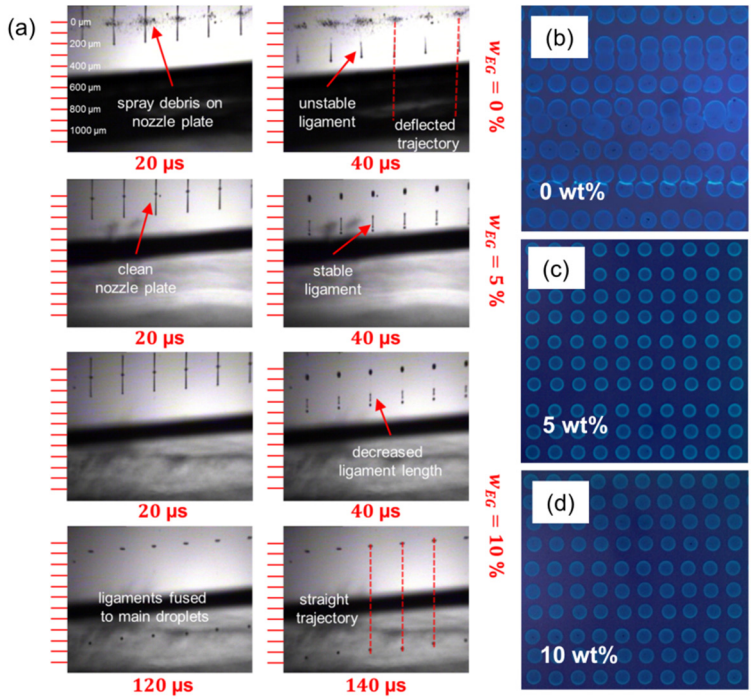

Figure 20. (a) View from the drop-watcher camera view of the droplet formation with varied EG co-solvent contents (w_{EG}) and strobe delays. Optical microscope images of droplet matrix for the assessment of the printing stability for the inks with (b) $w_{EG} = 0$ wt%, (c) $w_{EG} = 5$ wt%, and (d) $w_{EG} = 10$ wt%. Adapted with permission from [III] © 2017 American Chemical Society.

Annealing Methods for the In_2O_3 Semiconductor Layer

Both thermal annealing and FUV+T annealing were used to convert the precursor films to In_2O_3 [I–IV]. The deposited precursor layers were initially dried in air for 15 min at 90 °C. For the thermally annealed devices, the annealing was performed in air on a hot plate for 30 min at 300 °C. The flexible Xenomax substrate was clamped from the edges to allow a good thermal contact with the hot plate [I].

The FUV+T annealing was performed using a deuterium lamp with a MgF_2 window (Hamamatsu L11798) situated on top of a hot plate at ~ 5.5 cm distance. The peak intensity of the lamp was at $\lambda = 160$ nm,[26] and the optical power of the lamp was estimated as ~ 10 mW/cm^2 using a GaP photodiode (Thorlabs FGAP71) at the selected distance. The light intensity was measured to remain nearly constant during a 30 min test run. The annealing setup was fitted inside a N_2 filled glove box (M-Braun MB 200) with low O_2 and H_2O content (~ 1 ppm of H_2O and ~ 10 ppm O_2) to avoid the dissipation of the UV in O_2 and the subsequent O_3 generation that occurs at $\lambda < 240$ nm. The IR component of the light was measured to make a negligible contribution to the sample heating. Reference devices were processed in N_2 without the FUV exposure and also without additional hot plate heating.

Source/Drain-Electrodes, Post-Contact Annealing and Encapsulation

Thermally vacuum evaporated Sn, Cu and Al S/D-electrodes yielded functional In_2O_3 TFTs on Si/SiO_2 substrate, where Al gave the highest μ_{sat} and V_{on} closest to zero as shown in Figure 22, and was therefore selected as the optimal S/D-material. A shadow mask was used to define the S/D-electrodes that had channel dimensions of $W = 1$ mm and either $L = 40$ µm or $L = 80$ µm, yielding W/L-ratio of 25 or 12.5, respectively. Some of the $L = 40$ µm devices had a shadow in the channel and exhibited a persistent negative V_{on} or poor gate modulation [II]. Therefore $L = 80$ µm was used for the rest of the work [I,III,IV].

The as-prepared In_2O_3 TFT devices typically exhibited a negative V_{on} that slowly drifted towards $V_{on} \sim 0$ V during storage. A low-T post-contact annealing step was developed to control the V_{on} of the devices and decrease the device-to-device variation [I-IV]. The physics behind the method are discussed in Section 6.2.

For the encapsulation of the devices against interaction with gaseous molecules, spin-coated SU-8 (SU-8-5, Microchem) was used as an ~ 4 µm thick layer and hard-baked at 200 °C for 30 min. The hard-bake was found necessary to restore the turn-on voltage back to $V_{on} \sim 0$ V.

[26] The light intensity at 160 nm is $\sim 10\times$ higher than in the $120 - 150$ nm range, and $> 50\times$ higher than at > 170 nm, according to the manufacturer specifications: (accessed 18.12.2016)
http://www.hamamatsu.com/resources/pdf/etd/L11798_L11799_TLSZ1014E.pdf

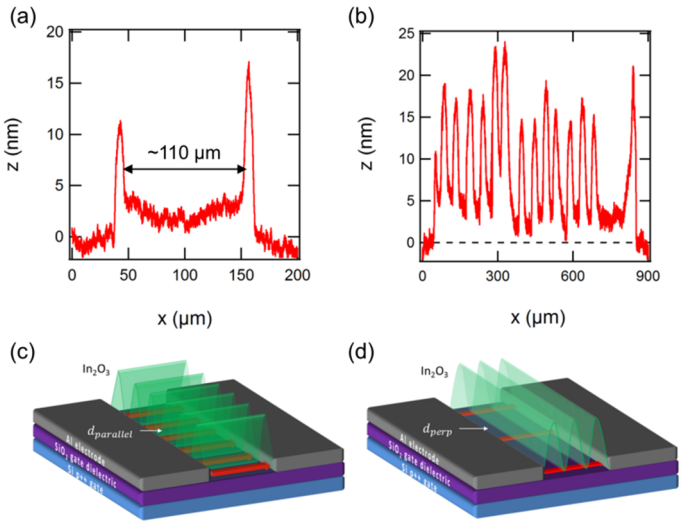

Figure 21. Profilometer scan of inkjet-printed In_2O_3 ink on Si/SiO_2 surface, where (a) a single 10 pl droplet profile is showing a "coffee-ring", and (b) the coffee-ring is utilized in a large area to create a pattern of alternating peaks and valleys. Schematic image of the resulting inkjet-printed In_2O_3 device where (c) peaks are parallel, and (d) perpendicular to the current flow. Figures (b) – (d) are reprinted with permission from [IV] © 2016 IEEE.

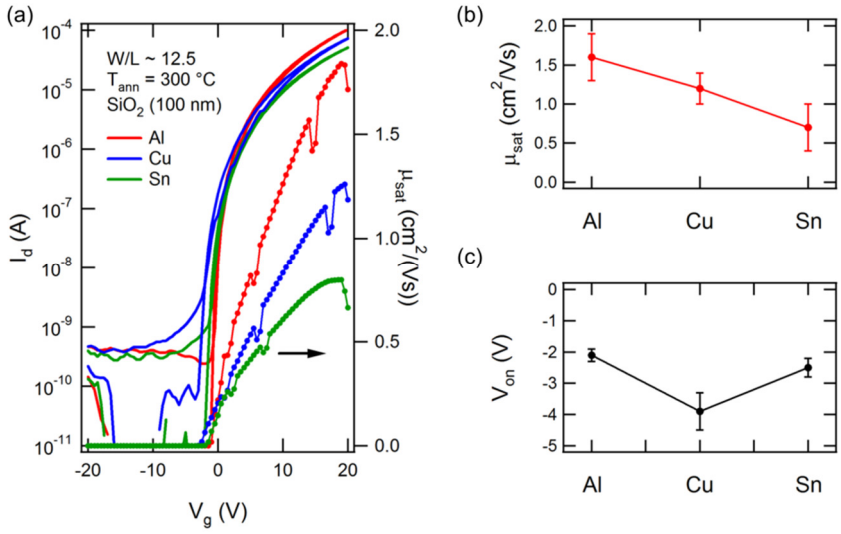

Figure 22. (a) Transfer characteristics of spin-coated In_2O_3 TFTs with varied source/drain-contact metals, where In_2O_3 was patterned with wet etching. (b) μ_{sat} and (c) V_{on} for varied contact metals. The devices with Al were post-annealed at 150 °C in air, whereas the devices with Sn and Cu were not post-annealed.

5.2 Characterization Methods

The In_2O_3 semiconductor layers were characterized using several experimental methods that are discussed in this section. The electrical characterization methods used to measure the TFTs are also summarized.

Semiconductor Layer Characterization Methods

A complete and impurity-free precursor-to-metal oxide conversion is important for the hysteresis-free operation characteristics of the TFTs. The thermal conversion of the dried In_2O_3 ink precursor to MO film was measured for using simultaneous thermogravimetric analysis (TGA), differential thermal analysis (DTA) and mass spectrometry (MS) (Netzsch STA 449 Jupiter® / Netzsch QMS 403C Aëolos) [I].[27] An Al_2O_3 sample cup, a scan rate of 5 °C/min and a dry air environment were used in the measurements. In TGA, the m of the specimen is monitored as a function of T. DTA allows the determination of endothermic and exothermic reactions during the heat ramp. Simultaneous MS spectrum allows the identification of the evaporated reaction products by tracking their mass-to-charge-ratio (m/z).

The information obtained from the thermal analysis can be complemented by probing the vibration modes of the functional groups and inorganic ions present in the film using Fourier transform infrared (FTIR) spectroscopy. The removal of the hydroxyl groups (OH^-) can be detected by looking at the broad $O\text{-}H$ stretching vibration at $\sim 3200 - 3600$ cm^{-1} and the removal of the nitrate ions (NO^{3-}) at the complex peaks at $\sim 1330 - 1470$ cm^{-1}. In this work, attenuated total reflection (ATR) mode FTIR was used to study the In_2O_3 thin films [I,III]. In ATR, the IR light arrives at the sample surface from the probe crystal at an incident angle that is above the angle of total reflection with respect to normal to the sample surface. Only the evanescent field of the light penetrates the sample. Ge-crystal was used in the work as $n_{Ge} \sim 4 > n_{In2O3} \sim 2$ ensures that total reflection occurs in the probe crystal. Harrick Scientific Products Inc. VariGATR grazing angle ATR was installed on Thermo Scientific Nicolet iS50 system measuring at 4 cm^{-1} resolution.

X-ray diffraction spectroscopy (XRD) can be used to probe the crystalline structure of materials by detecting X-ray photons reflected by the atoms of the material arranged as crystal lattices. Thin films are best probed using a grazing incidence XRD (GIXRD) method where a monochromatic, collimated X-ray beam is held at a fixed, low angle of incidence (ω) above the angle of total reflection (θ_c) with respect to the sample surface. The X-ray detector is scanned over a selected range in Bragg angle (2θ) to detect the diffraction peaks. Amorphous materials are free from distinct peaks as they lack a long-range crystalline order. However, distinguishing between amorphous films and films containing nanocrystalline inclusions ($d_{avg} < 5$ nm) is difficult based solely on XRD studies, as the detection of such nanocrystals is dependent on the XRD setup [240]. A complimentary technique

[27] The simultaneous TGA, DTA and MS measurements were performed by Mr. T. Kokkonen at University of Oulu, Finland.

such as high-resolution transmission electron microscopy (TEM) is required to verify the amorphous phase [171]. Cubic, bixbyite-type In_2O_3 yields the most intense (222) peak at $2\theta = 30.6°$ and the second highest (400) peak at $2\theta = 35.5°$. The broadening of the observed diffraction peaks can be used to estimate the average crystallite size (d_{avg}) with the Scherrer formula

$$d_{avg} = \frac{\lambda}{FWHM \cdot \cos\theta}, \tag{16}$$

where λ is the X-ray wavelength, FWHM the full-width at half-maximum of the most intense peak (given in rad), and θ the Bragg angle of the reflection. In this work, a Pananalytical Xpert Pro MRD system was used with $Cu\ K_\alpha$ radiation ($\lambda = 1.5406$ Å) at 40 kV voltage and 40 mA emission current. The GIXRD measurements were performed at $\omega = 0.5°$ angle of incidence in a measurement range of $2\theta = 25 - 50°$ [I,III].

X-rays can also be used to measure the thickness, density, and interface/surface roughness of the thin-films using the X-ray reflectivity (XRR) technique. The sample is subjected to a monochromatic, collimated X-ray beam at low ω and scanned over a small range in ω, e.g. $0° < \omega < 2°$, while having the X-ray detector follow at an angle of $\omega = 2\theta$, as shown in Figure 23 (a).[241] The refracted waves produce a decrease in the reflected portion of the intensity measured by the detector at 2θ. As the refracted waves are then reflected from the variations in the electron density in the internal structure of the sample, such as thin-film surfaces, they interfere with the reflected waves from the top surface and produce an interference pattern (Kiessig fringes), as shown in Figure 23 (b). When considering a single ideal uniform thin-film layer on infinite bulk substrate, one can obtain information on the properties of the thin-film from the interference pattern as depicted on top of the XRR measurement curve of In_2O_3 sample in Figure 23 (b) [241].

XRR has been successfully used to detect the vertical differences in the density of solution-processed MO films, where a thin, high-density crust was observed at the top surface of the films after low-T annealing [242]. Similarly, we used a two-layer model for the In_2O_3 films to simulate the observed XRR curves for extracting the ρ, d and surface roughness of the annealed films, as shown in Figure 23 (c) [III]. The curve fitting was performed using software based on a genetic algorithm by Tiilikainen *et al.* [243].

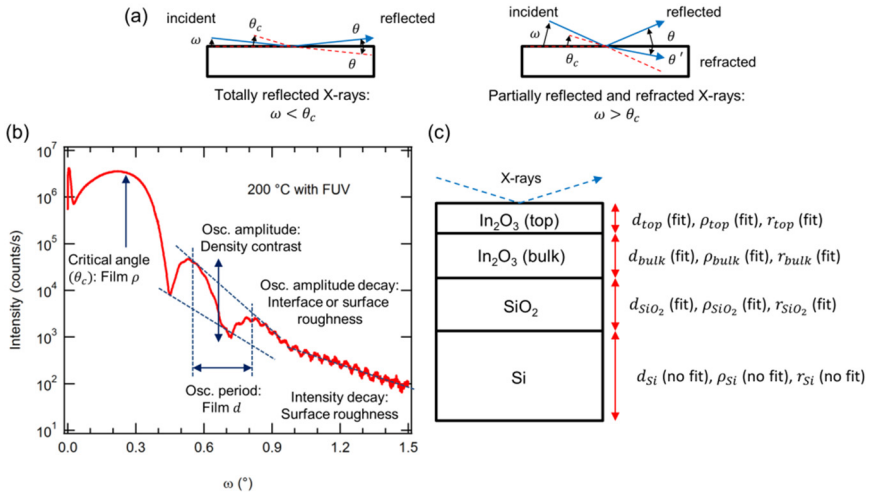

Figure 23. (a) Relevant angles in XRR measurements. (b) XRR measurement of In_2O_3 sample and the effect of various parameters on the Kiessig fringes. (c) Two-layer model used for simulating XRR measurements and fitted parameters. (b) and (c) are adapted with permission from [III] © 2017 American Chemical Society.

A low impurity content (e.g. C and N) and a high degree of M-O-M bonds in the semiconductor films are important for the stable operation characteristics of MO TFTs. The elemental composition and the local chemical environment of the thin films can be studied using X-ray photoelectron spectroscopy (XPS), where the sample is subjected to a beam of monochromatic X-ray photons. When a X-ray photon is absorbed in the material, electrons are knocked off from the inner levels of the atoms (i.e. 1*s*, 2*p* etc.) and they are released with a characteristic energy for each element, which can be used to study the elemental composition of the sample. The characteristic energies are modulated by the local binding environment of the atom, which can be used to detect the changes in the bonding environment, for example by looking at the O1*s* level in MO. The higher electronegativity of H (2.20 Pauling units) than In (1.78 Pauling) or Zn (1.65 Pauling) shifts the O1*s* peak to higher binding energy (BE) in MO films with increasing M-OH content as the oxygen atom becomes less negatively charged. The effect can be used to study the M-OH content in the MOs [87]. The XPS measurements for IZO films were performed using a Perkin-Elmer PHI 5400 spectrometer with a monochromatized Al K_α (1486 eV) source as a survey spectra and high-resolution (0.1 eV) spectrum of C1*s*, In3*d*, O1*s* and Zn2*p* peaks before and after 2 min of sputtering [II].[28]

The interface roughness of the dielectric layer and the semiconductor films can limit the μ by increased charge carrier scattering, as described by Equation (10). Surface roughness (R_a) was measured using atomic force microscopy (AFM)

[28] XPS measurements and peak fitting were performed by J. Dahl, M. Tuominen and P. Laukkanen at University of Turku, Finland.

(Veeco Nanoscope 3) in tapping-mode over a 1 or 10 μm^2 area [I–IV]. After performing a plane fit to exclude tilt and large-scale waviness on the data, the R_a is calculated as the arithmetic average of the height deviations from the mean plane.

The semiconductor and dielectric film thickness (d) were measured using a stylus profilometer (Dektak 150, Veeco Instruments) or AFM [I–IV]. d was measured from the edge of the printed area for the printed In_2O_3 films and over a step, etched using 1 M oxalic acid ($(COOH)_2$), for the spin-coated In_2O_3 films [244]. A UV-releasable dry film resist (Asahi Kasei) was used as the etch mask. For the ALD-grown Al_2O_3 films, a hole was etched in the films using phosphoric acid (85 % H_3PO_4) [III].

Electron microscopy can be used to study the morphology of the samples at the nm-scale. A LEO Zeiss Supra 35 field-emission SEM was used in the work at 3 kV acceleration voltage [I]. A more detailed image of the sample can be obtained using high-resolution cross-sectional TEM analysis, which is capable of producing images of an individual atom and can give information on the crystallinity of the samples. A JEOL 200 TEM was used with 200 kV acceleration voltage [I]. The TEM lamella were prepared using a focused-ion-beam (FIB) FEI Dual-Beam Helios 450 system with 30 kV and 8 kV ion energy for the milling and polishing steps, respectively.[29]

Electrical Characterization of the Thin-Film Transistors

All electrical characterization was performed using a Keithley 4200 SCS semiconductor analyzer and a manual probe-station with Au-plated W probes [I–IV]. The devices were measured in the dark. The noise-floor of the setup was ~ 100 pA, which limited I_{off} and the maximum obtainable I_{on}/I_{off} in some of the TFTs. The data from devices, which were either shorted between the S/D electrodes and the gate, or showed $I_g \sim I_d$, were excluded from the data. Devices that had an appreciable I_g but which did not prevent the reliable extraction of the TFT parameters, however, were included in the data. The transfer-curve at saturation (e.g. $V_d = 20$ V for devices on Si/SiO_2), the output-curve, and, for some devices, also the transfer curve at the linear region ($V_d = 1$ V) were measured. V_{on} was determined and μ_{sat} was calculated with Equation (9) from the saturation current. For obtaining a value for V_t in this work, a linear fit was performed to $I_d^{1/2}$ measured at the saturation regime and the resulting slope was extrapolated to $I_d = 0$. μ_{inc} and μ_{avg} were calculated with Equation (11) from the linear region current by approximating $g_d(V_g) \approx G_d(V_g) = I_d(V_g)/V_d$. In this approximation, $\mu_{inc} = \mu_{FE}$ holds. For the gate-bias-stress stability measurements, a gate field of $+1$ MV/cm or -1 MV/cm was used at low $V_d = 0.2$ V [I].

[29] The cross-sectional TEM measurements and the lamella preparation using the FIB technique were performed by C. Tan at Nanolab Technologies, USA.

6. Results

In this chapter, the results obtained in the thesis are summarized based on **Publications [I–IV]**.

6.1 Thermal Conversion of the In-nitrate Precursor

In_2O_3 semiconductors were fabricated from In-nitrate-based precursors in 2-ME solvent. In **Publication [I]**, $T_{ann} = 300$ °C was selected on the basis of the TGA, DSC, MS and FTIR measurements shown in Figure 24. The TGA signal shows that the mass loss is complete at 300 °C. The simultaneous DSC and MS data indicate that the conversion has two main exothermic peaks at ~ 120 °C and $\sim 260 - 290$ °C, and a third, smaller peak at ~ 200 °C, which all are accompanied by the release of NO_x, 2-ME and H_2O in condensation reactions. These peaks concur with the decomposition scheme presented in the literature for In-nitrate hydrate [245]. The FTIR data confirmed that most of the prominent nitrate (peaks at $\sim 1330 - 1470$ cm^{-1}) and hydroxyl groups (O-H stretching at $\sim 3200 - 3600$ cm^{-1}) were successfully eliminated from the precursor films at 300 °C with only residual trace absorptions left, thus in agreement with other reports [88], [246].

The GIXRD-measurements suggested that the crystallinity of the In_2O_3 started to rise between 200 °C and 250 °C, as indicated by the appearance of the diffraction peak at $\sim 30.6°$. The reference In_2O_3 film annealed at 600 °C shows clear peaks of cubic In_2O_3 (bixbyite) at $\sim 30.6°$ and at $\sim 35.5°$ that correspond to the (222) and (400) reflections, respectively [86], [246]. We obtain, for the films annealed at 300 °C, an average crystallite size of $d_{avg} \approx 6.1$ nm by using the Scherrer formula in Equation (16). This is supported by the TEM images of Figure 24 (e) and (f) from the spin-coated devices on glass annealed with $T_{ann} = 300$ °C, which confirm the presence of nanocrystalline domains with a size of < 10 nm that are embedded in an amorphous In_2O_3 matrix. For the reference device annealed at 600 °C, calculation with Equation (16) yields $d_{avg} \approx 8.5$ nm. This indicates that the d_{avg} of the nanocrystals grows only slightly with further heating, although the nanocrystalline content of the film might increase based on the more distinct peaks in the XRD data [171].

The crystallinity of the MO semiconductor films has been shown to be affected by the layer thickness [172], [192], by dopants that inhibit the onset of crystallinity

[46], [176], and the surface conditions and composition of the underlying dielectric layer [92]. This indicates further room for optimization of the In_2O_3 semiconductor morphology towards more amorphous or crystalline films.

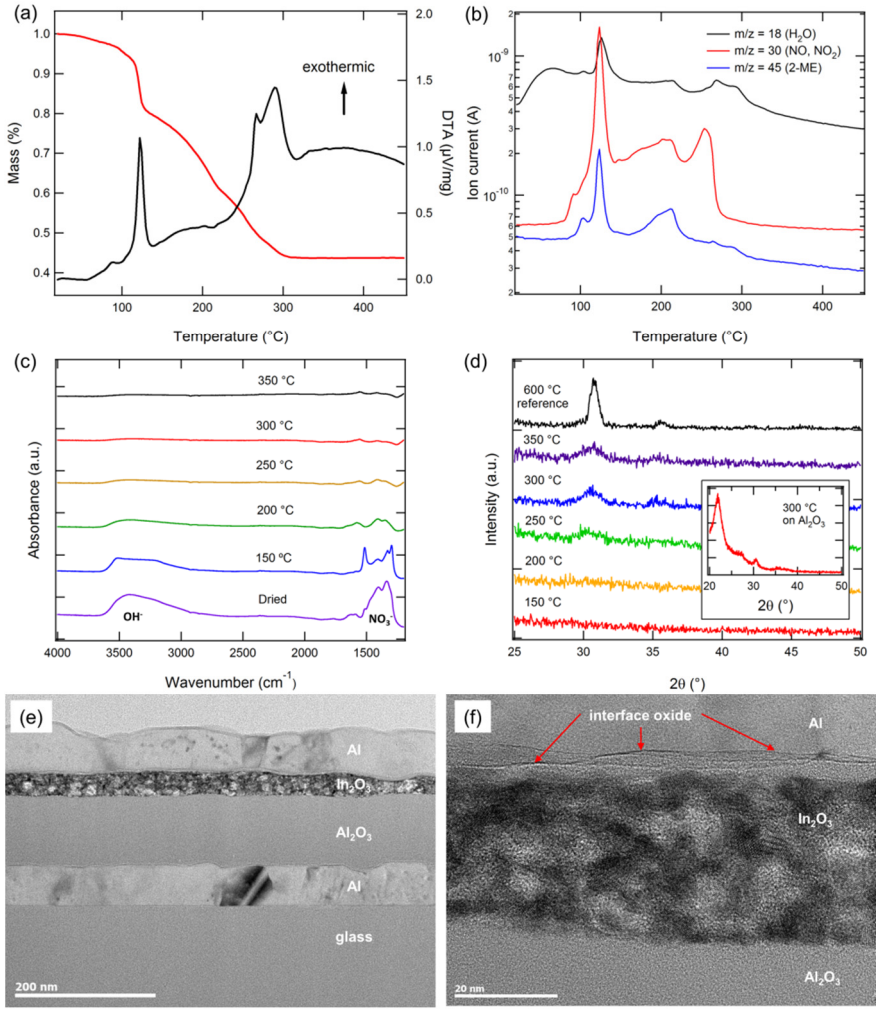

Figure 24. In_2O_3 films annealed on Si/SiO_2 substrate at varied temperatures: (a) TGA/DSC analysis of dried precursors with (b) simultaneous ion current MS signals for H_2O, NO_x and 2-ME. (c) FTIR-spectra and (d) GIXRD-spectra of samples annealed at varied T. The inset shows the In_2O_3 film on the ALD-grown Al_2O_3 surface. (e) TEM image of In_2O_3 TFT device on glass substrate with a 100 nm thick ALD-grown Al_2O_3 dielectric layer. (f) High magnification TEM image of the nanocrystalline In_2O_3 layer underneath the Al-contact electrode with visible interface oxide.[I]

6.2 Post-Annealing for Controlling the Turn-On Voltage

After completing the TFT devices with the Al S/D-electrodes that were thermally evaporated in vacuum,[30] we observed that the In_2O_3 TFTs can exhibit a large spread in the V_{on}, where some devices have $V_{on} < -20$ V, a high SS and an anomalously large μ, thus suggesting an excess in n_e. As the V_{on} of the films was observed to slowly shift during storage in the positive direction towards $V_{on} \sim 0$ V, a post-contact annealing step was developed to accelerate the drift. The low-T annealing in air helped to fix V_{on} close to zero, decrease the device-to-device variation, and stabilize the devices. With the help of the process, thin layers of In_2O_3 could be used as semiconductors in enhancement-mode TFTs. These devices are preferred over depletion-mode devices due to their unipolar operation, as a negative V_g is not required to turn-off the device.

Figure 25 (a) shows the transfer curves of spin-coated In_2O_3 TFTs on Si/SiO_2 substrate that were annealed with $T_{ann} = 300$ °C from **Publication [I]**. The curves are shown both before and after a 30 min long post-contact-annealing step, performed in air at 150 °C. The variation in the μ_{sat} and V_{on} values decreased after the post-annealing, as highlighted by Figure 25 (b) and (c). The In_2O_3 films were, likely due to the low thickness, too resistive both before and after the post-annealing to perform Hall measurements and obtain n_e and μ_H.

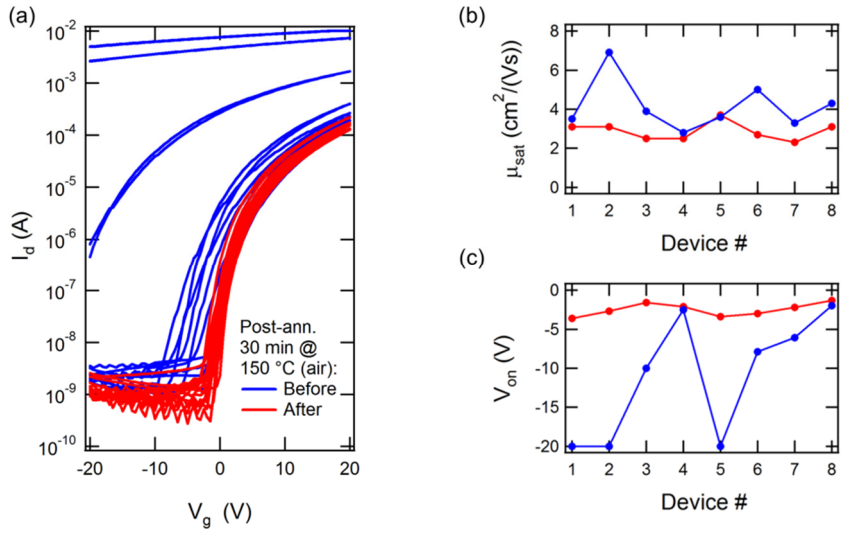

Figure 25. In_2O_3 TFTs ($n_{\#} = 8$) on Si/SiO_2 substrate thermally annealed at 300 °C with Al-electrodes (a) transfer characteristics [I], (b) μ_{sat}, and (c) V_{on} of the devices before and after post-annealing at 150 °C in air.

[30] Typical pressure of the chamber before evaporation is $\sim 5 \cdot 10^{-6}$ mbar.

The mechanisms behind the observed charge carrier generation in vacuum evaporation and the suppression in post-annealing that lead to the observed changes in V_{on} are not fully understood. The two main hypotheses are: (i) the interaction of the back-channel with various gas molecules, and (ii) increased conductivity induced by H_i^+ or V_O. Four possible scenarios that can a have contribution to the changes in the n_e are schematically depicted on top of a TEM image of the In_2O_3 channel in Figure 26. Firstly, unpassivated bottom-gate devices have a host of gas molecules adsorbed on the exposed top surface of the semiconductor layer. O_2 molecules adsorbed on the surface of the channel layer can undergo a partial charge transfer with the semiconductor, e.g. $O_2(g) + e^- \rightarrow O_{2,ads}^-(s)$, that leads to the formation of a depletion region in the channel [160]–[163]. On the other hand, adsorbed H_2O molecules on the top surface are expected to donate a partial negative charge to the semiconductor, and allow the formation of an accumulation layer at the back-channel [160]–[162], [164]. When the semiconductor is exposed to the low-pressure of the evaporation chamber, either some of the initially adsorbed O_2 can be desorbed, and/or H_2O adsorbed,[31] thus resulting in an increase in the n_e. In addition, H_2 gas is generated during the Al evaporation when molten Al reacts with the H_2O molecules present in the vacuum chamber via $2Al + 3H_2O \rightarrow Al_2O_3 + 3H_2$. Hydrogen, which is known to act as a shallow donor (H_i^+) for In_2O_3 [170], can be incorporated in to the In_2O_3 films with the plume of the evaporated Al. Ultimately, changes in the n_e are dictated by the balance of these effects and the observed decrease in the n_e during the post-annealing at 150 °C can result from (i) the excess water being desorbed from the surface and replaced by oxygen, (ii) or H_i^+ being removed from the film by diffusion [247]. Thermal desorption of H_2O and H_2 have been detected during low-T post-contact annealing of thin (~ 25 nm) IGZO with thermally evaporated Al contacts, suggesting a dominating role for H_2O and hydrogen in the process [247].

Another source of the increased n_e are the V_O that could be created during the evaporation in vacuum. After we started adopting the post-annealing to our devices, a report on post-annealing of solution-processed IGZO devices with thermally evaporated Al-contacts was published by Xu *et al.* [248]. They postulated that Al is scavenging oxygen from the IGZO film during the evaporation that leads to formation of V_O, which are then eliminated by the post-annealing at low-T. The oxidation of Al at the interface arises from more negative Gibbs free energy of oxide formation for Al_2O_3 than In_2O_3. For the formation of the interface oxide in metal-MO interface, such as Al-In_2O_3, the direction of the process is determined by

$$\Delta G^\circ = \Delta G^\circ{}_{oxide,1} - \Delta G^\circ{}_{oxide,2}\,, \tag{17}$$

where $\Delta G^\circ{}_{oxide}$ are the Gibbs free energies for oxide formation for both metals [249]. Now, by looking at the oxide formation per mole of O_2 we get

[31] During the last part of the pump-down, adsorbed H_2O molecules are desorbed from all surfaces in the vacuum chamber. Some of the free H_2O could then be re-adsorbed on the exposed sample surface.

$$\frac{4}{3}\mathrm{Al(s)} + \mathrm{O_2(g)} \rightarrow \frac{2}{3}\mathrm{Al_2O_3(s)};\ \Delta G^{\circ}_{Al2O3} = -1054 \text{ kJ/mol}$$
$$\frac{4}{3}\mathrm{In(s)} + \mathrm{O_2(g)} \rightarrow \frac{2}{3}\mathrm{In_2O_3(s)};\ \Delta G^{\circ}_{In2O3} = -553 \text{ kJ/mol.}$$

By the elimination of $\mathrm{O_2}$ from both sides, we get from Equation (17) $\Delta G^{\circ} = \Delta G^{\circ}_{Al2O3} - \Delta G^{\circ}_{In2O3} = -501$ kJ/mol, which indicates that it is thermodynamically favorable for Al to oxidize at the expense of $\mathrm{In_2O_3}$ at the interface. This reaction will create V_{o} in the semiconductor. In fact, the TEM images of the $\mathrm{In_2O_3}$ channel show a thin ~ 1 nm interface oxide below the Al-electrodes, as shown in Figure 24 (f). This hypothesis was further supported by the fact that devices with Cu required no post-anneal to stabilize the device operation as shown in Figure 22. ΔG° for $\mathrm{In_2O_3}$ is clearly more negative than for $\mathrm{Cu_2O}$ and CuO at -232 kJ/mol and -194 kJ/mol, respectively, thus indicating that the reduction of $\mathrm{In_2O_3}$ by Cu is not thermodynamically favored at the interface.[32] In addition to the oxygen scavenging effect, thin layers of $\mathrm{In_2O_3}$ have been proposed to show a relatively low formation entalphy for V_{o} at the surface of the film at the reducing conditions of low pressure [250]. In both cases, the post-annealing in air would bring the film closer to stoichiometric conditions by filling the V_{o} from the oxygen present in the air. Regardless of the exact mechanism, which is still being studied, the developed post-annealing step helps to stabilize the V_{on} of the thin $\mathrm{In_2O_3}$ TFT devices and was used throughout the subsequent work.

The observed changes in the V_{on} highlighted the importance of an encapsulation layer that could prevent the interaction of the gaseous molecules with the back-channel of the semiconductor. Field-induced adsorption/desorption of gas molecules has been identified as the cause of threshold-voltage instability during bias-stress testing [161], [162]. Earlier, solution-processed epoxy-based SU-8 resist has been found optimal for encapsulating sputtered IGZO devices for improved operational stability [46]. Our results, shown in Figure 27, indicate that spin-coated SU-8 encapsulation is also effective in stabilizing printed $\mathrm{In_2O_3}$ TFTs against a shift in turn-on voltage (ΔV_{on}) during gate-bias stress, where unpassivated and SU-8 encapsulated devices experienced ~ 3.9 V and ~ 1.7 V shifts, respectively, when biased at $+1$ MV/cm electric field, although the slight increase in the SS of the encapsulated device (0.5 V/dec to 0.8 V/dec) might lead to the underestimation of the ΔV_{on}. The remaining shift of the SU-8 encapsulated device can be assigned to charge trapping in the channel or in the channel-dielectric interface [251].

[32] However, $\mathrm{Cu_xO}$ can form on the interface from ambient $\mathrm{O_2}$ as was reported for In-Si-O TFTs with Cu-contacts [266].

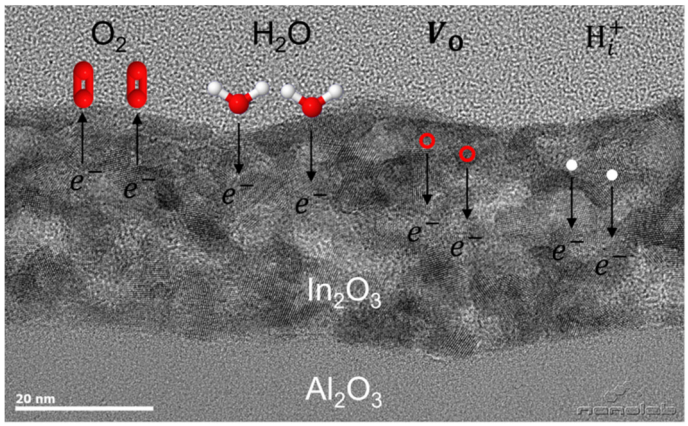

Figure 26. Schematic image of possible charge carrier generation mechanisms after the Al evaporation step: the effects of adsorbed $\mathrm{O_2}$, adsorbed $\mathrm{H_2O}$, generated oxygen vacancies (V_o) and injected hydrogen interstitials (H_i).[33]

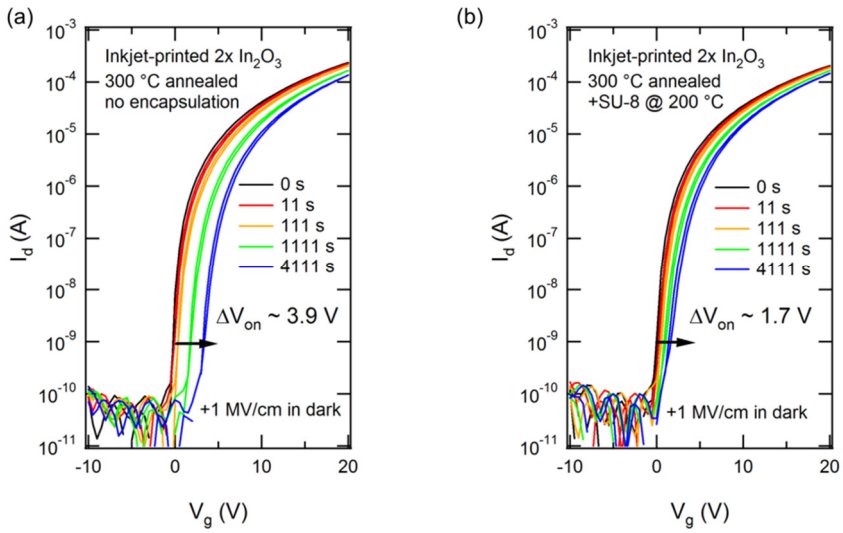

Figure 27. Transfer curves of $\mathrm{In_2O_3}$ TFTs thermally annealed at 300 °C on $\mathrm{Si/SiO_2}$ substrate during positive gate bias stress at $+1$ MV/cm electric field (a) without encapsulation, and (b) with SU-8 encapsulation hard-baked at 200 °C.

[33] The TEM image was taken by C. Tan at Nanolab Technologies, USA.

6.3 Flexographic-Printed In_2O_3 Thin-Film Transistors on Plastic Substrate

In **Publication [I]**, we show that flexographic printing allows the of use additive-free precursor inks without co-solvents, which are typically employed in the stabilization of the droplet formation in inkjet printing of MO precursors. The additives and co-solvents improve the printing stability, but can also participate in the precursor decomposition process [226]. The printing of such additive-free In-nitrate precursors was successfully performed on plastic-substrate with an ALD-grown Al_2O_3 dielectric and metal gate. As described in Section 5.1, the selected printing parameters and the O_2 plasma treatment helped to establish the printing of thin, uniform layers. A plastic substrate with high $T_{max}$and low CTE enabled the use of a high annealing temperature of 300 °C.

The electrical properties of the flexographic-printed nanocrystalline In_2O_3 TFTs were studied in terms of d_{In2O3} by increasing the layer amount from one to three. Each printed layer increased the d_{In2O3} by $\sim 7-10$ nm. Based on the data shown in Figure 28, the average value of μ_{sat} was found to increase in tandem with the layer amount, but was accompanied by an increase in the device-to-device variation for the devices with three layers. In addition, V_{on} moves slightly towards more negative values with an increasing amount of layers. A similar, reduced μ has been reported earlier for ultra-thin (< 7 nm) sputtered [252], [253], and thin (< 50 nm) inkjet-printed a-IGZO films [225]. Moreover, $\sim 5-20$ nm thick polycrystalline In_2O_3 films have also been shown to exhibit a strongly d-dependent μ, where μ increases in tandem with d [188]. The observed increase in μ can arise from (i) discontinuity of the In_2O_3 layer in the thinnest, single-layer devices,[34] and (ii) the vicinity of the back-channel interface that, with decreasing d, results in enhanced surface scattering and acceptor-like traps [252], [253]. Although the TFTs operate in the trap-limited regime based on the gradually increasing μ (μ_{inc} calculated in [I]) [46], effects of percolation-type conduction over potential barriers could also be considered [168], [253], where thicker nanocrystalline channels provide more low-potential percolation paths for the charge carriers. As the amount of layers is increased, the variations in d are easily amplified into a large variation in μ. In fact, the devices with three layers have a larger spread in their average thickness. The polycrystalline TFT model by Levinson *et al.*, described in Section 3.2, can qualitatively explain the changes in the V_{on} [165]. Thicker films can have a larger amount of available charges to pre-fill the initially neutral traps at the depletion-regions at the borders of the crystallites in the channel and, therefore, lead to an increase in I_d of the unbiased TFTs (at $V_g = 0$ V). Thus, the trends in μ and V_{on} can be understood to arise from the nanocrystalline nature of the channel.

For the optimization of the TFT fabrication process, we focused on the selection of the gate-electrode metal and the O_2 plasma pre-treatment time. The R_a of the dielectric-semiconductor interface is known to affect the charge carrier scattering

[34] The values for μ_{sat} span several orders of magnitude lower than the shown maximum value for the single layer devices.

and, thus, limit mobility especially when the gate voltage is large enough to draw the channel closer to the interface, as indicated by Equation (10) [159], [254]. ALD-grown Al_2O_3 on top of the substrate exhibited smooth layers with $R_a = 0.37$ nm. However, a high roughness of $R_a = 1.43$ nm was measured for the Al_2O_3 on top of the Al-gate, which clearly indicated that the metal gate-electrode contributed to the R_a of the dielectric-semiconductor interface. As the gate electrode was changed to Au to improve the interface, this resulted in a smoother Al_2O_3 layer with $R_a = 0.66$ nm. As described in Sections 2.1 and 5.1, the O_2 plasma treatment improves the wetting properties of the precursor films. By utilizing an extended 2 min O_2 plasma treatment, the γ of the substrate was increased and the surface possibly contained a higher amount of polar hydroxyl groups that could provide anchoring sites for the precursor ink [92]. For the optimized devices with an Au-gate, two In_2O_3 layers were printed after 2 min of O_2 plasma treatment.[35] The TFT devices exhibited improved properties, as shown in Figure 29, with a high saturation mobility of $\mu_{sat} = 8 \pm 4$ cm^2/(Vs), a turn-on voltage close to zero $V_{on} = -0.6 \pm 0.5$ V, and a small subthreshold swing of $SS = 0.4 \pm 0.1$ V/dec. In comparison, the two layer devices on an Al-gate show $SS = 0.8 \pm 0.3$ V/dec. The interface trap densities of $N_t = 5.9 \times 10^{12}$ cm^{-2} and $N_t = 3.6 \times 10^{12}$ cm^{-2} that were calculated using Equation (8) for the Al-gated and Au-gated devices, respectively, suggested that the lower N_t could act as an enabling factor for the improved μ. In addition μ_{inc}, calculated using Equation (11), peaked for the devices with Au gates at high V_g, which signalled that the operation shifted from the trap filling regime to a regime where the μ was limited by the interface roughness [159].[36]

The operation of the flexography-printed In_2O_3 devices was modeled with both the polycrystalline TFT model of Equation (12) [I], and the power law of Equation (13), as in ref. [2]. Figure 30 shows the I_d calculated using the both models. The Levinson model is only valid for a low-drain-field condition and, thus, could only be used to calculate the transfer curve at the linear region. The grain boundary mobility (μ_{gb}) and the grain boundary trap density (N_t) could be estimated by taking a logarithm from Equation (12) and plotting the measured transfer curve at the linear region as $\ln(I_d/V_g)$ vs. V_g^{-1}. μ_{gb} and N_t could be obtained as the y-axis intercept and slope, respectively, of a linear fit performed to the linear part of the graph at large V_g. Finally, the V_g-dependent μ_{avg} shown in Figure 30 (a) can be calculated with Equation (A22). For the power law, μ_{avg} is calculated first using Equation (11) and then the parameters α and β are obtained by fitting Equation (13) to the obtained μ_{avg} vs. V_g data. I_d is then calculated with Equations (A32) and (A33) at the pre-pinch off and saturation operation regimes, respectively. Both models give reasonably good fits for the linear transfer curve, whereas the transfer current at the saturation region obtained from the power law clearly deviates from the measured current at large V_g.

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[35] Two layers was selected as the optimum layer amount, as the large spread in mobility (over several decades) suggested non-continuous films for one layer and a large variation in thickness was observed for the three layers.

[36] A similar decreasing mobility at high V_g could arise from large contact resistance R_s or R_d. However, the contact area of ~1 mm^2 should provide a low-enough contact resistance.

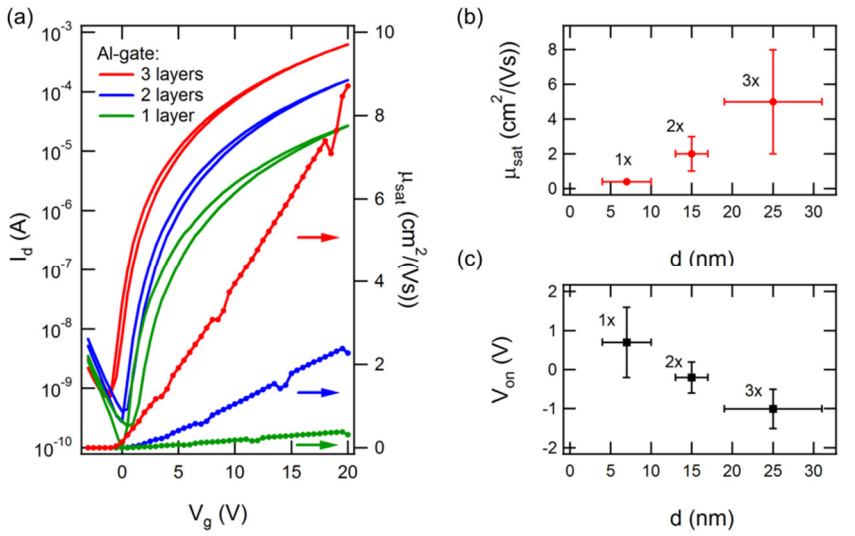

Figure 28. (a) Transfer characteristics of In_2O_3 TFTs on Xenomax PI substrate with a stack of Al-gate electrode, ALD-grown Al_2O_3 (100 nm) gate dielectric, flexographic printed In_2O_3 semiconductor layers with varied layer amounts and evaporated Al S/D contacts [I]. (b) μ_{sat} and (c) V_{on} as a function of device d with $1-3$ In_2O_3 layers. For one layer, the value corresponds to the maximum of μ_{sat}.

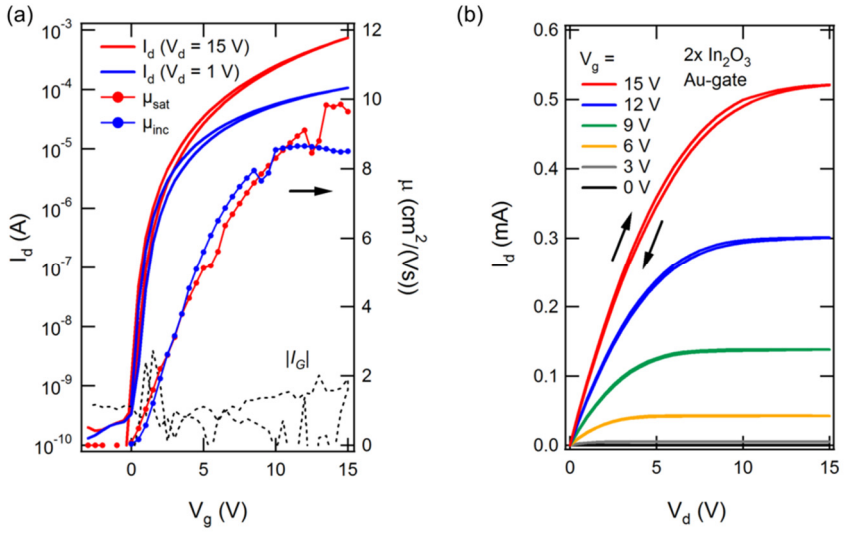

Figure 29. (a) Transfer characteristics of In_2O_3 TFTs on Xenomax PI substrate with a stack of Au-gate electrode, ALD-grown Al_2O_3 (75 nm) gate dielectric, flexographic printed double In_2O_3 semiconductor layers and evaporated Al S/D electrodes. (b) Output characteristics of the device.[I]

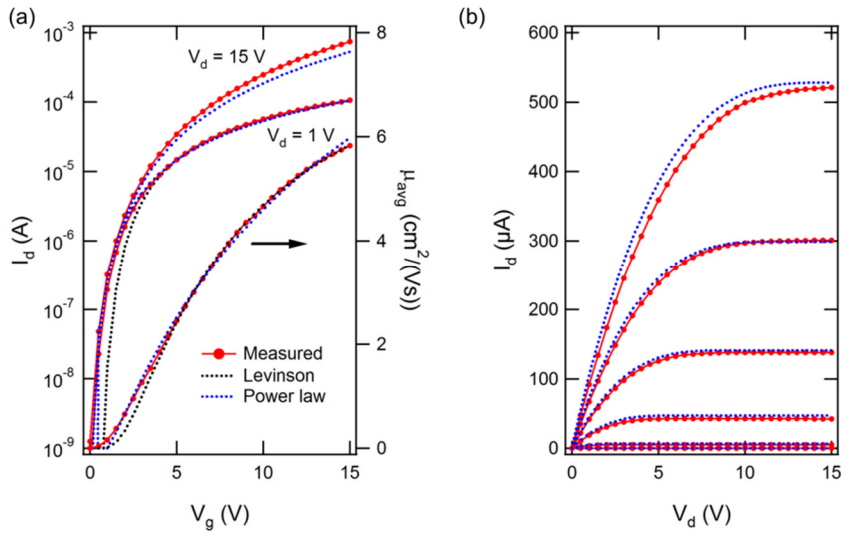

Figure 30. Measured and modeled (a) transfer and (b) output characteristics of In_2O_3 TFT device shown in Figure 29 with the measurement data from [I]. The measured and the modeled μ_{avg} is shown on right axis in (a).

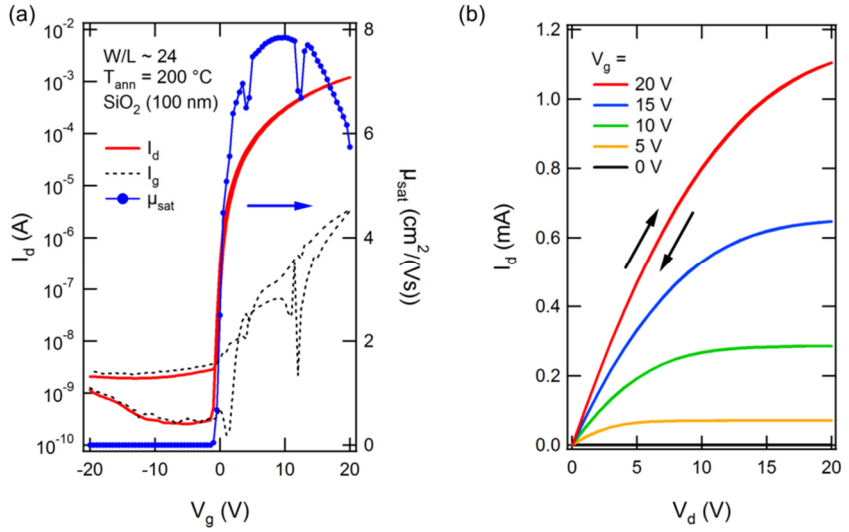

Figure 31. (a) Transfer and (b) output characteristics of spin-coated In_2O_3 TFT device on Si/SiO_2 substrate obtained with FUV+T annealing at 200 °C for $t_{ann} = 15$ min. In (a), the increase in the gate leakage I_g at $V_g > 0\ V$ and the high I_{off} result from the non-patterned semiconductor layer. Adapted from [II] with permission © 2014 AIP Publishing.

Further work to be done on the flexographic printed In_2O_3 TFT devices includes improving the yield as the ALD-grown Al_2O_3 showed a substantial portion of shorted devices. This could be reached by improving the substrate cleanness and the conditions supporting pinhole-free ALD-growth, or alternatively, utilizing printed dielectric layers. More precise control of the thickness of the semiconductor could help to reduce the variation in the μ_{sat}. The use of conductive, preferably amorphous, MO films as the gate electrode could help to lower the R_a of the semiconductor-dielectric interface. The operational instability of the devices, indicated by a shift in the V_{on} during a gate-bias stress, can result from (i) charge trapping in the channel or in the channel-dielectric interface [251], and (ii) from the interaction of the semiconductor with ambient gas molecules. Again, the latter case could be prevented with a suitable encapsulation of the devices [46], [161], [162], such as SU-8 as shown in Figure 27.

6.4 Combined FUV Exposure and Thermal Annealing

The low-cost plastic substrates, such as PET or PEN, cannot tolerate the $T_{ann} = 300$ °C used for the annealing of the flexography-printed In_2O_3 TFTs. After the example set by Kim *et al.* in using DUV exposure for the low-T conversion of sol-gel precursors to high-quality MO films [90], we also started investigating UV-assisted annealing. We focused on low wavelength FUV light at ~ 160 nm as it was expected to induce efficient photolysis of H_2O into elemental hydrogen (H^*) and hydroxyl radicals (HO^*) [207], [216], which are expected to enhance the condensation reactions [205].

6.4.1 Low-Temperature Annealing of Spin-Coated Devices

The combined FUV exposure and thermal annealing was first studied with spin-coated films obtained from the In-nitrate solution in **Publication [II]**. Our results show that the FUV+T annealing both reduces the required external temperature for efficient precursor-to-metal oxide conversion (T_{ann}) and the minimum time required for the processing (t_{ann}) [II]. This could arise from the *in situ* generation of HO^* radicals.

At first, we processed In_2O_3 films using FUT+T annealing at $150 - 200$ °C, and varied the t_{ann}, to study annealing temperatures that are compatible with low-cost plastic substrates. The device, shown in Figure 31 (a), processed at 200 °C for 15 min with FUV+T annealing showed a high, peaking mobility of $\mu_{sat} = 7.5$ cm^2/(Vs) and low $V_{hyst} = 0.4$ V in the transfer curve. These indicated that high-quality films with a low amount of charge traps were obtained with the FUV+T annealing. The output curve of the device in Figure 31 (b) showed current saturation, which indicated that there was no noticeable bulk/surface leakage present. The lowest external temperature attainable for In_2O_3 was 180 °C where a mobility of $\mu_{sat} = 3.2$ cm^2/(Vs) was measured. To study the uniformity of the devices, a set of 16

spin-coated In_2O_3 TFTs was processed with FUV+T at 200 °C for 15 min.[37] The low spread in mobility, $\mu_{sat} = 6.5 \pm 1.5$ cm^2/(Vs), together with the "XRD amorphous" films implied a good film uniformity. However, a high variation in $V_{on} = -5 \pm 4$ V was observed for the set, which could be correlated to the aforementioned shadow in the channel evaporation with $L = 40$ µm. Notably, for the spin-coated devices, μ-values can be heavily overestimated due to fringing currents arising from the non-patterned semiconductor layer [157]. However, $W/L \approx 25$ assures that most of the I_d flows in the channel area. In fact, devices with the In_2O_3 layer patterned via etching show less than $2x$ overestimation of μ_{sat} in the non-patterned state.

The IZO films processed with the FUV+T annealing showed a similar reduced T_{ann} when compared to reference IZO devices, thermally annealed in air at $T_{ann} = 350$ °C, which had $\mu_{sat} = 1.9$ cm^2/(Vs). Functional IZO devices could be obtained at $200 - 250$ °C with the FUV+T annealing, indicating that the temperature can be lowered more than 100 °C. The device annealed at 200 °C using FUV+T shows $\mu_{sat} = 1.3$ cm^2/(Vs), albeit working with a clear hysteresis of $V_{hyst} = 2.0$ V. The increased hysteresis could be assigned to an increased number of charge traps in the channel, which could arise from incomplete precursor conversion or leftover impurities.

The length of the annealing step is a critical parameter for the inline R2R-process. The $t_{ann} = 30$ min used for the thermally annealed devices could be reduced using the FUV+T annealing as functional IZO TFTs with a maximum mobility of $\mu_{sat} = 1.0$ cm^2/(Vs) could be already obtained after $t_{ann} = 5$ min of FUV+T annealing at 250 °C.

XPS-measurements performed on the IZO films indicated that the FUV+T annealing allows efficient precursor-to-metal oxide conversion. The $C1s$ and $N1s$ peaks were not observed in a survey scan measured after sputtering even for the samples that were processed either at low-T (30 min at 150 °C) or for a short time (5 min at 250 °C).[38] The $O1s$ peak deconvolution was performed from high-resolution scans (0.1 eV/step) to study the relative abundance of oxygen in $M\text{-}O$, $M\text{-}OH$ and $M\text{-}V_O$ binding environments for the varied annealing conditions. The data revealed that the largest portion of $M\text{-}O$ bonded oxygen was obtained for film annealed at 200 °C. The degree of $M\text{-}OH$ bonded oxygen increased when the temperature was increased from 200 °C to 250 °C or the time was extended from 5 min to 30 min for the films annealed at 250 °C. As the device properties are strikingly different for the TFT processed at 150 °C for 30 min (inactive) and the TFT annealed at 250 °C for 5 min (working) but they share almost similar $O1s$ peak deconvolution, we expect that additional changes in the MO film, such as the rearrangement of the $M\text{-}O\text{-}M$ network or an increase in the film density, are required to reach a good level of TFT operation.

[37] The spot size of the FUV-lamp was limited such that only 8 devices could be annealed simultaneously with the current shadow mask used for the S/D-evaporation.

[38] Estimated as $< 1\%$ atomic concentration based on the measurement duration and the XPS instrument limit.

6.4.2 Low-Temperature Annealing of Inkjet-Printed Devices

The FUV+T annealing can also be used to lower the processing temperature of printed In_2O_3 devices. Although functional IZO devices were obtained in 5 min process time at 250 °C and In_2O_3 devices in 15 min at 180 °C, both the T_{ann} and t_{ann} are still too high for R2R-processing on low-cost plastics. Based on this, batch processing methods, such as inkjet-printing, were considered better-suited for the FUV+T annealing than flexographic printing, as they allow the prolongment of the t_{ann} to enhance the precursor-to-metal oxide conversion [194].

A stabile and repeatable inkjet-printing process was established in **Publication [III]** using ethylene glycol (EG) as the co-solvent for the In-nitrate precursor solution. As described in Section 5.1, and in Figure 20, the printing stability improved with increasing w_{EG}. For the inks with $w_{EG} \geq 5$ wt%, the Z-value calculated using Equation (2) was lowered to the optimal range of $1 < Z < 10$. The μ_{sat} peaked with $w_{EG} = 5$ wt% for the inkjet-printed In_2O_3 TFTs devices thermally annealed at $T_{ann} = 300$ °C on Si/SiO_2 substrate. After studying the printing stability and the electrical properties of the In_2O_3 films with w_{EG} ranging from 0 wt% to 30 wt%, the EG content of $w_{EG} = 10$ wt% was selected as the optimal composition.

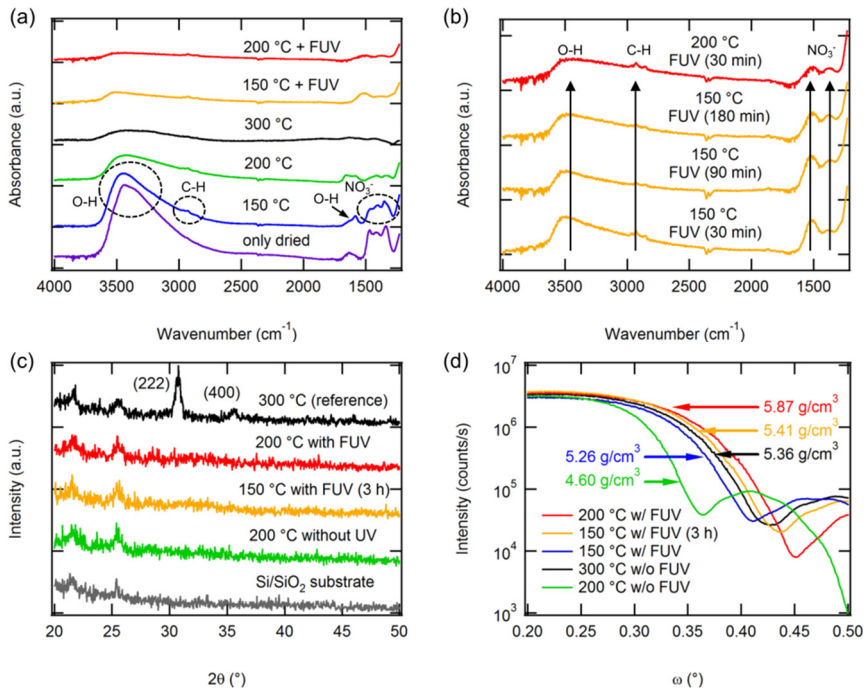

Figure 32. ATR FTIR-measurements (a) for samples thermally annealed or with FUV+T annealing, and (b) for samples processed with FUV+T annealing at $T_{ann} = 150$ °C with varied t_{ann}. (c) GIXRD-spectrum for varied samples. (d) XRR-data near critical angle ($\sim 0.25°$) and the corresponding calculated average ρ. Reprinted with permission from [III] © 2017 American Chemical Society.

The effect of varying T_{ann} and t_{ann} on the FUV+T annealing was studied with samples, which were spin-coated using the optimal ink with $w_{EG} = 10$ wt%. FTIR, GIXRD and XRR measurements were performed on the samples that were subjected to varied annealing conditions with the results shown in Figure 32. From the FTIR measurements in Figure 32 (a) we can see that the FUV exposure at 150 °C and 200 °C temperature removed most of the impurity-related absorptions, whereas for the corresponding samples thermally annealed without the FUV exposure, O-H stretching at $\sim 3200 - 3600$ cm^{-1}, O-H bending at ~ 1620 cm^{-1}, C-H stretching at $\sim 2850 - 3000$ cm^{-1}, and the bonds related to NO_3^- with the complex peaks at $\sim 1330 - 1470$ cm^{-1} were still clearly present. This suggests that the FUV exposure causes the scission of the impurity bonds [185]. Prolonging t_{ann} from 30 min to 180 min at 150 °C temperature led to only minor changes in the FTIR spectrum (Figure 32 (b)). The average density was calculated from the densities obtained from fitting of the two layer In_2O_3 model to the XRR data, as shown in Figure 23 (d). The data showed that the density increased from 5.26 g/cm^3 to 5.41 g/cm^3 when the annealing time was extended from 30 min to 180 min (Figure 32 (d)). The GIXRD spectra, shown in Figure 32 (c), indicated that all the samples were "XRD amorphous" except for the reference sample annealed at 300 °C which showed the (222) and (400) peaks at $\sim 30.6°$ and $\sim 35.5°$ that indicated the presence of nanocrystalline cubic In_2O_3.

Figure 33 shows the results of the electrical characterization of the inkjet-printed In_2O_3 TFTs on Si/SiO_2 substrate. Improvements in the TFT properties, where μ_{sat} increases, V_{hyst} diminishes, and the variation in V_t reduces, were achieved either as T_{ann} was increased during the FUV+T annealing or when t_{ann} was prolonged at constant $T_{ann} = 150$ °C external temperature. These results were supported by the chemical and physical characterization discussed above. The FUV exposure effectively removes impurities (i) that act as charge traps, which were evidenced by the lower V_{hyst} and impurity signals in the FTIR data, and (ii) that limit the M-O-M network formation, which is supported by the increase in the μ_{sat} and ρ. The hysteresis is, however, still considerable as $V_{hyst} \approx 2$ V was measured for the devices annealed at 150 °C for 180 min. The charge trapping can be caused by the remnant impurities seen in the FTIR data (Figure 32 (b)), which could possibly be removed by using a refined annealing process. Our preliminary results allude that V_{hyst} could be effectively diminished using additional vacuum annealing at 150 °C in 0.2 mbar pressure. In addition, the selection of a co-solvent with a lower T_{bp} than that of EG could assist the impurity removal to occur at low-T.

The applicability of the low-T batch process was demonstrated by inkjet-printing the In_2O_3 semiconductor on low-cost, transparent PEN-substrate. The processing temperature is kept at 150 °C for all processing steps: the growth of the 100 nm thick Al_2O_3 gate dielectric using ALD, the FUV+T annealing of the inkjet-printed semiconductor, and the post-contact annealing of the completed devices. The electrical characteristics of a TFT device after a 180 min annealing process are shown in Figure 34, where $\mu_{sat} \sim 1$ cm^2/(Vs) was attained with a low-hysteresis ($V_{hyst} < 1$ V) operation.

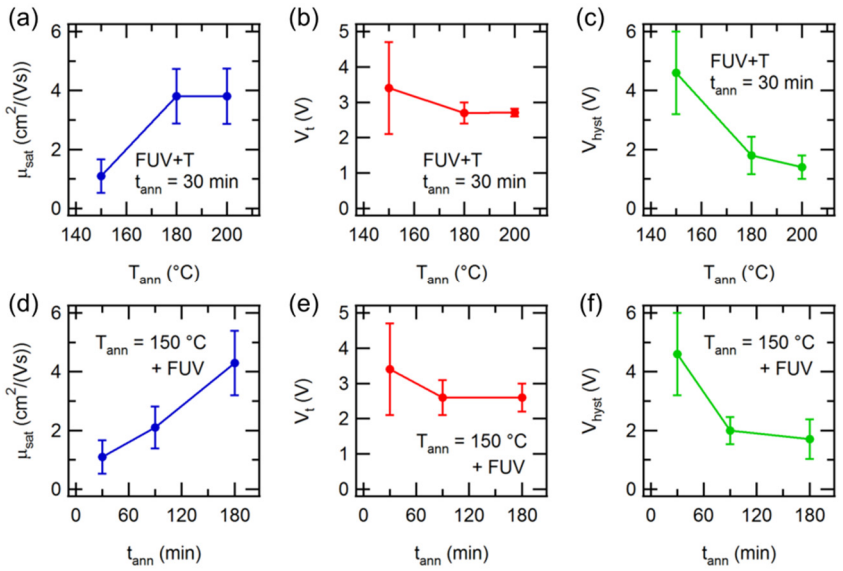

Figure 33. Electrical characteristics measured at saturation ($V_d = 20$ V) of inkjet-printed In_2O_3 TFTs ($n_{\#} = 8$) on Si/SiO_2 substrate with varied annealing conditions using FUV+T annealing. Reprinted with permission from [III] © 2017 American Chemical Society.

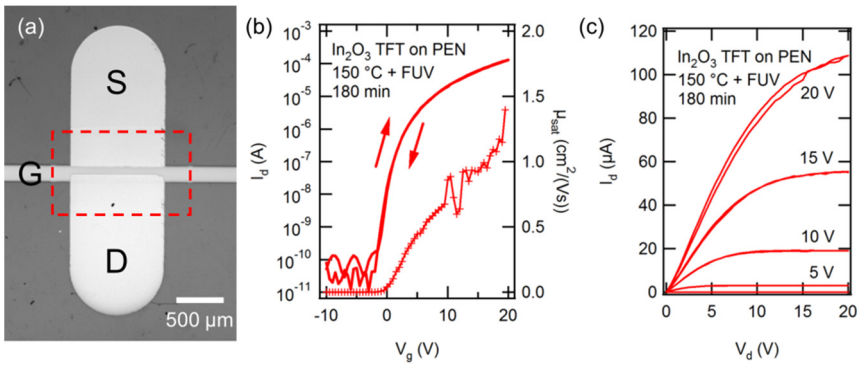

Figure 34. (a) Optical microscope image of In_2O_3 TFT on PEN-substrate where red dashed lines highlight the printed semiconductor area. (b) Transfer characteristics at saturation ($V_d = 20$ V) of inkjet-printed In_2O_3 TFT on PEN-substrate processed at 150 °C temperature using the FUV+T annealing and (c) the corresponding output characteristics. The gate dielectric is ~ 100 nm thick Al_2O_3 grown with ALD at 150 °C. Reprinted with permission from [III] © 2017 American Chemical Society.

As some of the devices on PEN substrate showed, after all the processing steps, cracks in the gate-electrodes improvements in the gate-electrode strain tolerance are required. These could be achieved by using a more ductile metal, such as Cu [255], or conductive MO as the gate electrode. In addition, the thickness of the substrate could be minimized to limit the thermally generated mechanical strain on the device stack [80].

6.5 Towards Circuits and Applications: Depletion-Load nMOS Inverters

For printed and flexible electronics, unipolar circuit elements (nMOS or pMOS) are still of interest as there is an imbalance between the performance of *n*-type and *p*-type semiconductors for both the organic materials as well as for the MO materials. Complementary logic (CMOS) circuits based on all organic materials [74], and the combination of *n*-type MOs with *p*-type organic or CNTs have been recently reported [66], [67]. Such hybrid approaches, however, might lead to difficulties in processing as the fabrication methods and requirements vary for the printed MOs and the organic materials. In addition, the lower μ of the printed organic *p*-type materials compared to that of printed MO *n*-type materials may require a higher footprint for the *p*-type devices.

The performance of unipolar inverters can be improved gain- and speed-wise by using a depletion-mode TFT as the pull-up of the inverter instead of a resistor or an enhancement-mode TFT. This improvement arises from the dynamic load, where both the driver and the load share concurrent high output resistance at the saturation operation. This results in a sharp switching in the voltage-transfer-curve (VTC) as shown in the simulations shown in Figure 35 for *n*-type devices. Conventionally, in Si-based electronics, the depletion-load is generated by local donor ion implantation of the enhancement-devices to change the n_e and the V_T for attaining the depletion operation [256].

Earlier in Section 6.3, we showed that the thickness of the nanocrystalline $\mathrm{In_2O_3}$ semiconductor layer ($d_{In_2O_3}$) affects the μ_{sat} and V_{on} of the devices.[I] By exploiting this effect in **Publication [IV]**, we show that $d_{In_2O_3}$ could be increased further, such that devices operate fully in the depletion-mode ($V_T < 0$ V), where negative V_g is required to deplete the channel from charges and completely turn off the TFT. Conversely, the enhancement-mode ($V_T > 0$ V) operation could be secured by lowering the $d_{In_2O_3}$ [225], [247], [252], [253].

In **Publication [IV]**, we demonstrate that inkjet-printing provides a ready means to control the thickness of the semiconductor by printing a different amount of layers. Figure 36 (a) shows the μ_{sat} of inkjet-printed nanocrystalline $\mathrm{In_2O_3}$ TFTs annealed at $T_{ann} = 300$ °C on $\mathrm{Si/SiO_2}$ substrate with varied layer amounts. μ_{sat} peaks at $d_{In_2O_3} \approx 25$ nm for two layer devices showing $\mu_{sat} = 1.7 \pm 0.3\ \mathrm{cm^2/(Vs)}$ and then rapidly decreases with a further increase of the layer amount. This can be explained by the deteriorating quality of the thicker $\mathrm{In_2O_3}$ films, which is seen as an increase in the layer roughness, as the devices printed with three or more

layers show a substantial R_a (Figure 36 (b)). V_{on} in Figure 36 (c) shifts monotonously towards more negative values and SS in Figure 36 (d) increases in tandem with the $d_{In_2O_3}$. These trends indicate an increase in the charge carrier density n_e of the unbiased devices that is caused by (i) a higher amount of bulk donor traps, such as V_o, that can pre-fill any traps at the depletion regions at the nanocrystalline boundaries [46], [165], [188], and/or (ii) the back-channel moving further away from the semiconductor-dielectric interface which diminishes the effects of the possible back-channel depletion region induced by absorbed O_2 [160], [163], [164].

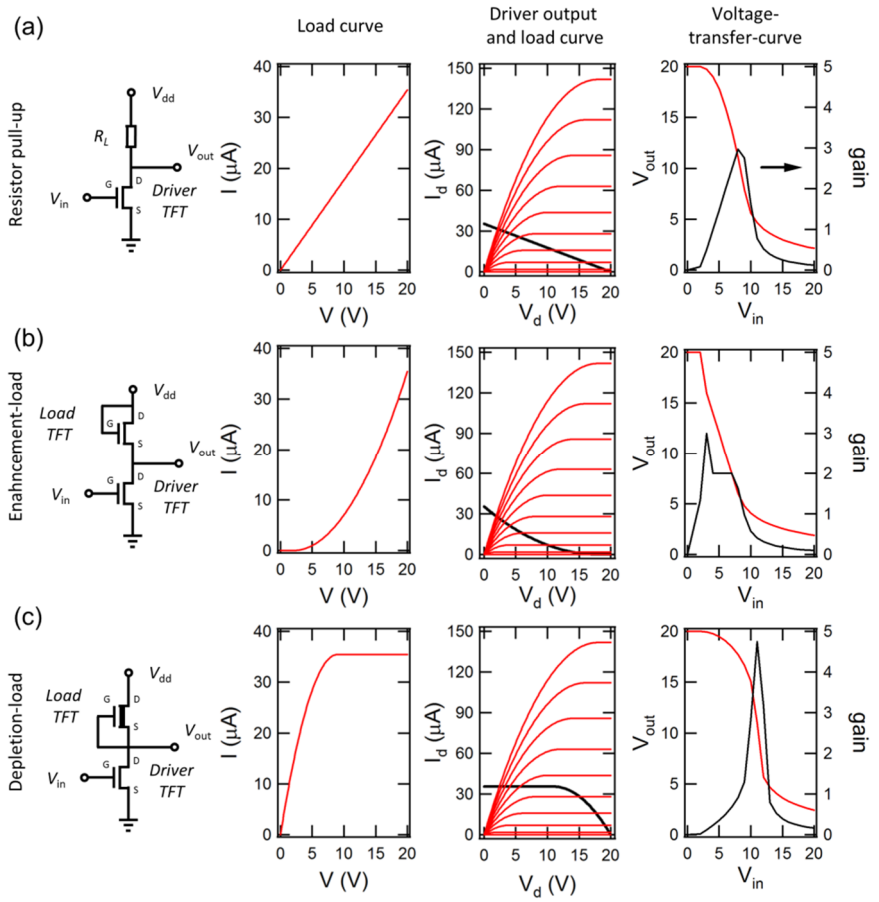

Figure 35. From left to right: Inverter circuit connections, load element IV-curve, load curve imposed on driver TFT output curve, and voltage-transfer-curve (VTC) with calculated gain for (a) resistor pull-up, (b) enhancement-load, and (c) depletion-load inverters. The data is simulated using the ideal square-law model with $C_i = 35$ nF/cm^2, $W/L = 12.5$, $V_t = 2$ V, and $\mu = 2$ cm^2/(Vs) for the driver TFT. For the load element in (a) $R_L = 565$ kΩ, in (b) $V_t = 2$ V, and $\mu = 0.5$ cm^2/(Vs), and in (c) $V_t = -9$ V, and $\mu = 2$ cm^2/(Vs) were used in the simulation.

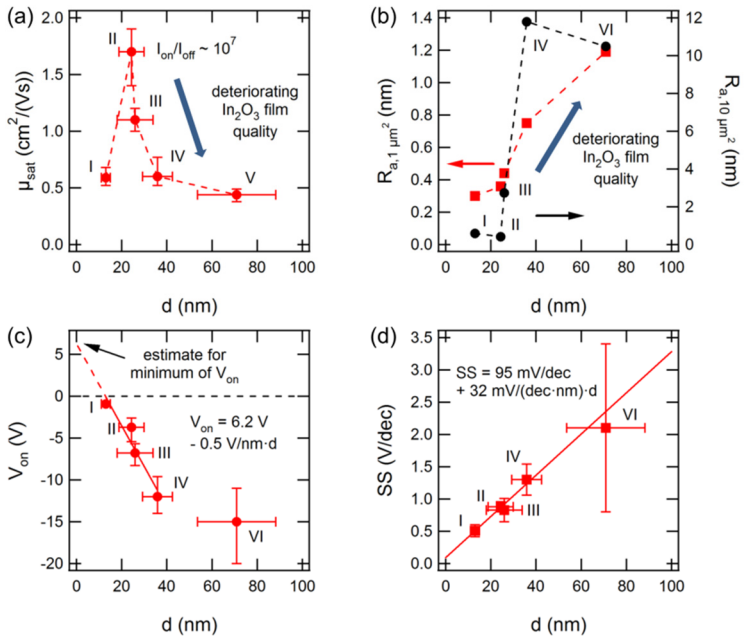

Figure 36. Characteristics for inkjet-printed In_2O_3 TFTs on Si/SiO_2 substrate ($n_{\#} \geq 5$) with one to six layers: (a) μ_{sat}, (b) R_a in 1 µm^2 and 10 µm^2 scan area, (c) V_{on}, and (d) SS. The number of layers is shown with Roman numerals. Reprinted with permission from [IV] © 2016 IEEE.

Another method to tune the effective $d_{In_2O_3}$ was to use directional inkjet-printing with a single nozzle to create the semiconductor area in multiple passes of the printhead, as was presented in Section 5.1. Recalling the schematic image shown in Figure 21, when the printing direction using a single nozzle was either perpendicular or in parallel to the current flow in the channel, a different effective $d_{In_2O_3}$ could be obtained. The different effective thickness leads to different operation characteristics, based on similar considerations to those for the multilayer devices. The devices printed in perpendicular and in parallel to the current flow in the channel operate in enhancement- and in depletion-mode, respectively.

When connecting the multilayer devices as a depletion-load inverter, a VTC exhibiting a sharp switching property and a high gain was demonstrated. Figure 37 (a) shows the transfer characteristics of selected multilayer In_2O_3 TFT devices on Si/SiO_2 and Figure 37 (b) the VTC for the corresponding depletion-load inverter with a gain of ~ 26 at 20 V operation voltage. Similarly, Figure 37 (c) shows the transfer characteristics for In_2O_3 TFT devices fabricated using directional printing on the Xenomax plastic with ALD-grown Al_2O_3 dielectric. Again, by connecting the devices as a depletion load inverter, a high gain of ~ 45 was obtained as shown in Figure 37 (d). The proposed inkjet-printed depletion-load inverters could be used in pre-amplifier circuits, for example, in the signal amplification of printed sensors.

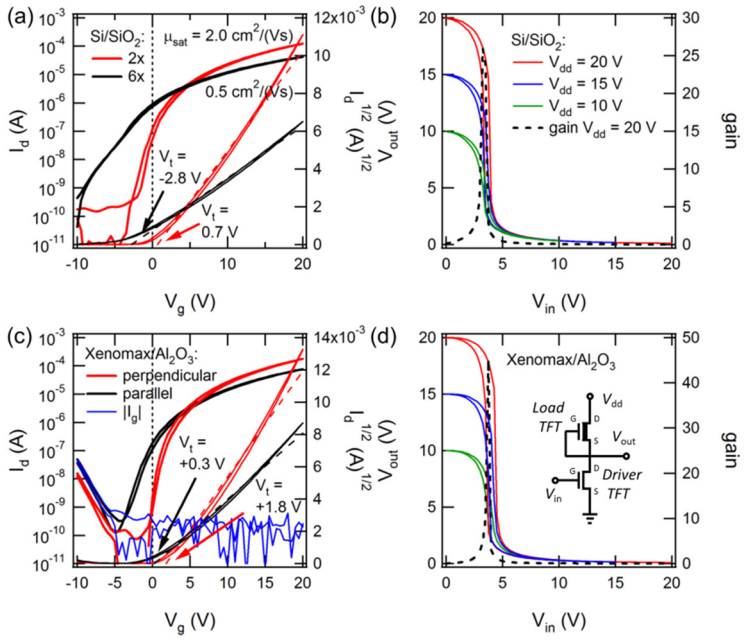

Figure 37. (a) Transfer characteristic of selected In_2O_3 devices inkjet-printed with two layers and six layers of In_2O_3 on Si/SiO_2. (b) VTC for the devices in (a) connected as a depletion-load inverter. (c) Transfer characteristics of In_2O_3 devices inkjet-printed with a single nozzle and multiple sweeps on Xenomax plastic substrate with Al_2O_3 gate dielectric. (d) VTC for the devices in (c) connected as a depletion-load inverter. Reprinted with permission from [IV] © 2016 IEEE.

7. Discussion

In this chapter, the results obtained in this thesis are first compared to the results reported in the literature on printed and low-temperature annealed MO TFTs. Then, the potential applications for printed MO TFTs are studied with a cursory analysis of five different application areas using strength-weakness-opportunities-threats (SWOT) analysis and materials-cost analysis. Finally, some remaining research questions are introduced.

7.1 Comparison of Printed and Low-Temperature Processed Metal Oxide Thin-Film Transistors

In order to see where the results obtained in this thesis stand among the previously published literature, comparisons were made in terms of μ versus T_{ann} graphs for both the different printing techniques utilized in printed MO TFTs and the different low-T annealing processes. In the comparison graphs, we've tried to cover all relevant published work to date focusing, however, on the results obtained through the precursor-route. Problems for obtaining a fair comparison in terms of μ arise from (i) the different assessment methods used in the literature for μ, as also seen in Figure 11 (b) [46], [157], (ii) the transversal electric field dependency, i.e. V_g-dependency, of the μ, which is also dependent on the overvoltage ($|V_{on} - V_g|$ at $V_g > V_{on}$) [46], [157], (iii) the frequency-dependent C_i of the solution-processed dielectrics due to mobile ions [220], [257], residual hydroxyl groups [142], hydrogen hopping [258], or the electron emission from the solution-processed dielectric [259], which can all overestimate the μ, and (iv) non-patterned semiconductors combined with a low W/L-ratio that results in non-negligible fringing currents [157].

In the first comparison graph of Figure 38, printed MO TFTs are collected in a μ versus T_{ann} graph for different MO materials and printing techniques [I], [III], [IV], [85], [89], [101]–[105], [126], [129], [140], [182], [183], [195], [220]–[236], [141], [142], [237], [238]. The results obtained in this thesis, circled on the graph, are among the highest performing MO TFTs obtained on conventional vacuum-processed or thermally oxidized gate dielectrics. The solution-processed dielectrics, shown in the graph as open symbols, can overestimate the device μ due to the above-mentioned reasons. When omitting such results, the maximum μ seems to fall roughly on a line on the semi-log plot, where μ decreases along with T_{ann}.

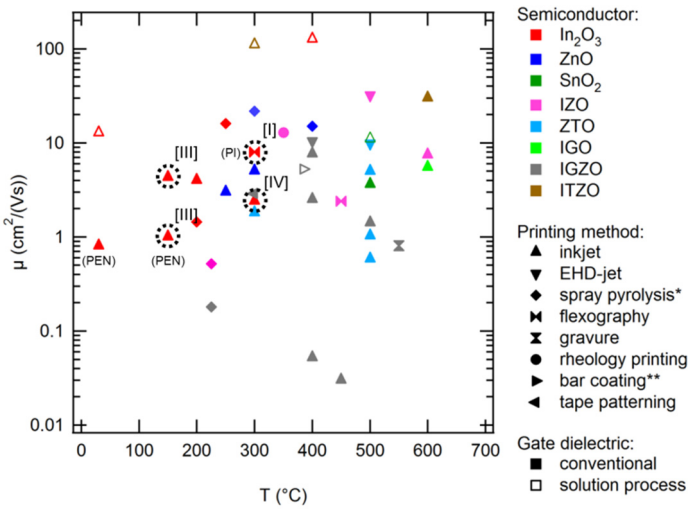

Figure 38. Comparison chart on published printed MO TFTs, where μ is given as a function of T_{ann} for different *n*-type MO semiconductors and printing methods.[39]

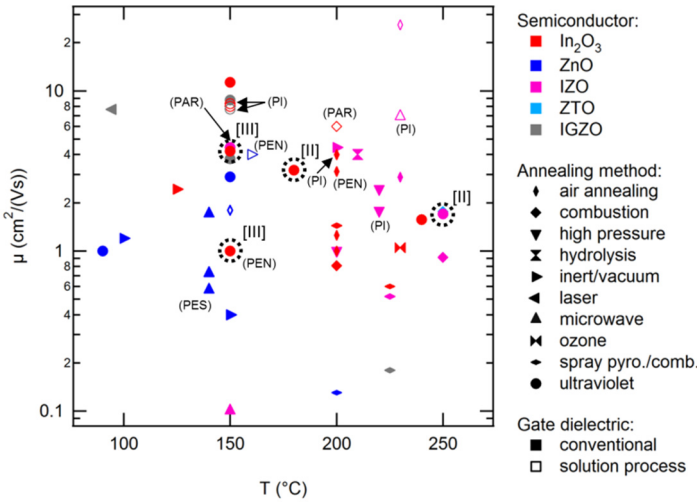

Figure 39. Comparison chart on published low-T annealing methods for MO TFTs where μ is given as a function of T_{ann} for different *n*-type MO semiconductors and annealing methods.

[39] *Spray pyrolysis produces films with high-throughput and low-cost, but requires patterning steps such as conventional wet etching or selective wetting [105]. **Bar coated IGZO layer was patterned using a hydrophobic coating defined by a shadow mask [100].

In the second comparison graph in Figure 39, the low-T annealed MO TFTs are collected in a similar μ versus T_{ann} graph, limited to results with $T_{ann} < 250$ °C [II], [III], [84], [86], [90], [92], [197], [104], [183], [185], [190], [191], [193]–[196], [198], [199], [201], [202], [200], [203], [211], [215].[40] At the processing temperatures compatible with low-cost plastic substrates ($T_{ann} \leq 150$ °C), the binary oxides of ZnO and $\mathrm{In_2O_3}$ appear to be the optimal material when combined with the UV-assisted annealing method.

As a result of the cursory and qualitative meta-analyses, the combination of UV-assisted annealing and a $\mathrm{In_2O_3}$ semiconductor seem to suit the low-T processing of printed MO TFTs, as was also demonstrated with the batch process in **Publication [III]**. Thus far, the printing and annealing steps have been separated and no reports exist combining the printing and low-T annealing processes in-line, which is possible for R2R-processed OTFTs [109]. In fact, the applicability of some of the low-T annealing methods to R2R-processing is limited. The UV-assisted, laser and spray-pyrolysis/combustion annealing methods could be readily utilized in in-line R2R-processing, as they can provide rapid annealing and do not require complicated setups. The minimum speed of the processing line sets the limit for the maximum processing time of an in-line annealing step. In the work, we showed that it is possible with the FUV+T annealing to reduce the t_{ann} below 15 min, albeit with an increase in the device-to-device variation with diminishing time [II]. Rapid annealing has also been obtained using microwave annealing for ZnO TFTs ($t_{ann} < 5$ min)[198], UV-assisted rapid thermal annealing for IZO TFTs ($t_{ann} = 3$ min) [215], spray-combustion for $\mathrm{In_2O_3}$/IZO/IGZO TFTs ($t_{ann} \approx 8$ min) [104], spray-pyrolysis for $\mathrm{In_2O_3}$ ($t_{ann} \approx 10$ min) [103], and laser annealing for IGZO TFTs obtained from the NP route ($t_{ann} = 10$ min) [196]. The fastest conversion has been obtained with pulsed light annealing that is reported to convert the MO precursors into IGZO films in ~ 1 s time, albeit heating the substrate rapidly to ~ 300 °C [204]. The research work on developing in-line-compatible annealing methods that can be demonstrated in a realistic R2R-production environment is still ongoing.

7.2 Applications for Printed Metal Oxide Thin-Film Transistors

The possible applications for printed MO TFTs naturally include the current applications of the conventional vacuum-processed TFTs, such as flexible active-matrix displays [53], [59], and X-ray sensors [62], [63]. In addition to these, printed MO TFTs could be used as sensor elements, where either the semiconductor, electrode or the gate dielectric layers are sensitive to changes in environmental conditions such as pH, adsorbed gas molecules, ambient temperature, or light [65], [260]. Moreover, as the back-channel of non-passivated MO TFTs is sensitive to changes in the electrical charge at the interface, functionalizing the back-channel surface with groups that provide chemical reactions with selected molecules al-

[40] When several results are given in the reference, the results with the lowest T_{ann} are presented for a given set of substrate and gate dielectric.

lows TFTs to be used as sensitive biosensors [60]. Printed MO TFTs can be used in ICs consisting of input/output, logic, memory and sensors, especially when the footprint of the system is not a key factor [260]. Non-volatile re-writable memory elements can be realized from TFTs via a controlled hysteresis loop arising from a ferroelectric gate dielectric [125], [261]. Radio frequency (RF) applications of TFTs include components required in RF identification (RFID) tag technology such as rectifiers for realizing a DC-power supply [68], [69].

A strength-weakness-opportunities-threats (SWOT) analysis for five selected application areas of printed MO TFTs is shown in Figure 40: (i) flexible displays, (ii) biosensors, (iii) active-matrix sensors, (iv) IC, and (v) analog RF-circuits.

Flexible displays have already been widely demonstrated with vacuum processed oxide TFTs, thus highlighting the suitability of MO TFTs in this application [53], [59]. The biggest opportunity lies in the existing market pull for flexible displays, regardless of the manufacturing method. However, the application requires high-electrical performance in terms of mobility and operational stability. Complying even with the lowest level of current ISO standards on malfunctioning pixel density, i.e. < 100 defects per 1 million pixels, can be a tough target. Also, the printing of MO TFTs will not necessary be an any more cost-effective method than the well-established technology of vacuum processed TFTs (a-$\mathrm{Si{:}H}$ or MO).

The strength of the TFT-based biosensor or other chemical sensor application area is that even a single TFT device can be utilized as a sensor element with lesser demands on the μ and device-to-device uniformity than with the other applications. A pre-amplifier circuit for improving the signal-to-noise ratio of a printed sensor is an application where a low number of TFTs, in the order of dozens, can suffice. On the other hand, the readout of the sensor signal will demand more advanced logic functions, which are readily provided by embedded Si-chips with sensor readout and communication capabilities. The biggest opportunity arises from the emerging markets of wearables in sports and health-monitoring applications that could benefit from low-cost, selective biosensors. The largest threats come from other low-cost printed biosensors that can be simpler to fabricate and from the selectivity of the signals, which can be difficult to control as the TFTs can be sensitive to various simultaneous changes in the environment. The SWOT considerations also follow the same reasoning for other types of low-cost TFT sensor applications.

R2R-printed TFTs can be cost-effective in large-area applications with a low packing density, such as in large-area active-matrix sensors, when compared to conventional vacuum-processed TFT technologies or to the hybrid assembly of Si-chips. However, in small dimensions and at high packing density, even the R2R-printed TFTs cannot compete in cost with the conventional vacuum-processed TFTs (see below). The demands on yield are relaxed for the active-matrix sensors as the large sensor arrays can operate even with a small portion of defective TFTs. The opportunity lies in new applications where the flexibility and the large sensor area are of benefit, such as in flexible X-ray sensors [62], [63]. However, the high demands for device-to-device uniformity, especially in terms of V_{on}, and

the operational stability are the weakest points for using the printed MO TFTs in active-matrix sensor applications.

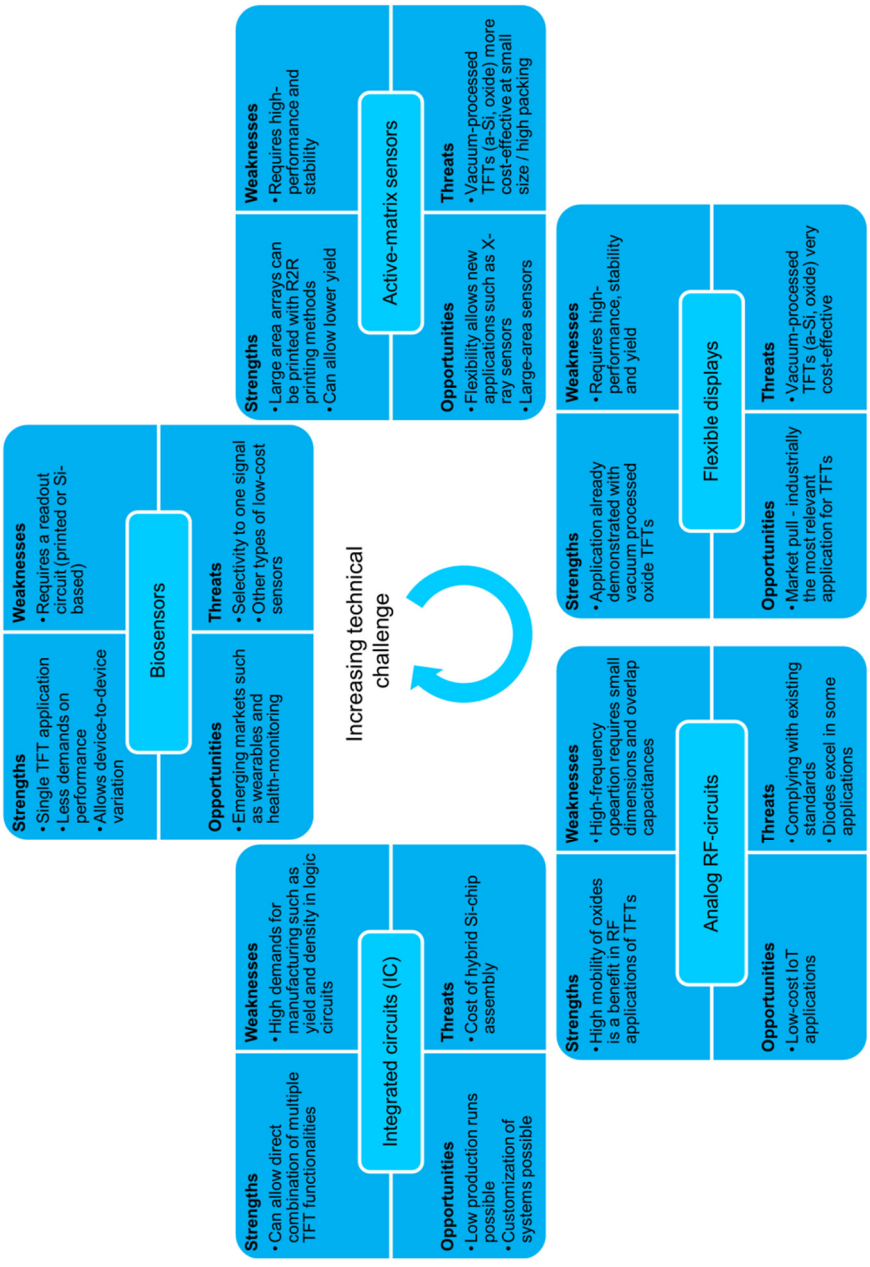

Figure 40. A cursory SWOT analysis of five printed MO TFT applications.

Integrated circuits fabricated with printing technologies can utilize printed MO TFTs in many different functionalities (input/output multiplexing, logic, memory), which makes the application area especially good for low-volume production runs where the cost of a customized Si-chip can be significantly higher than for the low-cost off-the-shelf chips. The high demand for the TFT yield in logic circuits, where a single defective device can cause the whole system to be non-operational, is a stark weakness that will require heavy efforts especially in the process development phase. Therefore, the hybrid Si-chip assembly on flexible substrates is the largest threat for this application case.

The demand for low-cost RF components is apparent with the onset of the Internet-of-Things (IoT), where sensors with communication capabilities are embedded in various objects. The high μ of the MO semiconductors makes MO TFTs suited for some analog RF applications, such as for passive RF rectifiers and for active signal processing tasks [68], [69], which are, mobility-wise, typically beyond the performance limits of OTFTs and a-Si:H. However, based on the unity-gain frequency of Equation (13), not only the mobility, but also the gate capacitance consisting of the channel and the overlap capacitances, limit the maximum operation frequency of the TFTs. In this scenario, with the current registration accuracy of the printing processes, the overlap capacitances are easily comparable to or even larger than the channel capacitance, and therefore pose a serious challenge to this application case. This can be overcome by advanced processing techniques such as the self-alignment of the S/D electrodes [262]. However, Schottky-diodes utilizing the same semiconductor materials can easily reach a higher operation frequency than TFTs [71]. Complying with the existing standards poses the largest challenge for using the printed circuits in active RF communication.

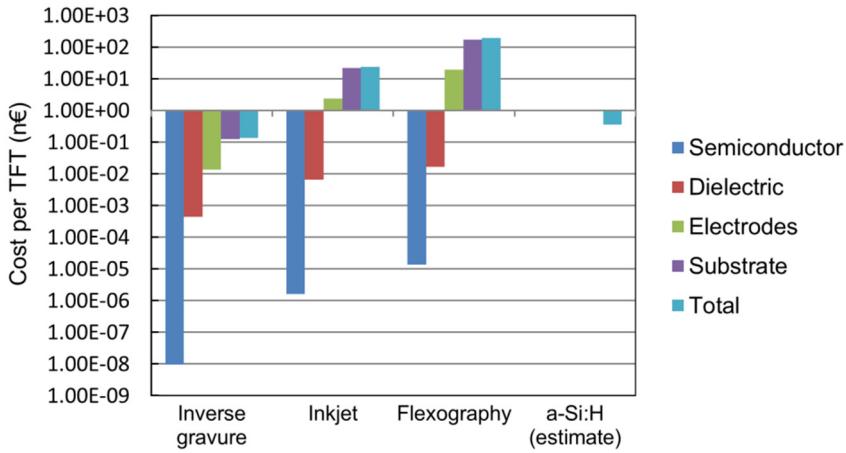

Figure 41. The results of the materials cost analysis of fully printed In_2O_3 TFTs on PEN substrate with various printing techniques for the semiconductor layer.

7.2.1 Cost Analysis for Printed In_2O_3 Thin-Film Transistors

The manufacturing cost of the printed MO TFTs is relevant to many of the aforementioned applications. By using an old cost estimate of 0.4 n$ per a-$Si:H$ TFT[41] as a reference [15], the materials cost of printed MO TFTs can be compared to the cost of the a-$Si:H$ devices obtained using conventional vacuum-processing technology. Most likely, the current price of a-$Si:H$ is significantly lower due to the improvements in the process during the last decade [260]. Also the cost of sputtered MO TFTs is expected to be at similar level to a-$Si:H$ due to the similarly of the processes, such as the same minimum mask amount for the device fabrication via photolithography [53].

In our cursory cost analysis, we focus only on the material cost of the all-printed MO TFTs and consider only In_2O_3 as the semiconductor,[42] Al_2O_3 as the gate dielectric, Cu as the metal electrodes, and PEN as the substrate.[43] We can see how the device size affects the cost by comparing different printing techniques, such as inverse gravure, inkjet, and flexography printing with typical minimum linewidths of 2 µm, 30 µm, and 75 µm that yield 4 µm^2 (square), ~ 700 µm^2 (circular), and ~ 5600 µm^2 (square) minimum area for the semiconductor, respectively. For the contact electrodes, we have assumed a printing technique capable of forming 3 µm wide lines, such as SIJ, inverse gravure or reverse offset, with the length of metal wirings being $15x$ the minimum linewidth of the semiconductor layer. d of the semiconductor, the dielectric, and the electrode layers were fixed at 15 nm, 50 nm, and 60 nm, respectively. For the printed and cured material, a density of $80\,\%$ of the bulk materials was assumed. The device size was estimated by assuming an equal empty space as the semiconductor area in all directions around the semiconductor. The semiconductor then takes up $1/9 \approx 11$ % of the total TFT device area. In this analysis, we have omitted several important factors, such as the capital costs and the printing speed, which will affect the overall cost but are difficult to estimate in a real scenario. In addition, the analysis considers only the ink that ends up on the substrate.

The results of the cost analysis are shown Figure 41. The substrate cost clearly dominates the total cost, indicating that a high packing density and narrow linewidths are critical when a large absolute amount of TFTs is required. In these applications, the cost of printed MO TFT can be comparable to the estimated cost of a-$Si:H$ only when a high-resolution printing method, such as the inverse gravure, is used in the fabrication. However, when a large absolute system area is required, such as in a large-area, sparse active-matrix sensor array, the substrate cost can be omitted from the calculations and also the printing techniques with

[41] Cost estimates of a-$Si:H$ are not freely available. This is from year 2002 in ref. [15].

[42] Typical sputtered IGZO contains approximately $33\,\%$ to $50\,\%$ of In of the metal content of the oxide film.[46], [53]

[43] In_2O_3 from $99.99\,\%$ purity In-nitrate (9.7 €/g, Sigma-Aldrich) as 0.2 M in $99.8\,\%$ pure 2-ME (0.15 €/ml, Sigma-Aldrich), Al_2O_3 from $99.99\,\%$ purity Al-nitrate (4.5 €/g, Sigma-Aldrich) as 0.1 M in 2-ME and Cu from inkjet-printable aqueous CuO nanoparticle formulation of Novacentrix ICI-002 HV (1.8 €/ml). For the PEN substrate, an estimate of 50 €/kg was used with thickness of 50 µm and material density of 1.39 g/cm^3.

higher minimum linewidths, such as flexography, become competitive. The second largest portion of the materials cost comes from the electrodes. Although we used 3 µm linewidth and the price of commercial CuO NP ink instead of Ag NP ink as the electrode material in the calculation, the material cost of the electrodes forms a significant part of the total material cost. However, only if the substrate price was reduced below 5 €/kg for 50 µm thick substrate or 10 €/kg for 25 µm thick substrate would the electrode cost start to dominate. Such low substrate cost could be obtained when using 25 µm thick PET as the substrate material, that would then limit the temperature budget available for the MO annealing to ≤ 150 °C, based on Table 2. The analysis also demonstrates that, from a materials-cost perspective, switching from In-based printed MO semiconductors to In-free materials, such as ZTO, might not be relevant cost-wise as the material cost of the printed MO semiconductor is negligible.

7.3 Suggestions for Further Research

As already shown in Figure 1, and based on the presented cost-analysis in Figure 41, the most critical, unsolved challenge in reaching fully printed MO TFTs on low-cost plastics, lies with the printed metal electrodes. There is a limited availability of metal NP inks suitable for S/D-contacts since the NPs from the optimal low-work function materials such as Al and Ti are highly reactive in $\mathrm{O_2}$ and cannot be used under ambient conditions [83]. One solution is to use printable transparent conducting oxide materials such as ITO or other substitutional-doped $\mathrm{In_2O_3}$-based materials as the contact electrode or, alternatively, as an interface layer between the metal electrodes and the semiconductor [263]. The use of optimal evaporated metals as the S/D electrodes could be reached by patterning of the evaporated metal layers with printed etchants [109], or by using printed sacrificial layers in a lift-off process [144]. Although the TFT device yield is mostly determined by the quality and the pinhole-density of the dielectric layer, we have found that by limiting the S/D to G overlap, the yield of the dielectric could be improved.[44] This in turn would demand high printing resolution and registration accuracy for the patterning of the electrodes.

Several steps in process development are required to upscale the processes developed in this thesis to suit in-line R2R-processing. The low-T annealing in the in-line process requires both realizing annealing in inert conditions and the use of scalable UV lamps capable of *in situ* hydroxyl radical generation, such as $\mathrm{Xe_2^*}$ excimer lamps ($\lambda = 172$ nm). Improving the device-to-device uniformity of the printed MO TFTs requires a stringent thickness control of the printed semiconductor layer, especially if nanocrystalline materials such as $\mathrm{In_2O_3}$ are used. Improved thickness uniformity over a large area could be reached by using novel patterning techniques of R2R-coated films such as the adhesive-tape removal [238], or the

[44] In [I], the yield of operational devices was between $33 - 69$ % with the total overlap area of ~ 1 mm^2. By reducing the width of the gate electrode, the overlap area was lowered to ~ 0.2 mm^2 and, in general, resulted in higher yields for the dielectric [III].

selective wetting by surface energy modification [101]. The inclusion of suitable polymers or metal cations could be utilized to prevent the crystallization of the In_2O_3, which could help in further improving the large area uniformity [176], [177]. The reproducibility of the process requires well-controlled laboratory conditions during the solution-processing as the changing RH can affect the results. The hydrolysis process requires the presence of H_2O but too high a water content ($RH > 50\,\%$) during manufacturing can have a detrimental effect on the transport properties and cause instabilities in MO TFTs, as has been shown for sputtered IGZO TFTs [264].

The biosensor application, where printed MO TFTs are functionalized at the back-channel and the I_d is modulated by the chemical reactions between the analytes and the functionalization [60], [61], could already be exploited using the current printed In_2O_3 TFTs. By using a stable, SU-8 encapsulated TFT as the driver and the functionalized TFT as the load, a depletion-load inverter as presented in this work might find its use in the readout of the biosensor signals.

The critical parameters of the printed MO TFTs are dictated by the potential application. By first selecting the application case, the most relevant parameters could then be optimized with the highest priority.

8. Summary

This thesis focused on developing solutions for the remaining key challenges in the processing of inorganic metal oxide semiconductor layers using printing technologies. In general, the thesis demonstrated that MO materials can be deposited using industrially-relevant printing processes such as flexographic printing and inkjet printing on flexible plastic substrates.

In **Publication [I]** and in Chapter 6.2, we showed that thin In_2O_3 layers can be used as enhancement-mode TFTs when the devices are treated with low-temperature post-contact annealing to stabilize the semiconductor back-channel and/or film stoichiometry. Furthermore, in **Publication [I]** and in Chapter 6.3, we demonstrate, for the first time, that inks based on metal nitrate precursors without additives can be printed with flexographic printing on flexible substrates and the printed precursor layers can be thermally converted to thin nanocrystalline In_2O_3 films, which can be used in MO TFTs whose electrical performance is beyond printed OTFTs or vacuum-processed a-$Si{:}H$ TFTs.

In **Publication [II]** and **Publication [III]**, and in Chapter 6.4, the low-temperature annealing based on combined low-wavelength, far UV exposure and thermal annealing can be used to convert inkjet-printed metal-nitrate precursor films to high-density In_2O_3 layers at 150 °C external temperature for TFTs on low-cost plastic substrates, such as PEN.

The absence of solution-processed *p*-type MO films prevents the use of CMOS-type inverter technology. Moreover, unipolar nMOS inverters exhibit poor gains when only enhancement-type devices are utilized. In **Publication [IV]** and Chapter 6.5, we propose that high-gain inverters can be realized with unipolar nMOS technology by utilizing the thickness-dependent electrical characteristics of In_2O_3 films to create depletion-load inverters using inkjet-printing of the semiconductor.

In Chapter 7.2, we analyzed the possible application areas for printed metal oxide TFTs and performed cursory materials-cost analysis that indicated that only by using high-resolution, additive printing methods, could printed MO TFTs ever compete cost-wise with the current a-$Si{:}H$ TFT technology.

The thesis took only the first steps in the path leading to fully printed MO TFTs on low-cost plastic substrates. Further studies are required in developing printable contact electrode materials for realizing source/drain electrodes that provide Ohmic contact to the MO semiconductors and in developing printable gate dielectrics

that allow a stable capacitance at low frequency. The approaches developed in this thesis, namely the low-temperature annealing and the printing of additive-free metal-nitrate precursors, could be utilized in these tasks.

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Appendix A: Derivation of Thin-Film Transistor Current-Voltage Equations and Operation Frequency

Ideal Square-Law Model

The derivation of the ideal square-law current-voltage equations can be found from various sources, for example by Sze in ref. [156] or Hong *et al.* in ref. [157]. The ideal square-law model for the current-voltage characteristics of TFTs is derived based on the gradual channel approximation, where the electric field E_x along the TFT channel between the source and drain electrodes is assumed to be much smaller than the perpendicular electric field induced by the gate electrode, E_z, i.e. $E_z \gg E_x$. This allows the separation of the two-dimensional electric field into separate perpendicular components E_z and E_x that modulate the charge carrier density and the charge carrier conduction, respectively [156]. The further assumptions for the ideal TFT model are: (i) a constant mobility μ for the channel, (ii) a constant areal gate capacitance, which is given by $C_i = \varepsilon_i \varepsilon_0 / d_i$, where ε_i is the relative permittivity of the gate dielectric, ε_0 the vacuum permittivity and d_i thickness of the dielectric, (iii) Ohmic contacts between the electrodes and the semiconductor, and (iv) an initial charge carrier density n_0 (in cm^{-3}) present in the unbiased device. The initial charge density for enhancement-type devices is $n_0 > 0$ with unfilled traps or acceptor states and for depletion type devices, $n_0 < 0$ with an excess amount of donor states [156].

The voltage supplied to the gate electrode induces a charge carrier density $\Delta n_g(x)$ (in cm^{-3}) in the film that depends on the distance x from the source potential kept at ground. Based on equation $Q = CV$, we can write the gate-induced sheet charge density (in C/cm^2) as

$$Q_g(x) = q d_s \Delta n_g(x) = C_i \big[V_g - V(x)\big], \tag{A1}$$

where q is the elementary charge, d_s the semiconductor thickness and $V(x)$ the drain voltage at distance x. Again, based on $I = V/R = W d \sigma E$, where σ is the conductivity, the drain current I_d of the device is

$$I_d = W d_s \big[\sigma_0 + \Delta\sigma_g(x)\big] E_x \tag{A2}$$

where σ_0 is the initial conductivity and $\Delta\sigma_g(x)$ the incremental conductivity due to the charges induced by the gate voltage. Now, with equation (4) for the conductivity, $\sigma = qn\mu$, and $E_x = dV(x)/dx$,

$$I_d = W d_s \big[q\mu n_0 + q\mu \Delta n_g(x)\big] \frac{dV(x)}{dx} \tag{A3}$$

and with the (A1), further

$$I_d dx = W\mu C_i \left[\frac{qd_s n_0}{C_i} + V_g - V(x)\right] dV(x). \tag{A4}$$

By integrating from 0 to L along the channel,

$$I_d \int_{x=0}^{L} dx = W\mu C_i \int_{V(x)=0}^{V_d} \left[\frac{qd_s n_0}{C_i} + V_g - V(x)\right] dV(x), \tag{A5}$$

which gives the square-law

$$I_d = \frac{W}{L}\mu C_i \left[(V_g - V_t)V_d - \frac{V_d^2}{2}\right], \tag{A6}$$

where the threshold voltage V_t is given by

$$V_t = -\frac{qd_s n_0}{C_i}. \tag{A7}$$

In TFTs, which are majority carrier devices and lack inversion, the threshold corresponds to the formation of accumulation layer.

Equation (A6) is valid in the pre-pinch-off region, where $V_g \geq V_t$ and $0 \leq V_d \leq V_{d,sat} = V_g - V_t$. The saturation voltage $V_{d,sat}$ is obtained from $\partial I_d/\partial V_d = 0$ condition that assumes a constant I_d at the saturation region after the channel pinch-off has occurred at the vicinity of the drain electrode. The saturation region current is obtained from (A6) by setting $V_d = V_{d,sat} = V_g - V_t$

$$I_d = \tfrac{W}{2L}\mu C_i (V_g - V_t)^2, \tag{A8}$$

which holds for $V_d \geq V_g - V_t$.

In the linear or Ohmic regime at low V_D, where $V_d \ll V_g - V_t$, the (A6) can be approximated by neglecting the quadratic V_d-term in parenthesis which yields

$$I_d \approx \tfrac{W}{L}\mu C_i (V_g - V_t)V_d. \tag{A9}$$

The drain conductance at linear region (at low V_d) is obtained from (A6) (or (A9)) and is written as

$$g_d = \frac{\partial I_d}{\partial V_d}\Big|_{V_d \to 0} = \frac{W}{L}\mu C_i (V_g - V_t - V_d)\Big|_{V_d \to 0} = \frac{W}{L}\mu C_i (V_g - V_t), \tag{A10}$$

which leads to the definition of effective mobility, which in this work is written as a function of V_g,

$$\mu_{eff} = \frac{g_d(V_g)}{\frac{W}{L}C_i(V_g - V_t)} = \frac{\frac{\partial I_d(V_g)}{\partial V_d}}{\frac{W}{L}C_i(V_g - V_t)} \tag{A11}$$

that estimates the average mobility of the charge carriers in the channel, but requires the assessment of the threshold voltage.

The transconductance at the linear region is obtained from (A6) (or (A9))

$$g_m = \left.\frac{\partial I_d}{\partial V_g}\right|_{V_d \to 0} = \frac{W}{L}\mu C_i V_d, \tag{A12}$$

which leads to the definition of field-effect or linear mobility as

$$\mu_{FE} = \frac{g_m(V_g)}{\frac{W}{L}C_i V_d} = \frac{\frac{\partial I_d(V_g)}{\partial V_g}}{\frac{W}{L}C_i V_d}. \tag{A13}$$

As both the μ_{eff} and μ_{FE} are obtained at the linear region at low V_d, they are affected by contact resistance between the S/D and the channel. At the saturation region recorded at high V_d, the mobility is written as

$$\mu_{sat} = \frac{\left(\frac{\partial\sqrt{I_d(V_g)}}{\partial V_g}\right)^2}{\frac{W}{2L}C_i}, \tag{A14}$$

which is not affected by contact resistances but is defined at a range where the channel length is reduced by the pinch-off condition and the gradual channel approximation is not valid.

Polycrystalline TFT Model

The model for polycrystalline TFTs was developed by Levinson *et al.* for CdSe and Si TFTs [165] and later by Hossain *et al.* for ZnO TFTs [166]. In the 1D conduction model by Levinson, the polycrystalline semiconductor is assumed to consist of a chain of crystalline grains with a fixed grain size of d_{avg} that give rise to grain boundaries with a sheet concentration N_t (in cm^{-2}) of initially neutral charge traps located at energy E_t with respect to the intrinsic Fermi-level E_i. The traps become negatively charged by electron trapping, i.e. they are acceptor-type traps, as shown in the main text, Figure 12. The semiconductor is assumed to have a uniform, fully ionized shallow donor trap concentration N_d (in cm^{-3}), which are considered as positive traps when empty. In the case of $\mathrm{In_2O_3}$, N_d arises from V_{o}^{n+} or H_i^+ shallow donors [170]. Due to charge neutrality considerations, the occupied acceptor traps (negative) induce a depletion region that arises from the localized ionized donors (positive) at the grain boundaries. The depletion region as acts a potential barrier E_B for the grain-to-grain charge carrier conduction, which then resembles conduction through a thread of back-to-back Schottky barriers.

At low V_d, the carrier conduction is via thermionic emission over barrier height E_B[45] and the current density is given by

[45] When the voltage drop over a single barrier is less than the thermal energy $k_B T \sim 25$ meV: in our case $d_{avg} < 10$ nm and channel length $L = 80$ μm, which indicates 0.125 meV for $V_d = 1$ V.

$$J = A^* T^2 e^{-E_B/k_B T}\left(e^{qV_s/k_B T} - 1\right) \approx A^* T^2 \frac{qV_s}{k_B T} e^{-E_B/k_B T} = \frac{4\pi q m^* k_B^2 T^2}{h^3} \frac{qV_s}{k_B T} e^{-E_B/k_B T} \quad \text{(A15)}$$

where V_s is the portion of V_d voltage over a single grain and $A^* = 4\pi q m^* k_B^2/h^3$ is the Richardson constant, where h is the Planck constant and m^* the effective mass [155], [156]. The inequality of $V_s \ll k_B T$ allows the series expansion of the second exponential function in (A15). Finally, when the Fermi-level is close to CB for non-degenerate semiconductors,[46] the electron density of the CB is $n_0 = 2(2\pi m^* k_B T/h^2)^{3/2}$ [156].This leads to the form presented by Levinson

$$J = q^2 n_0 \left(\frac{k_B T}{2\pi m^*}\right)^{1/2} \frac{V_s}{k_B T} e^{-E_B/k_B T}. \quad \text{(A16)}$$

The shallow donor concentration N_d determines whether the grains are fully depleted or partially depleted. A critical donor density N_d^* can be defined as

$$N_d^* = N_t/d_{avg}. \quad \text{(A17)}$$

In the case the where $N_d < N_d^*$, the grains are fully depleted and the grain boundary traps are assumed to be partially or fully filled. In the case where $N_d > N_d^*$, the grains are partially depleted and the traps are fully filled. For the former case, the conductivity is activated by thermal emission from the traps to the CB, i.e. over the $E_C - E_t$ barrier, such that

$$\sigma \propto e^{-(E_c - E_t)/k_B T}. \quad \text{(A18)}$$

The conduction in the latter case is activated by thermionic emission over the E_B barrier and, based on $J = \sigma V_s/d_{avg}$, the conductivity can be written from (A16) as

$$\sigma = q n_0 \mu_0 e^{-E_B/k_B T}, \quad \text{(A19)}$$

where $\mu_0 = q d_{avg}/(2\pi m^* k_B T)^{1/2}$, n_0 the total charge density and E_B the energy barrier, which is given by

$$E_B = \frac{q^2 N_t^2}{8\varepsilon_{sc}\varepsilon_0 N_d}, \quad \text{(A20)}$$

where ε_{sc} is the relative dielectric constant of the semiconductor.[165] In $N_d > N_d^*$ case with partially depleted grains and fully filled traps, a positive gate voltage induces a sheet carrier concentration in the semiconductor

$$n_g = \frac{C_i V_g}{q}, \quad \text{(A21)}$$

[46] Non-degeneracy is valid when $E_c - E_F > 3k_B T$ and, thus, is not valid for In_2O_3 that is heavily doped.

which can ascribed as an addition to the donor density N_d. Therefore, at positive gate voltages the barrier height E_B of (A20) is effectively reduced by the n_g, which results in increasing conductivity in tandem with an increase in the free charge carrier concentration. The changing conductivity can be associated with either (i) a change in carrier concentration $n = n_o e^{-E_B/k_B T}$ or (ii) a change in effective mobility $\mu = \mu_o e^{-E_B/k_B T}$. When accounting for the scattering events inside the grains by introducing a mobility μ_g, the total mobility can be written with the Matthiessen's rule (Equation (3)) as

$$\mu^{-1} = \mu_g^{-1} + \left(\mu_{gb} e^{-E_B/k_B T}\right)^{-1} \tag{A22}$$

where μ_{gb} is the grain boundary mobility. Typically, the mobility inside the grain is close to the mobility of bulk material and $\mu_g \gg \mu_{gb}$ holds. (A22) can then be written as $\mu \approx \mu_{gb} e^{-E_B/k_B T}$.

At positive V_g, sheet charge of n_g is induced and the total charge density is $n_0 = N_d + n_g/d_s$. Based on $I = JWd$, $J = \sigma V/L$, and (A19), the drain current I_d can be then written as

$$I_d \approx \frac{W}{L} q \mu_{gb} \left(N_d + \frac{n_g}{d_s}\right) d_s V_d e^{-\left(q^2 N_t^2\right)/\left[8\varepsilon_{sc}\varepsilon_0 \left(N_d + n_g/d_s\right) k_B T\right]}, \tag{A23}$$

where the penetration depth of the gate field is assumed to be the semiconductor thickness d_s at all V_g. When the gate voltage is large enough such that $n_g/d_s \gg N_d$ holds,[47] the (A23) can be written with the help of (A21) as

$$I_d \approx \frac{W}{L} \mu_{gb} C_i V_g V_d e^{-\left(q^3 N_t^2 d_s\right)/\left(8\varepsilon_{sc}\varepsilon_0 C_i V_g k_B T\right)}. \tag{A24}$$

The equation indicates that with increasing V_g the current increases due to the charges induced in the channel and the diminishing of the energy barrier, which can also be considered as a gate-dependent mobility.

Power-Law Model

As illustrated in the main text, the gate voltage dependence of the mobility causes deviation of the characteristics of the MO TFTs from those of the ideal model. This is especially important from a circuit design perspective, where robust models with a limited amount of parameters are required. Although the current-voltage characteristics of the nanocrystalline In_2O_3 TFTs might be physically based on the polycrystalline TFT model, the model doesn't provide a viable means to describe the TFT characteristics using parameters that are extracted by simple measurements.

[47] For example with $V_g = 0.5$ V and $C_i = 73$ nF/cm^{-2}, the charge sheet density induced by the gate is $n_g \sim 2 \times 10^{11}$ cm^{-2}. Based on the estimated donor density of $N_d \sim 6 \times 10^{12}$ cm^{-3} obtained using Equation (9) in ref. [165] and the measured off-state leakage current ($V_g = 0$ V) of $I_d \sim 8$ nA at $V_d = 0.5$ V for the 3 layer In_2O_3 TFT with $d_s = 25$ nm presented in [I], we see that $n_g/d_s \gg N_d$ holds even at low gate voltages.

A simple model to account for the gate voltage dependence of a-IGZO TFT mobility was developed by Abe *et al*. which utilizes the existing power law models developed for a-Si:H TFTs [167]. Although the power law model may not be physically motivated, due to possible differences in the sub-gap states between a-IGZO and the nanocrystalline In_2O_3, we have successfully adopted the simple power law model for the gate-dependent mobility to describe the solution processed and printed In_2O_3 TFTs in circuits [2]. The power law model is more straightforward to use than the *n*th-order polynomial model proposed by Hoffmann for poly- and nanocrystalline semiconductors [265].

In the power-law model, the gate voltage dependence of the average mobility μ_{avg} is modeled by a power law with two parameters α and β

$$\mu_{avg}(V_g) = \alpha(V_g - V_{on})^{\beta}. \tag{A25}$$

The current-voltage equations are derived based on ref. [167] as a function of gate voltage as follows. At the on-state of the TFT, I_d is determined by the mobile carrier charge sheet density available for the conduction, Q_m (in C/cm^2), and the drift mobility of the charge carriers, μ_d, which is dependent in on the Q_m. These are not, however, easily obtained from measurements. Due to charges trapped at the sub-gap trap states, Q_t (in C/cm^2), the Q_m is less than the charge sheet density induced by the gate voltage, Q_g (in C/cm^2). In other words, $Q_g = Q_m + Q_t$ holds. The gate-induced charge sheet density can be written as a function of the effective gate voltage, $V_{eff} = V_g - V(x)$, where $V(x)$ is the drain-field induced voltage at distance x from the source electrode. By $Q = CV$ we can write

$$Q_g(V_{eff}) = C_i[V_g - V(x) - V_{on}], \tag{A26}$$

where V_{on} is the turn-on voltage that denotes the gate voltage where the current conduction commences in the channel. The gate-dependent average mobility of the charge carriers, $\mu_{avg}(V_{eff})$, includes the contributions both from the mobile and the trapped charges and can be obtained by normalizing the drift mobility with the gate-dependent charge sheet density as [167]

$$\mu_{avg}(V_{eff}) = \mu_d \frac{Q_m(V_{eff})}{Q_g(V_{eff})}. \tag{A27}$$

From here on we denote for clarity the voltage-dependent parameters $Q_g(V_{eff})$, $Q_m(V_{eff})$, and $\mu_{avg}(V_{eff})$ as $\bar{Q}_g$, $\bar{Q}_m$, and $\bar{\mu}_{avg}$, respectively.

Similarly as (A1) - (A4) for the square-law, we can derive the expression for I_d from the charge density considerations and we get

$$I_d dx = W\mu_d \bar{Q}_m dV(x). \tag{A28}$$

By using (A27), we can re-write this as

$$I_d dx = W\bar{\mu}_{avg}\bar{Q}_g dV(x) = WC_i\bar{\mu}_{avg}\left[V_g - V(x) - V_{on}\right]dV(x), \tag{A29}$$

where the last form utilizes (A26). Integration and rearrangement yields

$$I_d = \frac{W}{L}C_i\int_{V(x)=0}^{V_d}\bar{\mu}_{avg}\left[V_g - V(x) - V_{on}\right]dV(x). \tag{A30}$$

Now, with the help of the power law for the average mobility (A25) we get

$$I_d = \frac{W}{L}C_i\alpha\int_{V(x)=0}^{V_d}\left[V_g - V(x) - V_{on}\right]^{\beta+1}dV(x), \tag{A31}$$

and calculating the integral yields finally a relation for the drain current at the pre-pinch-off region

$$I_d = \frac{W}{L}C_i\frac{\alpha}{\beta+2}\left[\left(V_g - V_{on}\right)^{\beta+2} - \left(V_g - V_{on} - V_d\right)^{\beta+2}\right]. \tag{A32}$$

For the saturation occurring at $V_d = V_g - V_{on}$, we get saturation drain current of

$$I_d = \frac{W}{L}C_i\frac{\alpha}{\beta+2}\left(V_g - V_{on}\right)^{\beta+2}. \tag{A33}$$

Quasi-static unity-gain frequency

When taking to account the overlap capacitances of a real TFT, the total gate capacitance is given by

$$C_{gate} = C_{chan} + C_{gs} + C_{gd} = C_i W(L + L_{gs} + L_{gd}), \tag{A34}$$

where C_{chan}, C_{gs}, C_{gd}, and C_i are the channel capacitance, gate-source overlap capacitance, drain-source overlap capacitance, and the areal capacitance of the gate dielectric ($C_i = \varepsilon_i\varepsilon_0/d_i$), respectively. W, L, L_{gs}, and L_{gs} are the channel width, channel length, gate-source overlap length, and gate-drain overlap length, respectively.

Unity-gain denotes the frequency when $gain = I_{out}/I_{in} = 1$ holds. The unity-gain frequency f_t in a quasi-static model is given by

$$f_t = 1/T_c, \tag{A35}$$

where T_c denotes the time needed to empty the charge stored in the capacitor C_{gate} to the drain electrode. The following derivation for f_t is based on the one by Kawamura *et al.* in ref. [69]. In a TFT, the output current is given by

$$I_{out} = I_d = g_m V_g, \tag{A36}$$

where $g_m = \partial I_d / \partial V_g$is the transconductance of the TFT. The transconductance in saturation is obtained from Equation (A8)

$$g_m = \partial I_d / \partial V_g = \frac{W}{L} \mu_{sat} C_i \left(V_g - V_t\right). \tag{A37}$$

The input current is the current required to swing the gate capacitance, i.e. fill the C_{gate}, by applying a voltage at the gate. Based on the complex impedance of a capacitor given as $Z = -i/\omega_f C$, where i is the imaginary unit, and ω_f is the angular frequency ($\omega_f = 2\pi f$), the input current can be written with the help of Equation (A34) as

$$I_{in} = I_{gs} = V_g / Z_{gate} = i2\pi f C_i W (L + L_{gs} + L_{gd}) V_g. \tag{A38}$$

Note here that the I_{gs} is different from the gate leakage current I_g. In saturation, the channel is at pinch-off and the contribution from C_{gd} can be neglected.

The current gain written based on Equations (A36) – (A38) is

$$gain = |I_{out}| / |I_{in}| = \frac{\mu_{sat}\left(V_g - V_t\right)}{2\pi f L (L + L_{gs})}. \tag{A39}$$

Finally, at the unity-gain frequency, we can write

$$f_t = \frac{\mu_{sat}(V_g - V_t)}{2\pi L (L + L_{gs})}. \tag{A40}$$

Appendix B: Erratum

In Figure 36 (a) and in Figure 2 (a) of **Publication [IV]**, the last Roman numeral should read VI instead of V.

Publication I

J. Leppäniemi, O.-H. Huttunen, H. Majumdar, and A. Alastalo, “Flexography-Printed In2O3 Semiconductor Layers for High-Mobility Thin-Film Transistors on Flexible Plastic Substrate,” Advanced Materials, vol. 27, no. 44, pp. 7168–7175, November 2015;

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Flexography-Printed In_2O_3 Semiconductor Layers for High-Mobility Thin-Film Transistors on Flexible Plastic Substrate

*Jaakko Leppäniemi, Olli-Heikki Huttunen, Himadri Majumdar, and Ari Alastalo**

Thin-film transistors (TFTs) based on solution process of organic, metal-oxide and carbon-nanotube-network semiconductors are being studied beyond the conventional amorphous silicon (a-Si) and low-temperature polysilicon (LTPS) semiconductors for novel flexible electronic applications.[1–4] Metal-oxide TFTs offer advantages over organic TFTs such as a higher charge carrier mobility that leads to higher achievable current density and circuit speed.[3] In contrast to the widely used a-Si semiconductor, where the conduction band is based on covalently bonded Si atoms with highly directional hybridized sp^3 orbitals, n-type metal-oxide semiconductors such as In_2O_3, In–Zn–O (IZO), and In–Ga–Zn–O (IGZO), where the conduction band is made of spherical *s*-orbitals with lower dependence of interatom wave function overlap on the bond angles between neighboring metal atoms, have shown to exhibit nearly as high charge-carrier mobility in amorphous films as in crystalline films and typically beyond that of a-Si.[2,3,5] Typically, Zn- and Ga-doping of In_2O_3 are utilized to allow the film to remain in amorphous phase during annealing and to control the charge-carrier concentration through limiting oxygen-vacancy formation with their ability to form stronger oxygen-bonds than indium.[2,3] Although undoped In_2O_3 possess high bulk charge-carrier concentration limiting its usability as semiconductor channel, thin (≈10 nm) In_2O_3 semiconductor layers have recently been successfully utilized as semiconductor layers for high-mobility solution-processed TFTs, albeit in some cases with nonoptimal depletion-mode operation.[6–12]

Metal-oxide semiconductor layers can be solution processed from stabilized nanoparticle dispersions or from sol-gel-precursor solutions.[3,4] Nanoparticles typically require high temperature sintering (>400 °C) to allow a connected network of particles and to remove dispersion stabilizing encapsulants. Although recently, chemical removal of the stabilizing encapsulant of In_2O_3 nanoparticles has been shown to enable low processing temperatures and allow good TFT performance when combined with short TFT channels (≈10 µm) and an electrolyte-gate,[13] the metal-oxide precursor route yields readily more uniform, continuous and dense layers and is thus more suitable for printed TFTs with larger channel dimensions. Several precursor routes for solution-processed metal-oxide semiconductor layers based on metal alkoxides,[14,15] and on metal salts such as acetates, nitrates, and chlorides have been reported.[16,17] Precursors based on metal nitrates have been shown to convert into metal oxides generally at lower temperatures than acetate- or chloride-based precursors.[17,18] In contrast to metal alkoxides, metal nitrates are less sensitive to air humidity and can be processed via an aqueous precursor route.[7] Based on these advantages, metal nitrates show promise as potential precursor materials for printed low-temperature-processed metal-oxide semiconductors. A large amount of work has concentrated on lowering the conversion temperature of the precursor solutions to semiconducting metal-oxide layers. Functional TFTs have been obtained at ≈200 °C or below (1) via the careful design of precursor chemistry utilizing metal alkoxides with controlled hydrolysis,[14,15] combustion process,[11,19] or the addition of oxidizing agents,[20] (2) via the use of additional energy in conversion such as various wavelengths of UV light,[8,15,21] or microwaves,[22] or (3) by employing conditions during annealing that promote efficient precursor conversion such as ozone or vacuum.[6,7,20] After the first report on inkjet-printed metal oxide layers from metal chloride precursors by Lee et al. in 2007,[16] the deposition of metal-oxide semiconductor layers for TFTs has been successfully performed via several printing techniques.[4] In addition to inkjet-printing,[12,16,17,19,23] metal-oxide TFTs have been fabricated with electrodynamic-jet,[24] spray pyrolysis,[9] gravure (glass substrate, 550 °C annealing),[25] and flexographic printing (Si wafer, 450 °C annealing).[26] The inkjet, electrodynamic jet, and spray pyrolysis techniques are typically utilized in noncontact sheet-to-sheet batch processes while the contact gravure and flexographic printing are readily available also as continuous high-throughput roll-to-roll processes. Also novel combinations of conventional vacuum processes and techniques well known from the field of printing have been proposed to prepare metal-oxide TFTs on flexible substrates such as inkjet-printed growth inhibitors for the patterning of atomic-layer-deposited (ALD) metal-oxide layers,[27] and transferring of vacuum-processed functional TFTs from rigid to flexible substrates by a roll-transfer method.[28] The previous results clearly indicate the challenges in the processability of materials that need to be overcome to enable large-area electronics fabrication using the industrial high-throughput additive printing processes on flexible low-cost substrates.

In this work, for the first time, the metal-oxide TFT fabrication process was performed on flexible substrate using process technologies that are roll-to-roll-compatible and industrially scalable, namely, flexographic printing and atomic layer deposition (ALD),[29,30] for the deposition of the

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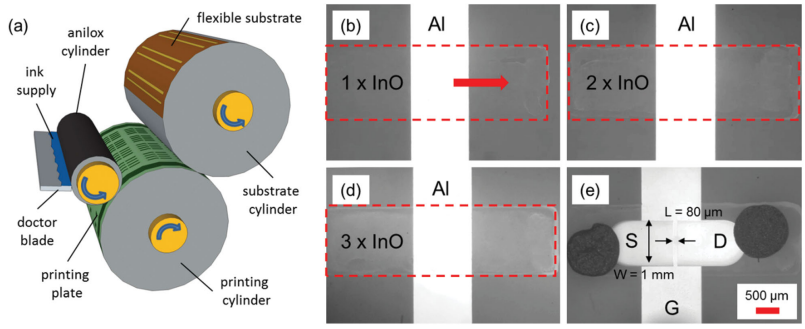

Figure 1. a) Schematic image of the flexographic printing process. Optical microscope images of In_2O_3 layers printed with b) one, c) two, and d) three successive runs with InO-ink perpendicular to the Al gate lines. The contrast and brightness of the images are optimized to show the printed layer and the edges are highlighted with red dashed lines. Red arrow indicates the printing direction. e) Dimensions of a completed TFT device with source (S), drain (D), and gate (G) contacts annotated. Width (W) and length (L) for the semiconducting channel are shown with a scale bar. Black dots are Ag paint to help the probing of the samples.

semiconductor and dielectric layers, respectively. We show that flexographic printing can be used to fabricate thin (<20 nm) continuous layers of In_2O_3 from In-nitrate precursor solution without printability-improving additives that could degrade the electrical performance. By fabricating bottom-gate top-contact In_2O_3 TFTs with ALD-grown amorphous Al_2O_3 gate dielectric using a 300 °C processing temperature on high-temperature-tolerant and dimensionally stabile flexible plastic substrates, we reach TFT performance with saturation mobility of (μ_{sat}) ≈8 $cm^2\ V^{-1}\ s^{-1}$, enhancement-mode operation with turn-on voltage (V_{on}) of ≈0 V, drain ON-current (I_D) of ≈1 mA, drain current ON/OFF-ratio above 10^6 and negligible gate leakage current (I_G) of ≈1 nA. We also identify the importance of annealing temperature, thickness of the In_2O_3 films and post-contact-annealing conditions of the film on the TFT device performance. To our knowledge, these are the first results of high-performance metal oxide-TFTs obtained with roll-to-roll-compatible process technologies on a flexible substrate. The presented work paves the way for printed circuits from metal-oxide TFTs on flexible substrates.

Flexographic printing offers several advantages such as high-throughput, good line edge definition, and the low cost of printing plates when compared to gravure printing.[29] As the first step, we optimized the printing quality of the single-solvent and additive-free precursor solution of 0.2 M In-nitrate in 2-methoxyethanol (2-ME), denoted as InO-ink from hereon (preparation steps in the Experimental Section), on flexible substrates by adjusting the anilox (between anilox and printing cylinders) and nip (between printing and substrate cylinders) pressures of the flexographic printing unit and by controlling the transfer volume of the anilox roll. A schematic image of the flexographic printing process is shown in **Figure 1**a. In order to obtain thin semiconductor layers in the ≈10 nm range, thus well below the typical µm-thickness obtained with conventional flexographic inks,[29] the low solid content (6.8 wt% In-nitrate) and the low viscosity InO-ink (≈2 cP for 2-ME) was printed using high printing speed of 50 m min^{-1} and low transfer volumes of 3–5 mL m^{-2}, that all promote the printability of thin layers. Crucial to the formation of optically continuous films in the printing process, initial 1 min O_2 plasma treatment was used to improve the wetting properties by reducing the contact angle of the InO-ink on ALD-grown Al_2O_3 surfaces from ≈17° to ≈5° (Figure S1a,b, Supporting Information). Transfer volume of 3 mL m^{-2} yielded films with the least amount of material flow in the printing direction and thus more homogenous layers when compared to the higher transfer volumes of 4 and 5 mL m^{-2}.

The bottom-gate top-contact TFT devices were fabricated using InO-ink on high-temperature-tolerant and dimensionally stabile flexible polyimide substrates in the following process steps: (1) gate-electrode deposition by vacuum evaporation; (2) Al_2O_3 via ALD; (3) flexographic printing of InO-ink; (4) drying and thermal annealing of InO-ink; (5) source-drain-contact deposition by vacuum evaporation; and (6) post-contact annealing. In the following text we discuss the processing steps and the rationale behind the relevant processing parameters that can be found in detail in the Experimental Section.

We utilize flexographic printing of multiple thin (<10 nm) precursor layers on top of each other to realize the semiconductor layer, thus taking further the approach that earlier has been shown via consecutive spin-coating steps to enhance solution processed metal-oxide TFT performance in terms of mobility, device-to-device variation and stability by improving semiconductor layer morphology (increasing density, reducing porosity).[17,31] Multilayer flexographic printing (1–3 layers) of InO-ink with 3 mL m^{-2} transfer volume was performed on the polyimide substrates with prepatterned Al-gate lines as the bottom gate and ALD-grown ≈100 nm thick amorphous Al_2O_3 as the gate dielectric. Consecutive semiconductor layers were printed perpendicular to the Al-gate electrodes as shown in Figure 1b,d without an interlayer drying step that was found to cause poor wetting on top of the preceding layer (Figure S2a, Supporting Information). SEM images of the completed TFT devices show that continuous layers could be obtained for 1–3 printed layers (Figure S3a–c, Supporting Information). The thickness and roughness of the printed InO-ink films are summarized in **Table 1**. The thickness of the printed layers was found to increase by ≈7–10 nm by each printed layer with a complementing decrease in the average surface roughness R_a when measured after annealing the films as shown in Table 1 (AFM scans in Figure S4, Supporting Information). This is

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Table 1. Layer and In_2O_3 TFT device characteristics for varied amount of successive printed InO-ink layers.

# layers	Gate-electrode material	Al_2O_3 gate oxide thickness [nm]	Amount of devices	In_2O_3 layer thickness d_{avg} [nm]	In_2O_3 film roughness R_a [nm]	TFT saturation mobility μ_{sat} [$cm^2 V^{-1} s^{-1}$]	Turn-on voltage V_{on} [V]	Sub-threshold slope [V dec^{-1}]	Hysteresis V_{hyst} [V]
1	Al	100	11	7 ± 3	1.2	<0.4	0.7 ± 0.9	1.2 ± 0.6	1.4 ± 0.6
2	Al	100	42	15 ± 2	1.1	2 ± 1	−0.2 ± 0.4	0.8 ± 0.3	1.0 ± 0.3
3	Al	100	22	25 ± 6	1.0	5 ± 3	−1.0 ± 0.5	0.8 ± 0.4	0.7 ± 0.2
2	Au	75	22	14 ± 4	0.5	8 ± 4	−0.6 ± 0.5	0.4 ± 0.1	0.7 ± 0.3

supported by the high-magnification SEM images of the Al_2O_3 dielectric and printed In_2O_3 layers in which the morphology of the top surface of the Al_2O_3 dielectric is less visible through increasing amount of printed In_2O_3 layers (Figure S5, Supporting Information). The observed smoothening of the top surface of the In_2O_3 layers suggests that the InO-ink is at least partly flowing on the surface during the multilayer printing.

After the printing and drying steps, the InO-films were thermally annealed in air. Even though several previously mentioned low-temperature annealing methods exist for solution processed metal-oxide semiconductor layers, we focused in this particular work on readily scalable thermal conversion of the InO-ink to In_2O_3 layers on high-temperature tolerant flexible substrate. Thermal annealing of precursor-derived solution-processed In_2O_3 is a balance between the temperature required for complete and impurity-free precursor-to-oxide conversion and the onset of formation of a significant fraction of crystalline inclusions in the amorphous phase that can limit the electron mobility by increased scattering, as reported by Buchholz et al. for pulsed-laser-deposition (PLD) processed In_2O_3 layers. However, the In_2O_3 films can exhibit moderate mobility even with 70 % of crystalline phase.[5] Here, the annealing temperature of 300 °C was selected based on thermal and chemical analysis of the InO-ink conversion process that was performed for dried precursor with thermogravimetric analysis (TGA), differential thermal analysis (DTA), mass spectrometry (MS), and Fourier transform infrared spectroscopy (FTIR). The mass loss in the TGA data shown in **Figure 2**a confirms that the precursor conversion is nearly completed at 300 °C. DTA analysis indicates that the conversion of the dried InO-ink in air is a complex process with two main exothermic peaks.The first exothermic peak in DTA at ≈120 °C can be associated to the liberation of NO_x (NO, NO_2) and H_2O in condensation reactions, as shown in the MS signal Figure 2b,[32] which possibly hinder the endothermic peak of evaporation of any remaining 2-ME (bp ≈ 125 °C). The process continues until the second main exothermic peak at 260–290 °C, where the remaining 2-ME, NO_x and H_2O are liberated and In_2O_3 is formed,[32] and which is possibly linked to changes in the film morphology. The remaining broad exothermic reaction at temperatures beyond 300 °C in the DTA data can be associated to further amorphous to crystalline transition of the In_2O_3 layer. To complement the thermal analyses, we performed FTIR measurements on InO-ink films on Si/SiO_2 substrates annealed at different temperatures as shown in Figure 2c. The obtained absorption spectra indicate removal of most of the nitrate NO_3^- ions (≈1330–1400 cm^{-1}) and OH^- groups (O–H stretching ≈3200–3600 cm^{-1} and O–H bending ≈1620 cm^{-1}) at 300 °C with no further improvement achieved at higher annealing temperature. The crystal structure of the films on Si/SiO_2 substrates annealed at various temperatures was studied using grazing incidence X-ray diffraction spectrometry (GIXRD). From the spectra shown in Figure 2d, the onset of crystalline inclusions of cubic In_2O_3 can be observed between 200 and 250 °C by the appearance of peaks at 2θ values of ≈31° and ≈35°.[19]

The importance of the annealing temperature is also evident from the TFT device performance. Our spin-coated reference In_2O_3 devices on ALD-grown Al_2O_3 show large hysteresis in transfer characteristics at 275 °C, whereas devices annealed at 300 °C operate with lower hysteresis, which together with the FTIR and the thermal analyses suggest that the In_2O_3 film annealed at 275 °C has too high impurity and charge trap concentration for good operation (see Figure S6b, Supporting Information). In transmission electron microscope (TEM) analysis of the cross section of the reference devices annealed at 300 °C shown in Figure 2e,f, ≈30 nm thick continuous layers with randomly oriented nanocrystalline domains of In_2O_3 can be detected with <10 nm of average size and ≈0.3 nm lattice plane separation. The presence of such nanocrystalline domains is evident also from the GIXRD measurements performed on In_2O_3 layers on Al_2O_3 as shown in the inset of Figure 2d, accompanied with the broad peak of amorphous Al_2O_3 at $2\theta = 22°$.[33] The variation of the crystallinity of the film with thickness and processing conditions is critical for the optimized operation of the transistors. Earlier, thin (≈7 nm) nanocrystalline In_2O_3 films have been obtained from the In-nitrate-route on thermally oxidized SiO_2 surface via spray pyrolysis at 250 °C,[9] whereas spin-coating has produced thin (<6 nm) amorphous In_2O_3 structures with less than 10% of crystalline phase at 300 °C on chemical vapour deposited (CVD) SiO_2 surface.[10] Recently, the maximum temperature for retaining the amorphous phase of In_2O_3 has been extended with mixing In-precursor with poly(4-vinylphenol) (PVP) polymers.[11] Since the roughness of the top surface of the In_2O_3 layer is reducing with increasing amount of layers, we do not expect a notable increase in average diameter of the nanocrystals with increasing semiconductor thickness. Active research on identification of the effect of different processing conditions, interfaces and precursor materials on the formation of either nanocrystalline or amorphous In_2O_3 thin film is required but is, however, outside the scope of this article.

After annealing, the TFT devices were completed with evaporated top contacts for source and drain electrodes using Al to provide good contact to the In_2O_3 semiconductor.[34,35] After the evaporation process performed in vacuum at typical pressure of 5×10^{-9} atm, the TFT devices exhibit high conductivity, a

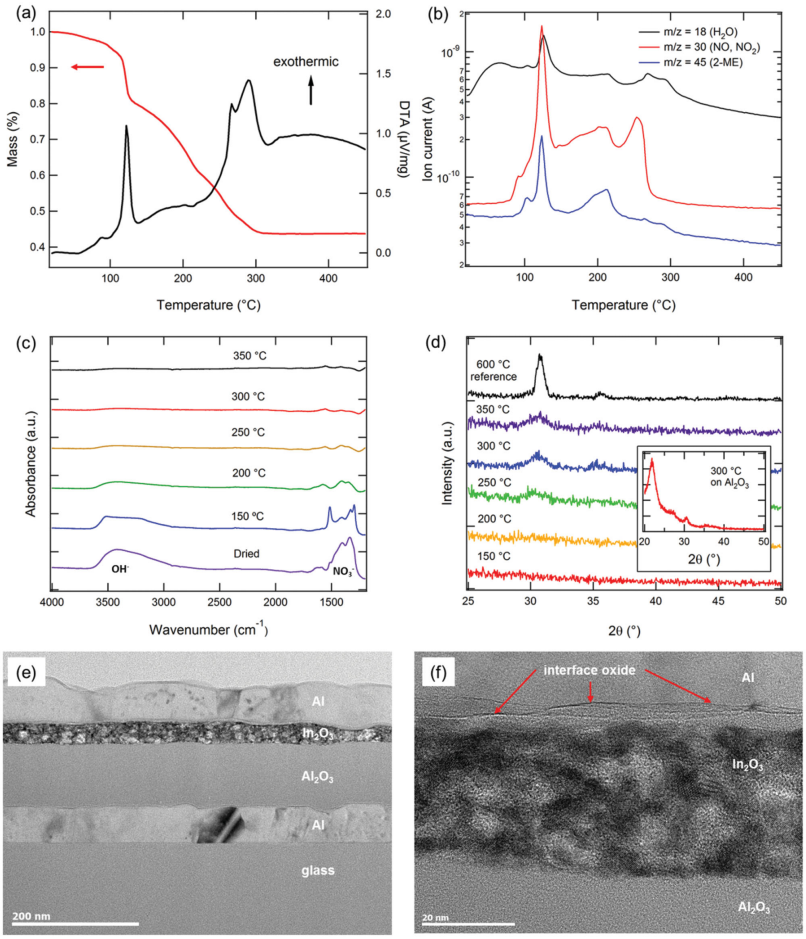

Figure 2. a) TGA and DTA thermal analyses for InO-ink. b) Mass-spectrometry ion current for selected *m*/*z*-values corresponding to InO-ink conversion products H_2O, NO_x, and 2-methoxyethanol as function of temperature (raw data). c) FTIR spectra of In_2O_3 films annealed at different temperatures with peaks related to OH^- and NO_3^- groups annotated. d) GIXRD measurements of In_2O_3 films annealed at different temperatures. Inset shows GIXRD on ALD Al_2O_3 surface. e) Cross-section transmission electron microscope (TEM) images of spin-coated In_2O_3 on top of Al_2O_3 under contact electrode. f) Close-up TEM image of In_2O_3 layer indicates nanocrystalline domains of In_2O_3. The red arrow indicates a thin (<1 nm) interface oxide-layer.

very negative V_{on} and poor gate modulation (see Figure S6a, Supporting Information) owing to oxygen vacancies in the In_2O_3 film that are understood to increase the charge-carrier concentration.[2,3] The depletion of oxygen from the semiconductor can be due to the evaporated Al-electrodes scavenging oxygen from the underlying In_2O_3 film.[35] This results from lower (more negative) Gibbs free energy of formation for Al_2O_3 (–1054 kJ mol^{-1} per mole of O_2) than In_2O_3 (–553 kJ mol^{-1} per mole of O_2) thus owing a spontaneous reduction of In_2O_3 and oxidation of Al at the interface.[36] The formation of thin (<1 nm) interface oxide layer between the Al-contacts and the semiconductor can be observed in the close-up TEM image in Figure 2f, indicating the formation of a compound interface,[36] and giving direct evidence of AlO_x formation during evaporation as also postulated by Xu et al.[35] In addition, oxygen depletion from the surface of the In_2O_3 film during the exposure to low oxygen partial pressure ($p_{O2} \approx 1 \times 10^{-9}$ atm, by assuming similar pumping rates for N_2 and O_2) can occur due to the relatively low formation entalphy $\Delta H(V^O)$ of oxygen vacancies at the surface of the In_2O_3 film.[37] However, by performing a low temperature post-contact-annealing step in air at 150 °C for 30 min,[8,35] the oxygen vacancies of the In_2O_3 film are brought closer to equilibrium with the oxygen partial pressure in normal conditions ($p_{O2} \approx 0.2$ atm) and the turn-on voltage, V_{on}, of the In_2O_3 TFTs can be reproducibly positioned to ≈0 V for enhancement-mode operation, as shown in Figure S6a, Supporting Information, for spin-coated reference devices on Si/SiO_2.

The electrical characteristics of the TFT devices with printed In_2O_3 semiconductor are summarized in Table 1. Typical

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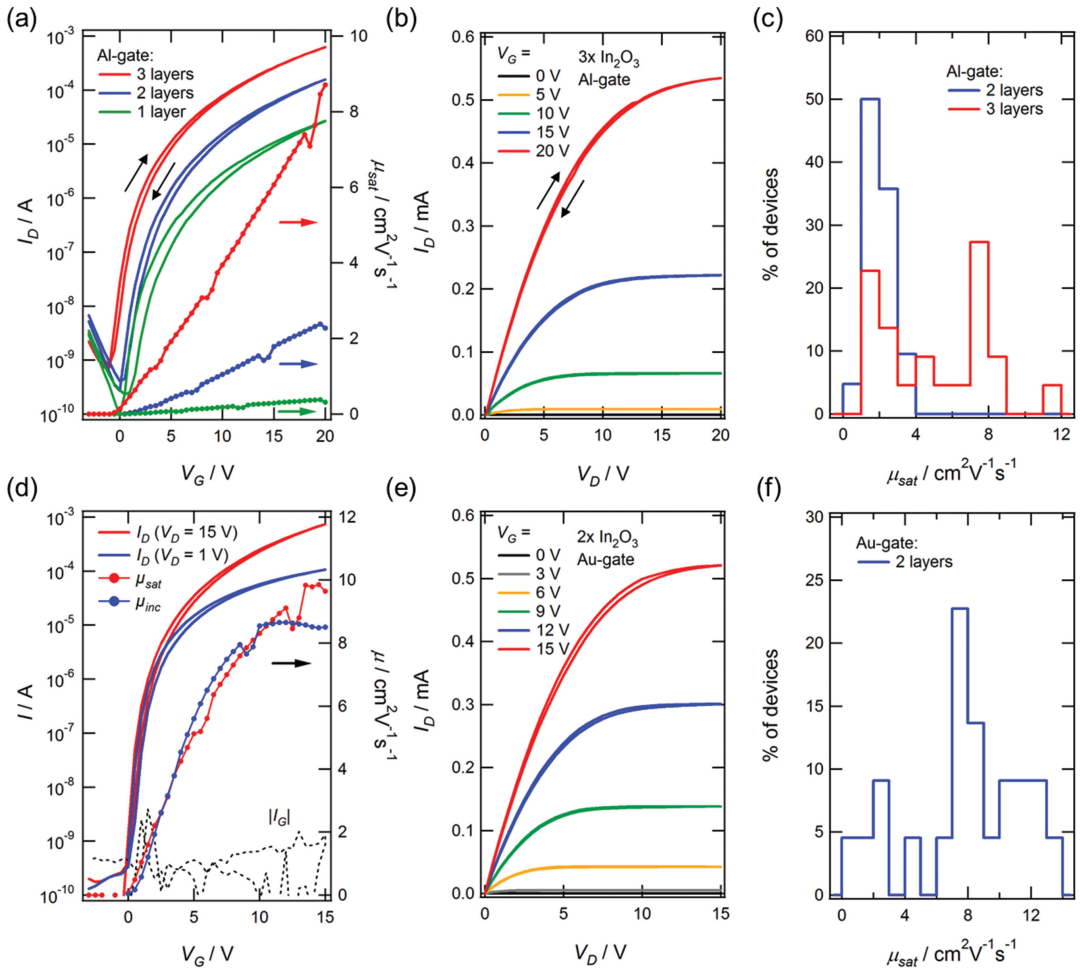

Figure 3. In_2O_3 TFT characteristics for $W \approx 1$ mm and $L \approx 80$ µm devices ($W/L \approx 12.5$) with printed In_2O_3 layers. a) Transfer characteristics of typical TFTs with one, two and three printed InO-ink layers along with calculated saturation mobility (right axis). b) Output characteristics for TFT with three InO-ink layers. c) Histogram of saturation mobility for devices with two and three InO-ink layers. d) Transfer characteristics of typical TFTs with two printed InO-ink layers on Au-gate with calculated saturation and incremental mobility (right axis). e) Output characteristics for TFT with two In_2O_3 layers on Au-gate. f) Histogram of saturation mobility for devices with two InO-ink layers on Au-gate.

transfer curves for devices with one, two and three successive InO-ink layers are shown in **Figure 3**a, indicating good switching properties with efficient gate modulation. The gate leakage currents I_G of pinhole-free devices were in the order of 1 nA as shown for devices with two and three InO-ink layers in Figure S7a,b, Supporting Information. On the average, the saturation mobility of the devices increases in tandem with the amount of printed layers. The devices with single layer exhibit a very low mobility with $\mu_{sat} = 0.4$ cm^2 V^{-1} s^{-1} at maximum along with a large spread in mobility with values spanning several decades below the maximum value. The low thickness of the films possibly prevents the formation of a continuous path in the channel and gives rise to the observed high variation. This is supported by the SEM images of the channel layer (Figure S5b, Supporting Information) where the structure of Al_2O_3 is still clearly visible through the single layer of InO-ink. However, for the devices with two InO-ink layers, the mobility increases to $\mu_{sat} = 2 \pm 1$ cm^2 V^{-1} s^{-1} along with a decrease in the variation. The devices with three InO-ink layers exhibit even higher mobility of $\mu_{sat} = 5 \pm 3$ cm^2 V^{-1} s^{-1}, however, accompanied by an increase in the mobility spread. This is evident from the mobility histogram shown in Figure 3c, where the average mobility for two layer devices is centered at ≈2 cm^2 V^{-1} s^{-1} whereas for three layer devices, the mobility is divided clearly into two groups centered at ≈2 and ≈7 cm^2 V^{-1} s^{-1}. Although some of the three-layer devices exhibit uneven spreading of

InO-ink on the top layer, the origin of the two mobility peaks cannot be fully correlated to uneven wetting and the exact reason might lie in the observed nanocrystalline nature of the resulting In_2O_3 films. Thermally evaporated thin polycrystalline In_2O_3 TFTs have been shown to exhibit a strongly thickness-dependent mobility in the 5–20 nm thickness range which could amplify a small variation in semiconductor thickness into large variation in device mobility.[38] In this scenario, the observed spread in device mobility could be improved by suppressing In_2O_3 crystallization for obtaining more homogenous amorphous phase via conventional Ga/Zn-doping or via PVP,[2,3,11] or by further optimization of the printing process for low variation in film thickness of the nanocrystalline In_2O_3. The incremental mobility for two and three layer devices measured at the linear regime at drain voltage $V_D = 1$ V (see Figure S7a,b, Supporting Information) is monotonously increasing with gate voltage V_G from V_{on} up to 20 V, which indicates that the devices operate at the trap-filling-limited mobility regime rather than in the regime where mobility is limited by semiconductor-dielectric interface scattering.[3,39,40] Since the In_2O_3 films contain nanocrystalline inclusions, the operation characteristics of the devices can be qualitatively understood based on the polycrystalline TFT model by Levinson et al.[41] The grain boundaries at the edges of the crystallites have overlapping depletion regions which act as initially neutral charge traps and can compensate for possible large bulk charge carrier concentration of In_2O_3. The barrier height of the grain boundary traps is modulated by the total charge carrier concentration which includes both bulk charges arising from nonstoichiometry (i.e., oxygen vacancies), n_B, and charges induced by the gate voltage, n_G.[3] At low V_D, a uniform charge concentration per unit area of $n_G = C_i V_G/q$ is induced in the channel as the gate voltage V_G is increased, where C_i is the gate dielectric capacitance density per unit area and q the elementary charge. The grain boundary traps are then filled with n_G before obtaining switching from off- to on-state,[41] resulting in gradually increasing mobility.[3] Apparent from Figure 3a and Table 1, V_{on} is moving slightly toward more negative values with increasing amount of layers accompanied with an increase in the drain current at $V_G = 0$ V. This can arise from the higher semiconductor thickness having larger n_B and thus more available charges to prefill the traps in the channel already at the unbiased condition. The mobility also increases in tandem with thickness as the thicker channels allow more percolation paths for conduction. The devices show flat saturation in their output curves, as shown in Figure 3b for a three layer device, which together with $V_{on} \approx 0$ V indicates that the semiconductor possess a charge-carrier concentration that is low-enough for good TFT operation and no charge accumulation layer exists on the back-channel (semiconductor–air interface) which would contribute to bulk and surface leakage, respectively.[39] The sub-threshold swing of the devices decreased from 1.2 ± 0.6 V dec^{-1} for single layer to 0.8 ± 0.3 and 0.8 ± 0.4 V dec^{-1} for two and three layer devices, respectively, in tandem with a decrease in the device operation hysteresis from 1.4 ± 0.6 V down to 0.7 ± 0.2 V for one and three InO-ink layer devices, respectively. The enhancement of the both characteristics can be assigned to the reduced degree of charge trapping as indicated by the decrease in the calculated trap density N_{trap} (Table S1, Supporting Information). The reduction in N_{trap} could be due diminishing contribution of the top interface to charge trapping as the roughness of the top layer decreases when the thickness of the layer increases, or due to improvements in the layer morphology such as pore filling and increased layer density.[17,31]

The roughness of the Al_2O_3 layer is higher on top of the Al-gate ($R_a = 1.4$ nm) than on the bare substrate ($R_a = 0.4$ nm) (Figure S4, Supporting Information), which indicates that the underlying Al-gate contributes to the roughness of the dielectric-semiconductor interface. However, by employing an Au-gate instead of Al, the roughness of the channel interface can be reduced to $R_a = 0.7$ nm. In an optimized process, where Au-gate, lower gate dielectric thickness (75 nm) and extended 2 min O_2 plasma surface pretreatment for full wetting (Figure S1c, Supporting Information) are combined, the printing quality in terms of layer uniformity can be improved, as shown in optical microscope (Figure S2c, Supporting Information) and in high-magnification SEM (Figure S5f, Supporting Information) images and supported by the reduced roughness ($R_a = 0.5$ nm) of the top In_2O_3 surface. The enhanced electronic properties of the two InO-ink layer devices in mobility $\mu_{sat} = 8 \pm 4$ cm^2 V^{-1} s^{-1} and in sub-threshold slope 0.4 ± 0.1 V dec^{-1} indicate a reduction in the amount of charge traps (Table S1, Supporting Information). Moreover, based on the peaking incremental mobility shown in Figure 3d, the device operation is now limited by the interface scattering instead of trap limited operation which also suggests less traps present in the film when compared to devices with Al-gates.[3,39,40]

In a positive bias-stress (PBS) measurement for device operation stability performed at +1 MV cm^{-1} gate field, reversible positive turn-on voltage shifts of ≈8.6 and ≈6.3 V are observed in 4000 s for devices with two InO-ink layers on Al- and Au-gates, respectively, which indicate charge trapping in the semiconductor film or in the semiconductor-dielectric interface (Figure S7c, Supporting Information).[3,39] The reduced V_{on}-shift observed for the device with Au-gate supports the reduced amount of traps for the optimized Au-gated devices. The observed PBS turn-on voltage shift is in the same order as reported for inkjet-printed In_2O_3 devices from similar In-nitrate precursor on Si/SiO_2 substrates.[12] In a negative bias-stress (NBS) measurement at −1 MV cm^{-1} gate field, smaller negative shifts of −1.4 and −3.4 V are observed in 4000 s for Al and Au-gated devices, respectively. We assign the observed negative shift to depletion of the prefilled charge traps at the grain boundaries by the negative gate voltage. The electrical stability of the devices could be readily improved by utilizing for the printed semiconducting channel a single multicomponent oxide material with higher stability, such as IGZO,[2,3] or sequencing of semiconducting metal oxide layers with high mobility-low stability (e.g., In_2O_3 or ITZO) and low mobility-high stability (e.g., IGZO).[31] Our initial tests with inkjet-printing of the InO-ink on Si/SiO_2-substrates yield functional TFT devices when annealed at 300 °C with comparable mobility of ≈4 cm^2 V^{-1} s^{-1} which could provide a straightforward method for studying the sequencing of printed thin metal-oxide semiconductor layers with varied material composition.

In summary, we showed that flexographic printing of In-nitrate-based metal-oxide precursor ink can be utilized to form continuous thin nanocrystalline In_2O_3 semiconductor layers

on high-temperature tolerant flexible substrates. The process leads into high-mobility In_2O_3 TFTs on ALD-grown amorphous Al_2O_3 with $\mu_{sat} \approx 8$ cm^2 V^{-1} s^{-1} which show enhancement-mode operation with reproducible turn-on voltages at ≈0 V after a low-temperature post-contact-annealing step. By combining the demonstrated process with available UV-based low-temperature annealing schemes,[8,15,21] roll-printed metal-oxide TFT devices and circuits on low-cost plastic substrates can be achieved in the future.

Experimental Section

In_2O_3 Precursor Ink Synthesis: Precursor ink for indium oxide (In_2O_3) (InO-ink) was prepared by dissolving $In(NO_3)_3 \cdot xH_2O$ (obtained from IGCatalyst Ltd.) in anhydrous 2-methoxyethanol (Sigma-Aldrich 99.8%) in 0.2 M concentration (6.8 wt% of $In(NO_3)_3 \cdot xH_2O$). Similarly as given by Kim et al.,[22] the solution was stirred at 75 °C for more than 12 h and filtered prior using with a 0.45 μm pore size glass fibre filter. The water content of the ready ink was measured to be ≈1 wt% with Karl Fischer titration (Mettler Toledo DL37), thus indicating the presence 2.5 of crystal H_2O per In-atom. TGA, DTA, and MS of the InO-ink thermal conversion were performed using Netzsch STA 449 Jupiter/Netzsch QMS 403C Aëolos and Al_2O_3 sample cup in air ambient with 5 °C min scan rate after drying InO-ink 1 h at 90 °C.

Thin-Film Transistor Device Fabrication: Bottom-gate top-contact TFTs were prepared on flexible 38 μm thick Xenomax polyimide substrate (TOYOBO Co. Ltd., Japan). First, Al or Au metal gate lines were evaporated using thermal evaporation in vacuum. Conventional batch process ALD was then used to fabricate ≈100 nm thick (≈75 mn for Au-gate) Al_2O_3 gate dielectric at 300 °C using trimethyl aluminum and H_2O as precursors. Flexographic printing of the patterned semiconductor layer was performed with RK Flexiproof 100 table-top printing machine on the substrates after 1 or 2 min O_2 plasma treatment (≈200 W, Diener Nano) for the Al-gated and optimized Au-gated devices, respectively. The contact angle of the In_2O_3 precursor ink was measured on the Al_2O_3 surface before and after plasma treatments using contact angle goniometer with Young/Laplace-fitting (CAM 200 KSV). The precursor ink was printed on top of the gate lines with printing direction perpendicular to the gate electrode lines. The printing was optimized with print speed of 50 m min^{-1} for homogenous layers using anilox rolls with different transfer volumes: 3 mL m^{-2} (400 lines cm^{-1}), 4 mL m^{-2} (320 lines cm^{-1}), and 5 mL m^{-2} (200 lines cm^{-1}). After printing, the samples were dried at 90 °C on a hot plate in air for 15 min. and then annealed at 300 °C for 30 min. A metal shadow mask having patterns for source and drain electrodes with a width-to-length-ratio (W/L) of ≈12.5 ($W = 1$ mm, $L = 80$ μm) was aligned to the printed semiconductor areas. ≈50 nm of thermally vacuum evaporated Al was used for the S/D-contacts for ensuring good injection properties. The devices were post-annealed on a hot plate at 150 °C for 30 min in air. The number of TFTs with identical processing was at least 20 to gain information on statistical device variation. Reference devices were prepared using spin-coating of InO-ink at 6 krpm on Si/SiO_2 (100 nm thermal oxide), ALD-grown Al_2O_3 (100 nm) on glass (Corning Eagle) or Xenomax substrates with the process parameters kept otherwise the same.

Electrical Characterization: Electrical characterization of the TFTs was performed in dark using a semiconductor analyser (Keithley 4200 SCS). Back and forth transfer curves were recorded in saturation mode by sweeping gate voltage V_G in 0.5 V steps using 0.01 s step time while keeping drain voltage $V_D = 20$ V constant. The output curves were recorded by sweeping drain voltage V_D in 0.5 V steps using 0.01 s step time while keeping gate voltage V_G constant. The saturation mobility is calculated from

$$\mu_{sat} = \frac{\left(\frac{\partial(\sqrt{I_D})}{\partial V_G}\right)^2}{\frac{1}{2} C_G \frac{W}{L}} \quad (1)$$

where I_D is the drain current, C_G the gate capacitance density, and W/L the width to length-ratio of the transistor channel.[3] The incremental mobility probing the mobility of the charge carriers induced by the gate voltage, as introduced by Hoffman,[40] is calculated in the linear operation regime (here $V_D = 1$ V) using

$$\mu_{inc} = \frac{\frac{\partial gd}{\partial V_G}}{C_G \frac{W}{L}} |_{V_D \to 0V} \quad (2)$$

where drain conductance $g_d = \partial I_D / \partial V_D$ was obtained from transfer curve measured at $V_D = 1$ V and by approximating $g_d \approx G_D = I_D / V_D$ at the low V_D.[39] Notably, in this approximation, the incremental mobility equals the conventional field-effect mobility μ_{FE}. The sub-threshold slope was calculated as

$$SS = \left[\max\left(\frac{d \log(I_D)}{dV_G} \right) \right]^{-1} \quad (3)$$

The gate capacitance density of the ≈100 nm thick ALD-grown Al_2O_3 layer was measured as ≈73 nF cm^{-2} ($\varepsilon = 8.3$). Devices shorted to gate electrode (due to impurities, handling, and probing) were omitted from the presented data.

Material Characterization: The printing resolution was characterized using optical microscope. The thickness and the average roughness R_a from 1 μm^2 scan area of the printed In_2O_3 layers were measured after annealing with a stylus profilometer (Veeco Dektak 150) and atomic force microscope (AFM) (Veeco Nanoscope 3), respectively. Spin-coated In_2O_3 films on Si/SiO_2 annealed at different temperatures (150–300 °C) were analysed using FTIR with Ge-crystal in attenuated total reflection (ATR) mode at 4 cm^{-1} resolution (Thermo Scientific Nicolet iS50) and using grazing incidence X-ray diffraction (GIXRD) spectroscopy (Cu Kα peak, Pananalytical Xpert Pro MRD) at 0.5° angle of incidence. Transmission electron microscopy was performed at 200 kV using JEOL 200 TEM. The lamella for the cross-section TEM images was prepared using focused ion beam (FIB) (FEI Dual-Beam Helios 450) with ion energies of 30 and 8 kV for milling and polishing steps, respectively. Scanning electron microscopy (SEM) was done with LEO Zeiss Supra 35 field-emission SEM at 3 kV acceleration voltage.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Publication II

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Rapid low-temperature processing of metal-oxide thin film transistors with combined far ultraviolet and thermal annealing

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We propose a combined far ultraviolet (FUV) and thermal annealing method of metal-nitrate-based precursor solutions that allows efficient conversion of the precursor to metal-oxide semiconductor (indium zinc oxide, IZO, and indium oxide, In_2O_3) both at low-temperature and in short processing time. The combined annealing method enables a reduction of more than 100 °C in annealing temperature when compared to thermally annealed reference thin-film transistor (TFT) devices of similar performance. Amorphous IZO films annealed at 250 °C with FUV for 5 min yield enhancement-mode TFTs with saturation mobility of ~1 $cm^2/(V{\cdot}s)$. Amorphous In_2O_3 films annealed for 15 min with FUV at temperatures of 180 °C and 200 °C yield TFTs with low-hysteresis and saturation mobility of 3.2 $cm^2/(V{\cdot}s)$ and 7.5 $cm^2/(V{\cdot}s)$, respectively. The precursor condensation process is clarified with x-ray photoelectron spectroscopy measurements. Introducing the FUV irradiation at 160 nm expedites the condensation process via *in situ* hydroxyl radical generation that results in the rapid formation of a continuous metal-oxygen-metal structure in the film. The results of this paper are relevant in order to upscale printed electronics fabrication to production-scale roll-to-roll environments. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4895830]

Sputtered amorphous metal-oxide (a-MO) semiconductors have emerged as potential replacements for amorphous silicon (a-Si) and poly-silicon (p-Si) materials in next generation thin-film transistor (TFT) applications.[1] Mixed n-type a-MO semiconductors, such as ternary oxides $M1_xM2_yO_z$, where M1 and M2 are typically post-transition metals (In, Ga, Sn, and Zn),[1–3] or more recently In_2O_3 doped with Si, W, or Ti,[4] or In-Zn-O (IZO) doped with Ba or Sr,[5] have been intensively investigated because of their high carrier mobility, device operation stability, and good optical transparency. The high mobility results from the low spatial dependency of the spherical metal s-orbital that compose the conduction band.[1,2] Although the conventional sputtering process of a-MO layers can also be performed with roll-to-roll (R2R) methods,[6] the solution processing of the a-MO semiconductors offers the possibility of low-cost device fabrication with high-throughput R2R printing methods.[7] Even though the mobility of charge-carriers with the solution processed a-MO semiconductors are superior to that of solution processed organic semiconductor materials,[8] the requirements for high annealing temperature (>350 °C) and long curing time (~1 h) of the a-MO-based semiconductor-layers have been the largest obstacles for R2R fabrication of solution processed TFTs on flexible plastic substrates.

Several approaches have been published on the choice of materials and curing conditions that can lead to fabrication of the a-MO semiconductor layers at low-temperature (<250 °C).[7] The approaches can be divided into two main groups: (1) chemical methods that tailor the constituents of the precursor solution to convert to a-MO layers at low external temperature;[9,10] and (2) annealing methods that utilize alternative energy sources or controlled annealing conditions to limit the processing temperature during the semiconductor annealing.[11–13] Banger *et al.*[9] utilized a controlled hydrolysis of metal alkoxides on the substrates and IZO TFTs processed at 230 °C yield mobility of ~10 $cm^2/(V{\cdot}s)$. Kim *et al.*[10] reported the fabrication of diverse MO films at a low external temperature via a combustion process using inks containing exothermic oxidizers and fuel. The external temperature required to initiate the combustion was 225 °C to attain mobilities of 0.3 $cm^2/(V{\cdot}s)$ and 1.8 $cm^2/(V{\cdot}s)$ with IZO and In_2O_3 TFTs, respectively. To develop new curing methods, Han *et al.*[11] annealed In_2O_3 films in O_2/O_3 atmosphere at 200 °C obtaining TFTs with a mobility of 0.9 $cm^2/(V{\cdot}s)$. Hwang *et al.*[12] showed that post-annealing of In_2O_3 precursors in vacuum yielded TFTs with mobility of 2.4 $cm^2/(V{\cdot}s)$ at a low temperature of 125 °C, but required a pre-annealing step in air for 4 h. Finally, photochemical activation of a-MOs induced by deep-ultraviolet (DUV) light was utilized by Kim *et al.*[13] as a method to convert precursor solutions to In_2O_3, IZO, and IGZO semiconductor films at low temperatures (~150 °C). As a result, IGZO TFTs on Si/SiO_2 reached a mobility of 2.6 $cm^2/(V{\cdot}s)$ after an annealing time of 90–120 min. The UV wavelengths used in that work were those of a low pressure Hg lamp at 185 nm (10%) and 254 nm (90%).[13] The light energy of the DUV at 648 kJ/mol ($\lambda = 185$ nm) is sufficient for breaking several carbon bonds (C-C: 347 kJ/mol, C-H: 410 kJ/mol) which can assist in removing carbon impurities from the film.[14] The improvement of TFT device characteristics has been reported to follow with DUV exposure during

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pre-annealing,[15] annealing,[5,13] and post-annealing steps.[16] In our work, we have focused on shorter UV wavelength of 160 nm using a deuterium source since it is expected that such a short wavelength can introduce enhanced UV absorption and hydroxyl radical generation through the photolysis of water[17–19] as discussed in more detail in what follows.

In a R2R processing line, the annealing times are limited by the length of the in-line curing ovens. For example, for a moderate web speed of 1 m/min and a typical oven length of 5 m, the curing time for each processed layer is limited to 5 min. However, most of the low-temperature processing methods reported in literature require annealing time typically from 0.5 h up to 4 h.[9–13] As the notable exception, ZnO-based TFTs have been processed both at a low-temperature of 140 °C and with a short process time of 3 min by using a microwave-assisted annealing method, resulting in TFTs with mobilities of 0.7 $cm^2/(V{\cdot}s)$.[20] However, the polycrystalline nature of ZnO typically induces poor device stability and large hysteresis due to abundant charge traps in the grain boundaries between the particles.[1] In this letter, by combining a short-wavelength far ultraviolet (FUV) photochemical activation and conventional thermal annealing of air-processable metal-nitrate precursors, we report high-performance IZO and In_2O_3 TFTs fabricated at low-temperature of 180–200 °C and in short time of 5–15 min. The proposed combined annealing method can be used to upscale metal-oxide TFT fabrication to high-throughput R2R environments.

Indium nitrate ($In(NO_3)_3{\cdot}xH_2O$, 99.9%), zinc nitrate ($Zn(NO_3)_2{\cdot}6H_2O$, >98%), and 2-methoxyethanol (2-ME, 99.8%) were purchased from Sigma-Aldrich and used without any purification. In and Zn precursor solutions were prepared by dissolving In- and Zn-nitrate salts in 2-ME for inks with 0.2 M concentration. For the IZO ink, the component solutions were mixed in 7:3 In to Zn atomic ratio. Similarly, as in Ref. 13, the inks were heavily stirred at 75 °C for 12 h prior using. A p++ doped Si wafer with thermally grown SiO_2 (100 nm) was used as the substrate providing a gate capacitance of $C_g \sim 35$ nF/cm^2. The substrates were pre-cleaned and 1 min of O_2 plasma treatment was used to improve the wetting of the ink. The ink was spin-coated at 6 krpm in air and the samples were dried in air on a hot plate at 90 °C for 15 min. The reference IZO samples were annealed in air on a hot plate at 350 °C for 30 min. The process conditions of the combined FUV and thermal annealing were varied and the annealing was performed in dry N_2 glovebox (MBraun MB 200, $H_2O \sim 1$ ppm, $O_2 \sim 20$ ppm) to avoid UV absorption in O_2 and subsequent O_3 formation. A deuterium UV source (Hamamatsu L11798) with MgF_2 window allowing a radiant peak intensity of 160 nm in the far UV region was located at 5.5 cm distance above the hot plate. The heating caused by possible IR component of the UV light was measured to be negligible with a thermocouple attached to Si/SiO_2 substrate. The optical power of the UV source was measured as ~10 mW/cm^2 with a GaP photodiode (Thorlabs FGAP71). For the source and drain electrodes, ~40 nm of Al was evaporated through a shadow mask for bottom-gate top-contact TFTs with channel width of $W \approx 1$ mm and channel length of $L \approx 40\ \mu m$ ($W/L \approx 25$). A 30 min post-annealing step was performed at 150 °C in air. The electrical characterization was performed with a Keithley 4200 semiconductor analyzer in dark in continuous mode with both back and forth sweeps recorded using a 0.01 s step time. The saturation mobility (drain voltage $V_D = 20$ V) was calculated from $\mu_{sat} = (\delta(I_D^{1/2})/\delta V_g)^2/(1/2{\cdot}C_g{\cdot}W/L)$, where I_D is the measured drain current and V_g the applied gate voltage. The thickness of the semiconductor layer <10 nm was measured with a stylus profilometer (Dektak 150, Veeco) and the surface roughness of the metal oxide film was measured with an AFM (Veeco Nanoscope 3) in 1 μm^2 scan area. The amorphous nature of the thin films was verified with x-ray diffraction analysis (XRD) (Pananalytical Xpert pro MRD, Cu K_α peak). IZO and In_2O_3 reference samples for XRD were annealed at 600 °C in air. The x-ray photoelectron spectra (XPS) were measured with a Perkin-Elmer PHI 5400 spectrometer with a monochromatized Al K_α source. A 1400–0 eV survey spectrum as well as high resolution (0.1 eV/step) spectra of C 1s, In 3d, O 1s, and Zn 2p were recorded before and after 2 min of sputtering (Perkin-Elmer PHI model 04-300 Differential Ion Gun operated at 3 kV and 25 mA emission current).

Metal nitrate-based precursors are promising candidates for printed a-MO semiconductors. They can be processed in air, convert to metal-oxygen-metal (M-O-M) network at lower temperatures than the corresponding chloride-[21] or acetate-based precursors,[22] employ a simple scalable synthesis, allow a water-based alternative synthesis route[12] and show good ink stability (in 2-ME).[23] For this work, the reference IZO TFTs fabricated from the metal nitrate solution were processed in air at 350 °C for 30 min without UV irradiation and they show a saturation mobility of $\mu_{sat} = 1.9$ $cm^2/(V{\cdot}s)$ and a low hysteresis of $V_{hyst} = 0.7$ V in the transfer curve, as shown in Fig. 1(a). The increase in the gate leakage with positive V_g, which is due to non-patterned semiconductor with global gate, can be avoided by patterning the semiconductor layer by printing or etching. In order to lower the annealing temperature, TFTs were processed with the combined thermal and FUV annealing. Consequently, TFTs annealed at 250 °C for 30 min with FUV as shown in Fig. 1(b) exhibit a high mobility of $\mu_{sat} = 3.5$ $cm^2/(V{\cdot}s)$ and a low hysteresis of $V_{hyst} = 0.6$ V, thus exceeding the performance of the thermally generated reference devices. However, we have noticed that the FUV exposure at 250 °C can possibly harm the SiO_2 dielectric layer, which leads to increased gate leakage and to saturated reverse current of Fig. 1(b). Based on the XRD measurements, the metal-nitrate-based IZO film processed with the combined annealing at 250 °C with FUV is amorphous. Also, the low average surface roughness of <0.2 nm indicates a dense homogenous film structure. At a lower temperature of 200 °C with the FUV, the TFTs exhibit a reasonable mobility of $\mu_{sat} = 1.3$ $cm^2/(V{\cdot}s)$ but also show an onset of a hysteresis loop of $V_{hyst} = 2.0$ V that is illustrated in Fig. 1(c). Lowering the temperature further to 150 °C with the FUV, the device functionality was lost as shown in Fig. 1(d). The appearance of the hysteresis loop at the lower annealing temperatures can be attributed to an incomplete precursor conversion to M-O-M network and/or to a high impurity content, both of which will result in abundant charge traps.

In order to reach processing times relevant to R2R fabrication, the shortening of the annealing time was studied. Figure 2 shows the effect of reducing the annealing time

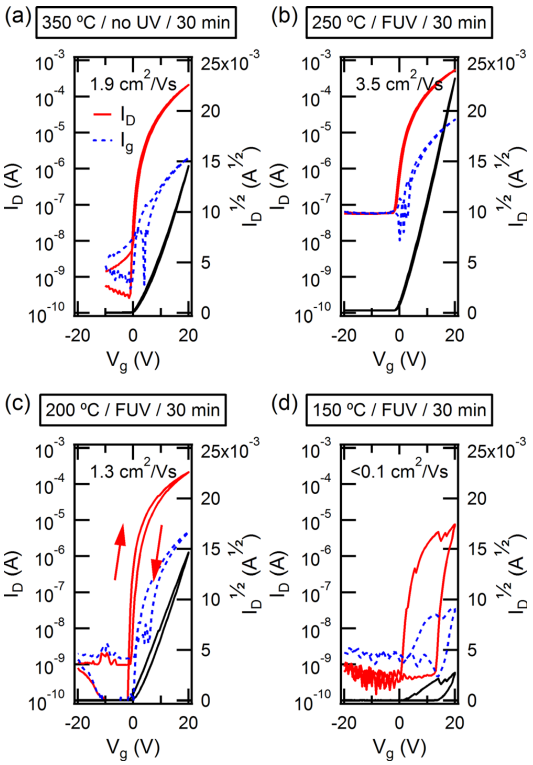

FIG. 1. Varied annealing temperature for IZO TFTs. (a) Transfer curve of a reference device annealed in air at 350 °C for 30 min. Transfer curves of devices annealed in N_2 for 30 min (b) at 250 °C with FUV, (c) at 200 °C with FUV, and (d) at 150 °C with FUV. All the curves are recorded with a double sweep and $V_D = 20$ V. The arrows in (c) denote the onset of a hysteresis loop. The blue dashed line denotes gate leakage current I_g.

from initial 30 min to 15 min and further to 5 min. The performance of the TFTs annealed at 250 °C with FUV for 15 min in Fig. 2(a) ($\mu_{sat} = 1.7\ cm^2/(V{\cdot}s)$ and $V_{hyst} = 1.0$ V) and for 5 min in Fig. 2(b) ($\mu_{sat} = 1.0\ cm^2/(V{\cdot}s)$ and $V_{hyst} = 1.2$ V) indicate a trend of lowering mobility but only slightly increasing hysteresis. Moreover, 5 min annealing

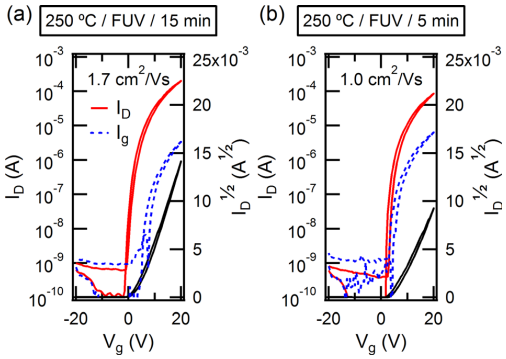

FIG. 2. Varied annealing time for IZO TFTs annealed in N_2 at 250 °C with FUV. Transfer curves of devices annealed (a) for 15 min and (b) for 5 min.

time signifies that in a R2R process the web could move at a moderate speed of 1 m/min.

The efficient and fast precursor-to-metal oxide conversion can be explained by the chemical hydrolysis and condensation processes that take place under the presence of both FUV and temperature in the nitrate-based IZO precursor film. As a contrast to the previous work performed with DUV light,[5,13,15,16] the linear extinction coefficient of water is several orders of magnitude ($>10^3$) larger at 160 nm than at 185 nm, leading to more efficient light absorption in H_2O via the FUV exposure.[17,18] The FUV light energy at 748 kJ/mol ($\lambda = 160$ nm) used in this work can induce the photolysis of water by breaking water molecules at a high quantum yield and produce atomic hydrogen (H*) and hydroxyl radicals (HO*) via a process that is nearly absent with $\lambda > 185$ nm[17,19]

$$H_2O + h\nu(\mathrm{FUV}) \rightarrow HO^* + H^*.$$

The hydroxyl radicals are reported to accelerate the condensation reaction of sol-gel metal oxide precursor films.[14] A positive feedback loop occurs as the condensation proceeds further and produces more H_2O which subsequently is broken by the FUV. The elevated temperature via the hot plate evaporates the reaction products of the fast condensation process and also the shortened non-aromatic compounds formed by the aforementioned carbon-bond cleavage.[14] The achieved minimum processing times for the combined annealing are notably lower than earlier reported in the literature for the DUV-activated photo-annealing[13] or thermal annealing.[12]

The condensation process was studied with XPS measurements for a sample dried at 90 °C and for samples annealed at different conditions. The O 1s peak deconvolution, as shown in Figure 3, was performed for resolving oxygen in metal-oxygen bonds (M-O ~ 530 eV), oxygen near oxygen vacancies (M-Ov ~ 531 eV), and oxygen bonded in metal hydroxide (M-OH ~ 532 eV). All the samples show a clear change from the only dried sample (data not shown) with dramatic increase in M-O bonded oxygen. Based on the XPS results, the sample annealed at 200 °C with FUV has the highest ratio of M-O to M-OH bonded oxygen. The sample annealed at 250 °C with FUV for 30 min (Fig. 3(a)) shows notably higher M-OH bonded oxygen than samples annealed at the same conditions for shorter time (5 min) (Fig. 3(b)), at lower temperature of 200 °C and 150 °C (Figs. 3(c) and 3(d)) or processed at 250 °C without FUV exposure (data not shown). The high M-OH content and the observed high reverse current of the TFT in Fig. 1(b) can be related and arise from the degradation of the SiO_2 dielectric or the IZO films with the 30 min exposure to high temperature and FUV, as also noted by mobility decrease for IZO films during long (>90 min) DUV exposure.[13] As the similar M-OH peaks for samples annealed at 250 °C with FUV for 5 min and at 150 °C with FUV for 30 min give clearly different TFT transfer characteristics in Figs. 2(b) and 1(d), respectively, the process enabling good TFT characteristics cannot be distinguished from the M-OH contribution alone. After sputtering, C 1s peak was not detected in any of the films, which indicate that the annealing process yielded films with

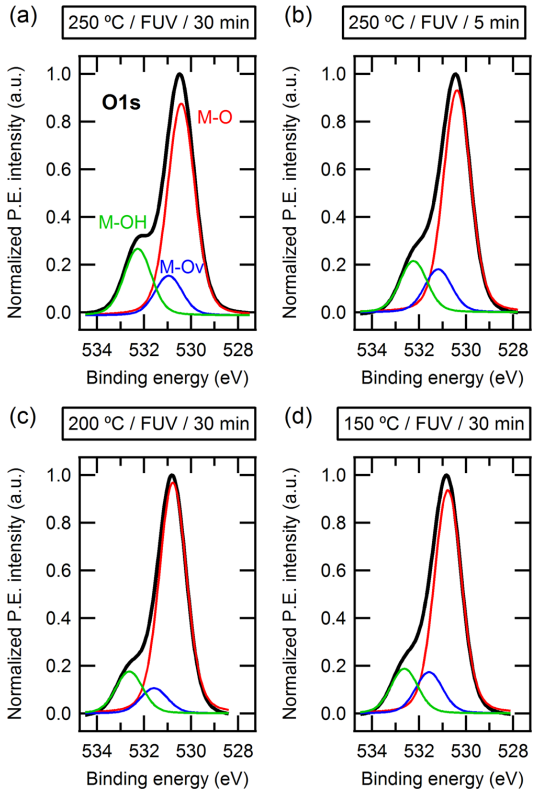

FIG. 3. Normalized x-ray photoelectron spectra of O 1 s peak of IZO samples annealed at (a) 250 °C with FUV for 30 min, (b) 250 °C with FUV for 5 min, (c) 200 °C with FUV for 30 min and (d) 150 °C with FUV for 30 min. Deconvolution of the O 1s peaks show the contributions of oxygen in M-O bonds (red) at 530.6 ± 0.2 eV, oxygen near oxygen vacancies (blue) at 531.4 ± 0.2 eV and oxygen in M-OH bonds (green) at 532.4 ± 0.2 eV.

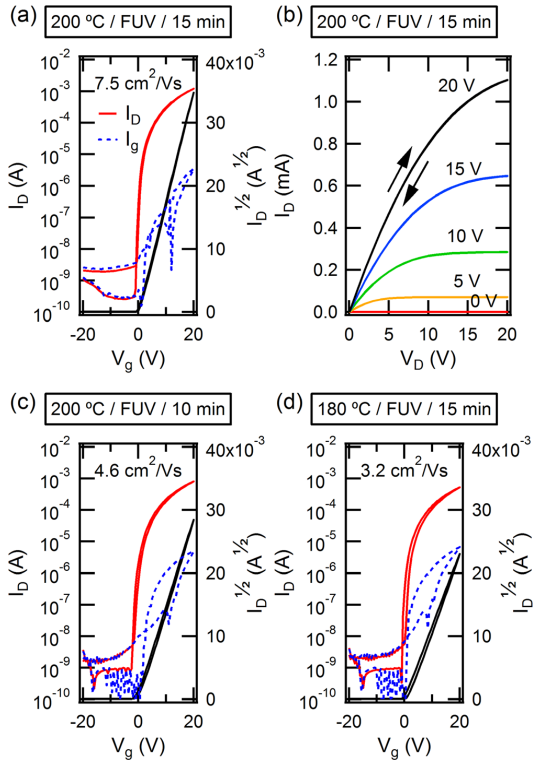

FIG. 4. Varied annealing conditions for In_2O_3 TFTs. (a) Transfer curve of a device annealed at 200 °C with FUV for 15 min. (b) Output curve of the same device in (a) with double sweep. (c) Transfer curve of a device annealed at 200 °C with FUV for 10 min. (d) Transfer curve of a device annealed at 180 °C with FUV for 15 min.

carbon impurity content beyond the XPS detection limit, regardless of the used temperature. Therefore, it is possible that temperature above 150 °C is required for the rearrangement of the M-O-M network, although the condensation process proceeds and most of the carbonic species are eliminated at lower temperature with the FUV exposure.

By utilizing a binary oxide of In_2O_3 instead of IZO, the annealing temperature could be further reduced with an additional improvement in the device mobility. Fig. 4(a) shows In_2O_3 TFTs annealed at 200 °C with the FUV for 15 min with a high mobility of $\mu_{sat} = 7.5\,cm^2/(V{\cdot}s)$ and a negligible hysteresis of $V_{hyst} = 0.4$ V. Fig. 4(b) shows the output curve for the same device with good saturation and no visible hysteresis. Reducing the annealing time to 10 min also yields TFTs with a high mobility of $\mu_{sat} = 4.6\,cm^2/(V{\cdot}s)$ and $V_{hyst} = 0.8$ V, as shown in Fig. 4(c), but a further shortening of the annealing time to 5 min reduces the mobility considerably to a level of $\mu_{sat} < 1\,cm^2/(V{\cdot}s)$. In_2O_3 TFTs annealed at 180 °C for 15 min had a mobility of $\mu_{sat} = 3.2\,cm^2/(V{\cdot}s)$ and $V_{hyst} = 1.2$ V (Fig. 4(d)). Shorting the annealing time to 10 min for the 180 °C curing temperature made the devices exhibit a large hysteresis in the gate transfer curve. The In_2O_3 reference transistors produced only by thermal annealing at 250 °C in N_2 without the FUV were non-operational, which justifies the need for simultaneous thermal and FUV annealing.

To study the uniformity of the devices fabricated with the combined annealing, a set of 16 In_2O_3 TFTs was processed at 200 °C with FUV for 15 min. The obtained saturation mobility $\mu_{sat} = 6.2 \pm 1.5\,cm^2/(V{\cdot}s)$ and hysteresis $V_{hyst} = 0.51 \pm 0.13$ V spread among the test set suggest a homogeneous structure of the metal oxide film, as supported by the low average roughness <0.2 nm of the In_2O_3 film. In_2O_3 from the aqueous nitrate-route is reported to remain amorphous at low-temperature until crystallization occurs at 250 °C[12] and our XRD measurements support this inference. XRD data of In_2O_3 film annealed at 600 °C shows a peak at $2\theta = 30.7°$ but no such peaks were observed in In_2O_3 sample prepared with the combined annealing at 200 °C and FUV.

In summary, the use of combined thermal and FUV annealing reduced the required thermal sintering temperature by more than 100 °C in IZO TFTs compared to the reference devices. The obtained low hysteresis and reasonably high mobility of IZO TFTs annealed merely for 5 min suggest that the FUV irradiation expedites the condensation process. We expect the enhancement to be caused by efficient *in situ*

hydroxyl radial formation by the 160 nm FUV light that leads into a continuous M-O-M structure in the film already within 5 min, which is notably shorter time than previously reported for longer wavelength DUV exposure.[13] For In_2O_3 TFTs, we obtained high mobilities of 3.2 $cm^2/(V{\cdot}s)$ and 7.5 $cm^2/(V{\cdot}s)$ for devices annealed for 15 min at 180 °C and 200 °C, respectively. The proposed annealing method is relevant for fabrication of high-performance a-MO semiconductor TFTs in a R2R process conditions.

All the work except the XPS analysis was performed at VTT. This project has received funding from the European Union Seventh Framework Programme (FP7/2007-2013) under Grant Agreement No. 263042. We acknowledge Dr. K. Banger from University of Cambridge for the helpful discussion on the UV-annealing and Dr. P. Kostamo from SiruTech Oy for performing the XRD measurements.

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Publication III

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Far-UV Annealed Inkjet-Printed In_2O_3 Semiconductor Layers for Thin-Film Transistors on a Flexible Polyethylene Naphthalate Substrate

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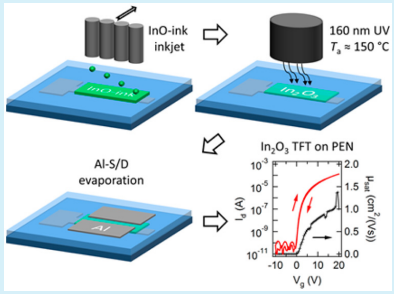
Supporting Information

ABSTRACT: The inkjet-printing process of precursor solutions containing In nitrate dissolved in 2-methoxyethanol is optimized using ethylene glycol as a cosolvent that allows the stabilization of the droplet formation, leading to a robust, repeatable printing process. The inkjet-printed precursor films are then converted to In_2O_3 semiconductors at flexible-substrate-compatible low temperatures (150−200 °C) using combined far-ultraviolet (FUV) exposure at ∼160 nm and thermal treatment. The compositional nature of the precursor-to-metal oxide conversion is studied using grazing incidence X-ray diffraction (GIXRD), X-ray reflectivity (XRR), and Fourier transform infrared (FTIR) spectroscopy that indicate that amorphous, high density (up to 5.87 g/cm^3), and low impurity In_2O_3 films can be obtained using the combined annealing technique. Prolonged annealing (180 min) at 150 °C yields enhancement-mode TFTs with saturation mobility of 4.3 cm^2/(Vs) and ∼1 cm^2/(Vs) on rigid Si/SiO_2 and flexible plastic PEN substrates, respectively. This paves the way for manufacturing relatively high-performance, printed metal-oxide TFT arrays on cheap, flexible substrate for commercial applications.



KEYWORDS: *printed transistor, thin-film transistor, metal oxide, low-temperature annealing, inkjet printing, plastic substrate*

1. INTRODUCTION

The development path from lab to market proceeded at a tremendous pace for transparent metal oxide (MO) semiconductors. In roughly ten years since the first reports of thin-film transistors (TFTs) based on sputtered ZnO[1−3] and In−Ga−Zn-O (IGZO),[4] MO semiconductors have been utilized in commercial products such as in backplane thin-film transistors (TFTs) for high-resolution active-matrix displays[5,6] and demonstrated in novel flexible applications such as flat panel X-ray sensors,[7,8] radio frequency (RF) circuits,[9] and biosensors.[10] The remarkable material properties of IGZO, such as high charge carrier mobility (>10 cm^2/(Vs)), high operational stability, and good device uniformity arising from the amorphous phase of the semiconductor, coupled with low production cost and the compatibility with industry standard processing techniques for amorphous Si (a-Si), are the key driving factors for the development.[11,12]

Solution processing of various MO semiconductors, such as binary oxides ZnO, In_2O_3, and SnO_2, ternary oxides In−Zn−O (IZO) and Zn−Sn−O (ZTO), and quaternary oxides IGZO and In−Sn−Zn−O (ITZO), can provide a viable route for the next-generation low-cost MO TFTs especially in flexible applications,[12,13] such as biosensor arrays.[10] MO TFTs have already been fabricated both with conventional printing methods such as inkjet,[14−16] gravure,[17] and flexographic[18,19] printing as well as with novel methods that allow the direct patterning of the solution-processed MO precursor layer.[20,21] Flexographic and gravure printing methods are of high interest as they can be applied in a continuous roll-to-roll (R2R) web that can lead into cost-effective mass production as already exploited in R2R-manufactured organic photovoltaics.[22] However, one of the key obstacles in using solution-processed MO semiconductors on low-cost plastic substrates arises from the precursor-to-metal-oxide conversion that typically requires a high temperature of ≥300 °C for attaining an impurity-free MO semiconductor.[13] To circumvent the problem, a wide selection of novel annealing methods have been developed that allow the metal oxide network formation at a low external temperature (<200 °C), such as ultraviolet (UV)-assisted,[23−25] ozone,[26] vacuum,[27] sol−gel-on-chip,[28] combustion,[29] and microwave[30] annealing methods. UV-assisted annealing of MO precursor films, as introduced earlier for dielectric MO films,[31,32] and, recently, also for MO semiconductor films,[23] has been shown to allow a rapid precursor-to-metal oxide conversion. Using UV-assisted annealing techniques, various dielectric MO films with high density[24] and working IZO TFT devices[25] have been obtained as swiftly as with a 5 min exposure. However, such time is still a relatively long process duration in the R2R environment, whereas in batch processing, longer curing times are more acceptable, therefore opening up the possibility to explore the effect of long annealing times.[33]

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A great body of work on printed MO semiconductors has thus far been performed with high-temperature annealing (≥300 °C) and on rigid substrates. In this paper, we demonstrate a batch process for inkjet-printed In_2O_3 TFTs on a low-cost plastic polyethylene naphthalate (PEN) substrate where the maximum processing temperature is kept at 150 °C to minimize the thermal expansion of the substrate during the processing. The inkjet-printing process of the In-nitrate-based MO precursor solution in 2-methoxyethanol (2-ME) is stabilized with a high-boiling-point cosolvent, ethylene glycol (EG). The low-temperature conversion of the precursor can be obtained at 150 °C temperature with a prolonged (3 h) exposure to low-wavelength (~160 nm) far-UV (FUV) light, regardless of the boiling point of EG at ~197 °C. This is presumed to arise from the photodecomposition of the constituents of the precursor ink, which is a nitrate anion, H_2O, 2-ME, and EG, under the FUV light. Moreover, generation of hydroxyl radicals (HO*) is expected to occur from the three first-mentioned photolysis processes (Scheme S1 in Supporting Information). HO* is a strong oxidant that further assists in the condensation process.[24,25,32] The precursor-to-metal oxide conversion is studied using X-ray reflectivity (XRR), grazing incidence X-ray diffraction (GIXRD), and Fourier transform infrared (FTIR) spectroscopy measurements. These confirm, after a prolonged 180 min FUV exposure at 150 °C temperature, the presence of high density, amorphous, and nearly impurity-free In_2O_3 films that are of similar electrical properties to the nanocrystalline In_2O_3 films obtained at the high temperature of 300 °C. The applicability of the low-temperature process is demonstrated with inkjet-printed In_2O_3 TFTs processed at maximum processing temperature of 150 °C on low-cost polyethylene napthalate (PEN) plastic substrate. Our initial results indicate that TFTs with ~1 $cm^2/(Vs)$ saturation mobility and low hysteresis operation (<1 V) can be obtained on the plastic substrate when the In_2O_3 semiconductor is printed on top of an atomic layer deposited (ALD) Al_2O_3 gate dielectric. The presented low-temperature batch process is expected to form a baseline for further TFT device optimization in terms of reduction of device-to-device variation via the control of printing strategy, curing conditions, and semiconductor doping[34] and improvements in operation stability via device encapsulation.[12]

2. EXPERIMENTAL DETAILS

2.1. Ink Preparation. In nitrate ($In(NO_3)_3{\cdot}xH_2O$, 99.99% from EpiValence, where x = 2.5)[19] was dissolved in 0.10 or 0.20 M concentration in 2-methoxyethanol (anhydrous, 99.8% Sigma-Aldrich), stirred overnight at 75 °C and filtered using a 0.45 μm pore size polytetrafluoroethylene (PTFE) filter to obtain the base solution. The mixing at the elevated temperature has been suggested to lead to the formation of solvated metal complexes with both aqueous and alkoxide ligand characters.[23,24] Ethylene glycol (EG) (anhydrous, 99.8% Sigma-Aldrich) was added to the 0.20 M base solution for inks containing 5, 10, 20, and 30 wt % of EG. The viscosity of the resulting solutions was measured using a m-VROC viscometer (Rheosense Inc.) at 10 k/s shear rate and the surface tension with EZ-Pi^{plus} (Kibron Inc.) at room temperature.

2.2. Inkjet Printing. Inkjet printing was performed at 75 μm drop spacing (339 dpi) with 10 adjacent nozzles using Dimatix Materials Printer DMP-2831 (Fujifilm, USA) with the DMCLCP-11610 cartridges of 10 pL droplet volume. A trapezoidal waveform was used for the jetting whose parameters were adjusted for each ink in order to achieve an in-flight speed of ~7 m/s and optimal jetting stability. The printing quality was inspected using an optical microscope and a software that analyzed a droplet matrix of 10 × 10 droplets and calculated the standard deviation of the center-to-center distance of the droplets both in x- and y-direction. The combined deviations in both directions were used as a quantitative metric for comparing the printing stability (see Supporting Information for details).

2.3. Thin-Film-Transistor Fabrication. The inkjet printing and far-ultraviolet (FUV) annealing processes were optimized on precut Si/SiO_2 (~100 nm oxide thickness) substrates of 13 × 13 mm in size that were cleaned using deionized water, acetone, and isopropanol in a sequential ultrasonic bath and activated before printing with a 1 min O_2 plasma treatment (200 W, Diener Nano). The In_2O_3 films were inkjet-printed as two successive layers printed without an intermediate drying step and dried at 90 °C for 15 min followed by annealing either at 300 °C for 30 min in air or using the combination of thermal annealing (varied temperature and time) on a hot plate and far-ultraviolet (FUV) exposure from a deuterium lamp with a MgF_2 window (L11798, Hamamatsu, Japan) that was situated at ~5.5 cm above the hot plate in N_2 environment (O_2 < 0.1 ppm, H_2O ~ 1 ppm). Evaporated 50 nm thick Al was used for the source and drain electrodes with channel width (W) of 1 mm and length (L) of 80 μm (W/L ~ 12.5). The completed TFT devices were postcontact-annealed in air at 150 °C for 30 min to control the turn-on voltage (V_{on}) of the devices close to V_g = 0 V.[19,35] For the devices on plastic substrates, 125 μm thick polyethylene napthalate (PEN) (Teonex Q65HA, Dupont Teijin Films) was used as the substrate with an evaporated 40 nm thick Al gate electrode and 100 nm thick Al_2O_3 gate dielectric that was grown with ALD at 150 °C using trimethylaluminum and H_2O as the precursors. An aluminum vacuum plate was used between the hot plate and the sample during the combined thermal annealing (150 °C) and FUV exposure to ensure a good thermal contact to the plastic substrate, whose top temperature was estimated using an IR thermometer.

2.4. Layer Characterization. Grazing-incidence X-ray diffraction (GIXRD) was used at a 0.5° angle of incidence (Pananalytical Xpert pro MRD, Cu K_α radiation) to determine the crystallinity of spin-coated In_2O_3 films (8 krpm) on Si/SiO_2 substrate, and X-ray reflectivity (XRR) was used for obtaining the density, roughness, and layer thickness. The samples were centered for XRR measurements using iterative adjustment of sample height z and and x–y location and performing rocking curve scans of ω and φ angles. Fourier transform infrared (FTIR) spectroscopy was used in the attenuated total reflection (ATR) mode (ThermoScientific Nicolet S50i and Harrick Scientific Products Inc. VariGATR grazing angle ATR with Ge-crystal) for obtaining the infrared spectrum of the In_2O_3 semiconductor to study the precursor-to-metal oxide conversion and the presence of impurity groups. The thickness of the printed In_2O_3 layers was estimated using atomic force microscopy (d_{AFM}) (AFM, Digital Instruments Dimension 3100/Nanoscope 3) and stylus profilometry (d_{sp}) (Veeco Dektak 150). AFM was used also to determine the average surface roughness (R_a) of the printed In_2O_3 layers over 10 μm × 10 μm scan area.

2.5. Electrical Device Characterization. The TFT properties such as saturation mobility (μ_{sat}), threshold voltage (V_t), and hysteresis in the transfer curve (V_{hyst}) were calculated from electrical data recorded using a Keithley 4200 SCS system in the dark. Both the forward and the reverse directions of the output curve and of the transfer curve at the saturation region with drain voltage of V_d = 20 V were recorded. μ_{sat} of the TFTs was calculated as a function of gate voltage (V_g) using $\mu_{sat} = [\partial(\sqrt{I_d})/\partial V_g]^2/(C_g W/2L)$, where C_g, W, and L are the areal capacitance, channel width, and channel length, respectively. V_t was calculated from the y-axis intercept of a linear fit performed to $\sqrt{I_d}$ in the range of V_g = 5−20 V. V_{on} was defined as the V_g when the I_d starts to increase during the forward sweep of the transfer curve plotted on the logarithmic current scale, thus denoting the gate voltage required to fully turn-off the TFT. V_{hyst} was estimated as the maximum voltage difference between the forward and reverse sweeps of I_d in the transfer curve. C_g and the dielectric constant ($\varepsilon \approx 9$ at 1 Hz) of the ALD-grown Al_2O_3 layer were determined from capacitance vs frequency (C–f) measurements (Alpha-A analyzer,

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Novocontrol, Germany) from Al/Al_2O_3 (~50 nm)/Al metal–insulator–metal (MIM) structures.

3. RESULTS AND DISCUSSION

The droplet formation in inkjet printing can be characterized by several parameters based on the physical properties of the printable fluids. One of the parameters, the so-called *Z*-value, is calculated as $Z = (\rho\gamma a)^{1/2}/\eta$, where ρ, γ, η, and a are the density, surface tension, and viscosity of the fluid and the characteristic length such as the nozzle diameter, respectively (see Supporting Information). *Z*-value shows a window for stable droplet formation at $1 < Z < 10$, where $Z > 10$ leads to satellite droplet formation and $Z < 1$ to poor droplet formation caused by high fluid viscosity.[36] Inkjet printing of the base solution (0 wt % of EG) resulted in poor jetting with unstable droplet trajectory and satellite droplets. However, adequate printing quality could be obtained for large areas, and inkjet-printed In_2O_3 TFTs and inverters were demonstrated earlier.[16] As a first step toward a more reliable process, the inkjet printing was optimized by using ethylene glycol (EG) as the cosolvent for the In nitrate base solution. The addition of cosolvent was expected to increase the jetting performance in several ways. First, the increased viscosity provided by the EG addition stabilized the ink meniscus at the nozzle orifice for a stable pinch off of the trailing ligament of the ink, whereas the surface tension of the ink increased only slightly with increasing EG content (Figure S1 in Supporting Information). Second, both the higher boiling point (~197 °C for EG and ~125 °C for 2-ME) and the lower vapor pressure (0.08 mmHg for EG and 6 mmHg for 2-ME) of the cosolvent decreased the evaporation rate of the ink at the nozzle and allowed sustainable jetting and ready recovery after nonjetting periods. Figure 1 shows drop watcher images for inks containing 0, 5, and 10 wt % of EG (percentage by mass of EG, w_{EG}) with a dramatically improved stability for the inks with added EG content where a stratified droplet trajectory, the elimination of a trailing ligament, and the absence of spray debris on the nozzle plate can be observed. These observations are in agreement with the aforementioned stability window in the *Z*-value as the EG addition leads to a decrease in the calculated *Z*-value from $Z > 10$ of the base solution (w_{EG} = 0%) down to the optimal range ($1 < Z < 10$) for the inks with EG added as the cosolvent (Figure 2(a)). The effect of the improved printing stability in terms of nozzle-to-nozzle consistency and straight droplet trajectory was quantitatively estimated by printing a droplet matrix on the Si/SiO_2 substrate and analyzing the results from optical microscope images using a software that calculated the standard deviations of the droplet center-to-center distances in both the *x*- and *y*-direction (see Supporting Information and Figure S2). The stability metric (σ^{-1}) value, defined as the inverse of the standard deviation of the set containing all center-to-center distances in both *x*- and *y*-direction, obtained from various ink batches indicated that, in general, the stability of the printing result increased with increasing EG content, as in Figure 2(b).

Earlier studies have shown that the addition of EG cosolvent to metal salt MO precursors in 2-ME is expected to also affect the electrical properties of the resulting MO films.[37] To find the optimum ink composition in terms of both printing stability and electrical performance, TFTs were processed using the inks with varied EG content. The results of the electrical characterization of inkjet-printed In_2O_3 TFTs subjected to high-temperature (300 °C) annealing on Si/SiO_2 substrate are shown in Figure 2(d)–(f) in terms of saturation mobility (μ_{sat}),

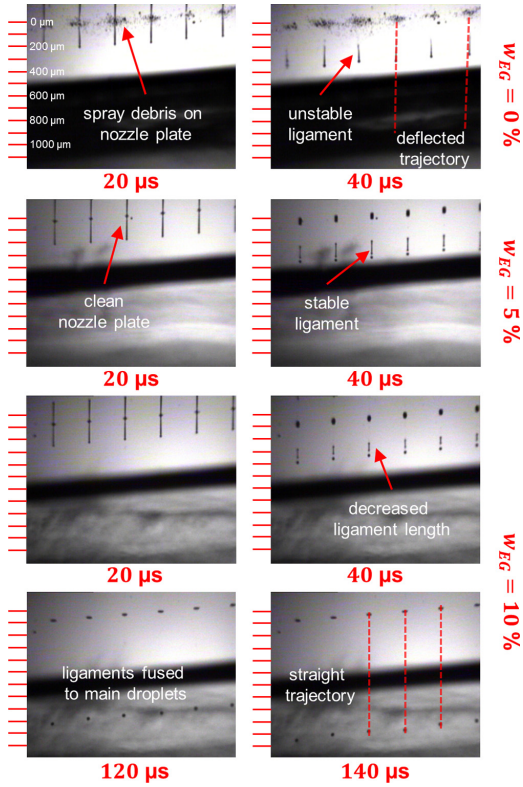

Figure 1. Drop watcher images of inks with w_{EG} = 0% (base solution), w_{EG} = 5%, and w_{EG} = 10% with varied strobe delay indicated below the still images (20 µs–140 µs). Note the trailing ligament, droplet trajectory, and debris on the nozzle plate that all indicate unstable drop characteristics for w_{EG} = 0%.

threshold voltage (V_t), and hysteresis in the transfer curve (V_{hyst}) (Table S1 in Supporting Information). When compared to the devices obtained from the base solution (w_{EG} = 0%), the device performance improves with the addition of a small amount of EG (w_{EG} = 5% or w_{EG} = 10%) and deteriorates with the addition of more cosolvent. Notably, the μ_{sat} decreases linearly for cosolvent contents higher than 5 wt % along with a linear increase in the V_{hyst}, while the V_t shows only minor changes. The improvement of the electrical properties compared to devices fabricated from the base solution can be affected by the film formation during printing and the chemical composition of the MO semiconductor films after the annealing. Based on the optical microscope images (Figure S3), the obtained films are homogeneous at the center, i.e., the TFT channel area, with narrow thicker edges which appear to widen and thin with increasing EG content based on the AFM and stylus profilometer thickness measurements, thus indicating improved ink leveling with the addition of the EG cosolvent. The lower vapor pressure of EG cosolvent could lead to a reduced outward convective flow toward the edges of the printed area that would otherwise deposit the solid material at the perimeter of the printed area and cause the formation of a "coffee ring", which is observed especially for the base

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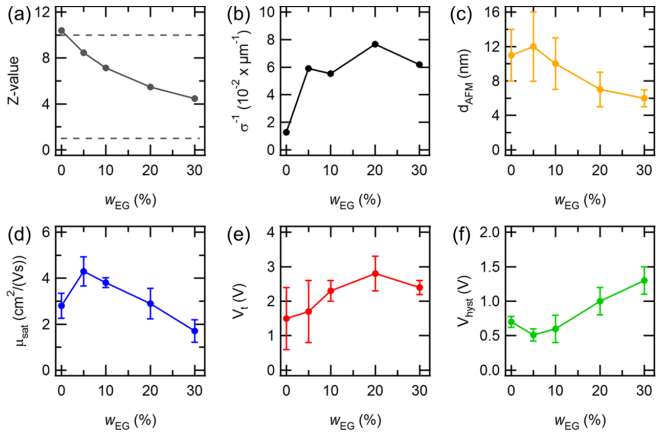

Figure 2. Stability of the inkjet printing in terms of (a) *Z*-value and (b) stability metric σ^{-1} obtained from the droplet matrix analysis (see Supporting Information and Figure S2). The gray dashed lines in (a) denote the stability window in the *Z*-value. (c) Thickness of inkjet-printed In_2O_3 double layers (d_{AFM}) measured using AFM. The electrical performance of TFTs with inkjet-printed In_2O_3 double layers on the Si/SiO_2 substrate annealed at 300 °C as (d) μ_{sat}, (e) V_t, and (f) V_{hyst}. The measurements were performed at the saturation region with V_d = 20 V.

solution.[38] The films had generally a low average roughness (R_a < 0.4 nm) which was lowered by increasing the w_{EG} (Figure S4).

During the thermal annealing of the deposited films, the precursors convert to MO films through hydrolysis and condensation reactions. For the changes in the chemical composition of the MO films after annealing, the higher dielectric constant of EG (~37) compared to that of 2-ME (~17) could (i) promote the dissociation of any remaining NO_3^- anions surrounding the In^{3+} cations that would hinder the hydrolysis and condensation reactions leading to MO films and (ii) provide an improved screening of the solvated ions.[39,40] In addition, EG added to metal-salt precursors in 2-ME solvent has been earlier proposed to act as an acidic condensation catalyst that provides H^+ which leads into MO films with less remnant hydroxide groups (M−OH) and oxygen vacancies ($M-O_{vac}$).[37] The catalyzing effect could occur by protonating the leaving groups from a hydroxo-ligand to an aquo-ligand or alkoxide groups to alcohols that are better leaving groups.[41] The M−OH and $M-O_{vac}$ of the MO semiconductor film act as charge traps and charge carrier donors, respectively, and modify the charge carrier concentration available for the transport.[37] The interplay between these could lead to the observed initial increase and the following decline in the μ_{sat}, as the V_t did not change enough to appreciably affect the overvoltage ($V_g - V_t$) of the measurements. Moreover, although the thickness measurement of printed films with thicker edge regions is of limited accuracy using AFM and stylus profilometry (nonlinear "bow" of the scanning piezo at long scans in the AFM and the selection of the linear fitting area in both methods), the data suggest that the thickness of the inkjet-printed and annealed In_2O_3 layers at the center decreased from d > 10 nm for the films obtained with low-EG content ($w_{EG} \lesssim 10\%$) to $d \sim 6$ nm for the film made from w_{EG} = 30% due to the lower molarity of the inks with the added EG content (Table S1). The lower semiconductor thickness could lead to back-channel-related effects such as enhanced charge scattering and trapping that could limit the electrical performance by decreasing μ_{sat} and increasing the V_{hyst} for the thinnest films.[42,43] The role of the decreasing semiconductor layer thickness in the deterioration of the electrical performance is supported by the lower performance of $\mu_{sat} \approx 0.3$ cm^2/(Vs) obtained for the devices printed using a 0.10 M base solution (w_{EG} = 0%) that leads to the formation of thin films ($d \sim 6$ nm) (Table S1). However, revealing the exact reason behind the trend in μ_{sat} requires further studies. As a compromise between the printing stability and the electrical performance, the ink with w_{EG} = 10% was selected for the next steps. The selected ink led to enhancement-mode In_2O_3 TFT devices on the Si/SiO_2 substrate with μ_{sat} = 3.8 ± 0.3 cm^2/(Vs), V_t = 2.3 ± 0.3 V, and V_{hyst} = 0.6 ± 0.2 V after annealing at 300 °C for 30 min.

Flexography[19] and inkjet[16] printing were earlier used to deposit films from the base solution (0 wt % of EG) on a polyimide-type (PI) opaque plastic substrate to be annealed at 300 °C for functional In_2O_3 TFTs. The substrate had a high thermal stability with the coefficient of thermal expansion (CTE) close to Si by the manufacturer specifications (~3 ppm/°C for Si) which allowed the use of the high annealing temperature. However, the annealing temperature of the In_2O_3 precursor needs to be lowered from 300 °C to be able to use low-cost, transparent plastic substrates, such as heat-stabilized polyethylene terephthalate (PET) or polyethylene naphthalate (PEN) films with maximum temperature tolerance of ~150 °C and ~180 °C and CTE of 15 and 13 ppm/°C, respectively.[44] The UV-assisted annealing can provide a viable route for reaching lower processing temperatures.[23−25] Earlier, we demonstrated that the combined FUV exposure and thermal treatment (denoted as FUV+T from hereon) can be utilized for lowering the required thermal budget and used to convert spin-coated In-nitrate-based precursors to In_2O_3 films at <200 °C external temperature for functional TFTs on Si/SiO_2.[25] By following the same principle, the FUV+T treatment was studied for the ink with w_{EG} = 10%, where the aim was to minimize the annealing temperature and limit the heat expansion during the annealing step in order to transfer the process from rigid substrates to the low-cost plastic PEN substrate that expands readily during the heating.

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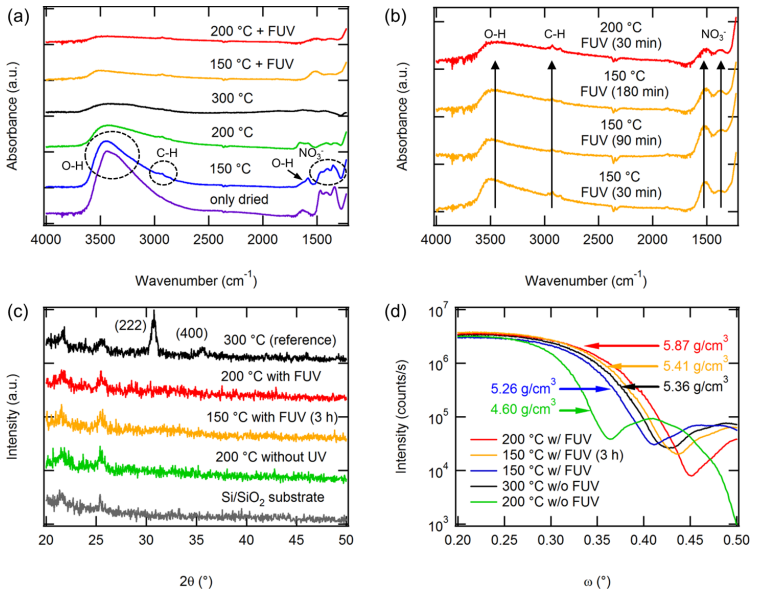

Figure 3. Characterization of the In_2O_3 precursor films annealed at varied conditions with and without concurrent far-UV (FUV) annealing. (a) Fourier transform infrared (FTIR) spectra of the films with the main bonds arising from impurity groups indicated (O−H, C−H, and related to NO_3^-). (b) FTIR spectra of the effect of increased annealing time for the FUV+T annealing. (c) Grazing incidence X-ray (GIXRD) spectra of the films. The Miller indices for cubic In_2O_3 are indicated for the reference film annealed at 300 °C. (d) X-ray reflectance (XRR) measurements of the films near the critical angle and the calculated average density from the curve fitting of the two-layer model (Table S2 in Supporting Information).

To study the conversion process, a set of precursor films were annealed for 30 min on the Si/SiO_2 substrate at various temperatures both with and without the FUV exposure, and the resulting films were measured using FTIR-spectroscopy, GIXRD-, and XRR-measurements. In Figure 3(a), the dried but nonannealed films exhibit high absorbance peaks in the FTIR spectrum that can be assigned to the presence of chemical bonds in the impurity groups with bonds related to NO_3^- (peaks at ∼1330−1470 cm^{-1}), OH groups (O−H bending ∼1620 cm^{-1} and stretching ∼3200−3600 cm^{-1}), and alkanes (C−H stretching at ∼2850−3000 cm^{-1}). By performing annealing without the FUV exposure, we see that only when the annealing is performed at high temperature of 300 °C the impurity groups are eliminated with only a minor contribution of O−H stretching remaining that can arise from adsorbed and dissociated H_2O molecules and/or remnant OH groups in the In_2O_3 film. However, when the same annealing is performed under the FUV exposure (FUV+T), the signals arising from nitrate and OH-related bonds are already clearly attenuated at 150 °C and nearly removed at 200 °C, thus indicating nearly impurity-free films. As the rate of chemical reactions can be, in general, enhanced by increasing the reaction temperature, conversely, by prolonging the annealing at 150 °C, the photochemical cleavage and the removal of the impurity groups could be improved. Figure 3(b) shows the FTIR spectrum of films annealed with FUV+T at 150 °C for 30, 90, and 180 min and, as a reference, 200 °C for 30 min. The remnant two peaks at ∼1380 cm^{-1} and ∼1510 cm^{-1} that suggest nitrate group presence, the broad O−H stretching, and the contribution from C−H stretching are only slightly diminished during the longer exposure. As the electrical performance is clearly improved by the longer annealing (see below), we studied the possible changes in the structure of the In_2O_3 films using X-ray techniques. The GIXRD spectrum, shown in Figure 3(c), reveals the films to remain amorphous in XRD except for the films annealed at 300 °C that show the peaks at ∼31° and ∼35° assigned to (222) and (400), respectively, of nanocrystalline cubic In_2O_3, in agreement with our earlier results without the EG addition.[19] From the XRR measurements (Figures S5), Kiessig fringes of two frequencies are apparent which correspond to interferences arising from the ∼100 nm thick SiO_2 dielectric (high frequency and low amplitude) and the <20 nm In_2O_3 layer (low frequency and high amplitude). However, as a model with a single In_2O_3 layer was unable to reproduce the curves, a two-layer model was utilized where the In_2O_3 layer was sectioned in two layers denoted as "top" and "bulk" (Figure S6).[45] From the following parameter fitting using the two-layer model, a slight improvement is seen in the average density (ρ_{avg}) of the films after prolonging the annealing time from 30 to 180 min at 150 °C (Table S2 in Supporting Information). The average density is calculated as $\rho_{avg} = \rho_{top}d_{top}/d_{total} + \rho_{bulk}d_{bulk}/d_{total}$, where the ρ_{top}, ρ_{bulk}, d_{top}, and d_{bulk} are the density and the thickness of the top layer and the bulk layer, respectively, and the total thickness is $d_{total} = d_{bulk} + d_{top}$. Figure 3(d) shows the XRR data near the critical angle for the selected films and the calculated average density of the films, where the ρ_{avg} increases from 5.26 g/(cm^3) to 5.41 g/(cm^3) when the annealing time is increased from 30 to 180 min for the film annealed with FUV+T at 150 °C. The highest ρ_{avg} of 5.87 g/(cm^3), which is ∼82% of the bulk In_2O_3 crystal density of 7.18 g/cm^3, is measured for the film where FUV+T annealing was performed at 200 °C. Notably, the ρ_{avg}

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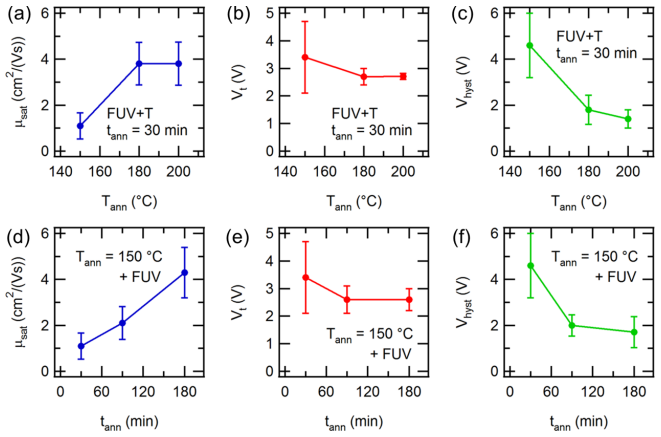

Figure 4. Electrical characteristics in terms of μ_{sat} in (a) and (d), V_t in (b) and (e), and V_{hyst} in (c) and (f) of inkjet-printed (w_{EG} = 10%) In_2O_3 TFTs (n_{TFT} = 8) on Si/SiO_2 obtained with FUV+T annealing, where (a)−(c) reflect the effect of the annealing temperature and (d)−(f) the effect of the prolonged exposure at 150 °C external temperature. The measurements were performed at the saturation region with V_d = 20 V.

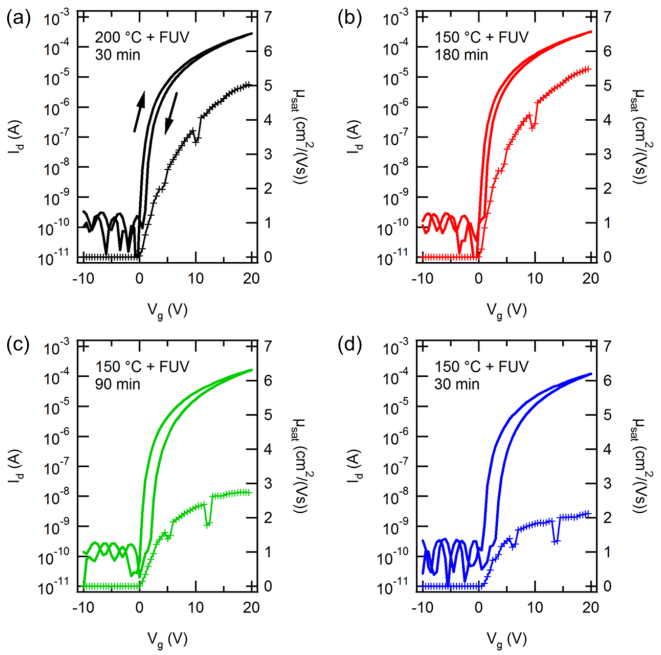

Figure 5. Transfer curves with the calculated saturation mobility of inkjet-printed In_2O_3 TFTs on Si/SiO_2 substrate obtained at different annealing conditions using the FUV+T annealing: (a) 200 °C + FUV for 30 min, (b) 150 °C + FUV for 180 min, (c) 150 °C + FUV for 90 min, and (d) 150 °C + FUV for 30 min. The measurements were performed at the saturation region with V_d = 20 V.

of the films annealed with FUV+T at 200 °C for 30 min clearly exceed the ρ_{avg} of 5.36 g/(cm^3) of the 300 °C annealed film. This lower density at the higher annealing temperature could arise from pores between the nanocrystallites observed in the GIXRD spectrum for the high-temperature annealed film. The trends in the average density are also reflected in the total thickness (d_{total}) obtained from fits to the XRR data (Table S2) of the films, where the thinnest layer is obtained for the film annealed with FUV+T at 200 °C for 30 min.

TFTs with inkjet-printed In_2O_3 semiconductor films were fabricated on Si/SiO_2 substrate, where the annealing was done using the FUV+T treatment. The results of the electrical characterization of the TFTs are collected in Figure 4 in terms of μ_{sat}, V_t, and V_{hyst}. For optimizing the transistor performance, the aim is to maximize the μ_{sat}, minimize the V_{hyst}, and

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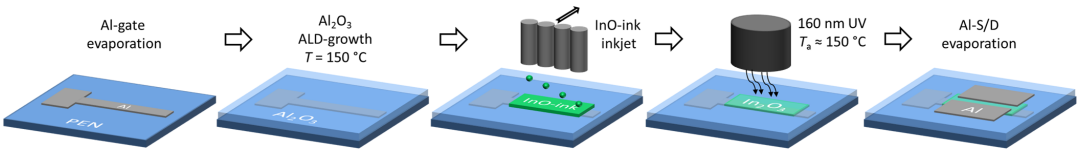
Scheme 1. Fabrication Steps for Inkjet-Printed In_2O_3 TFTs on the PEN Substrate



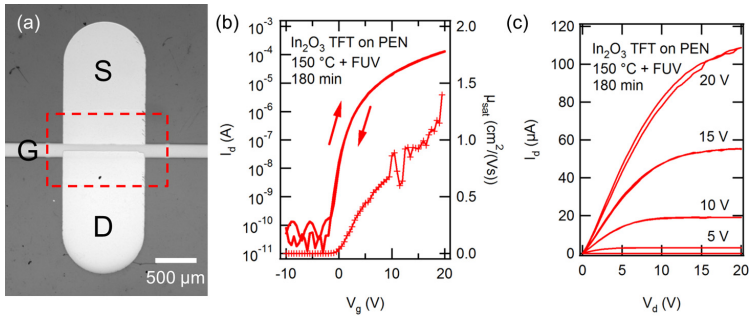


Figure 6. (a) Optical microscope image of In_2O_3 TFT on PEN substrate. The red dashed lines highlight the area of In_2O_3 (transparent). (b) Transfer curve at the saturation region (V_d = 20 V) and (c) output curve of inkjet-printed In_2O_3 TFT on PEN-substrate processed at maximum temperature of 150 °C using FUV+T annealing.

minimize the variation in the V_t. By increasing the external temperature during the FUV+T annealing from 150 to 200 °C, the μ_{sat} can be improved and the V_{hyst} reduced, while concurrently diminishing the variation in the V_t of the devices. On the other hand, by increasing the annealing duration at 150 °C, similar trends for the μ_{sat}, the V_{hyst}, and the variation in the V_t can be obtained. These results indicate the presence of fewer impurities that act as charge traps in the converted In_2O_3 films and a higher degree of MO-network formation, as reflected by the increased average density of the In_2O_3 films after the prolonged annealing step. In addition to the observed densification, changes in the distribution and fraction of amorphous and nanocrystalline inclusions, that are beyond the detection limit of the GIXRD, have been shown to affect the charge carrier transport in In_2O_3 and, thus, could also affect the electrical properties of the In_2O_3 films.[46] The transfer curves of the devices show a gate-field modulated mobility (Figure 5), and the output curves show Ohmic contact and current saturation (Figure S7). For the devices annealed with FUV+T at 150 °C for 180 min, we get μ_{sat} = 4.3 ± 1.1 cm^2/(Vs), V_t = 2.6 ± 0.4 V (enhancement mode), and V_{hyst} = 1.7 ± 0.7 V, thus a comparable electrical performance to the devices obtained at the high annealing temperature of 300 °C. The slightly higher hysteresis of the devices annealed with the FUV+T treatment can be assigned to the remnant impurity groups, as seen in Figure 3(b), which can cause some charge carrier trapping. A refined annealing process for removing of the remnant contents is under study. In addition, we expect that the process time could be shortened by using a suitable cosolvent with a lower boiling point than EG.

To finally demonstrate the general applicability of the low-temperature batch process, we followed the fabrication steps shown in Scheme 1 and fabricated In_2O_3 TFT devices on the PEN plastic substrate. Al was selected as the bottom gate material as it provides both the ductility and the adhesion required for the gate electrode to withstand the subsequent processing steps at 150 °C. To transfer the process from the rigid Si substrate to plastic substrates, also the SiO_2 gate dielectric needs to be replaced with a gate dielectric that can be processed on the plastic substrate at low temperature. Despite the recent progress both in the understanding and in the performance of solution-processed dielectric MO films,[47−50] many of the solution-processed dielectric MO films either require annealing temperature beyond that of the thermal tolerance of the low-cost plastics (>180 °C) or show the increase of the relative permittivity at low frequency that can lead to unstable, hysteretic operation characteristics and, in worst cases, to a severe overestimation of the TFT mobility.[49] Therefore, the Al_2O_3 dielectric layer was grown as the gate dielectric of the TFT devices on the PEN substrate using ALD and a robust process with trimethylaluminum (TMA) and H_2O as the precursor gases at 150 °C temperature. The dielectric properties of the Al_2O_3 films grown on PEN show a stable C−f curve down to 1 Hz frequency (Figure S8). The In-nitrate ink with w_{EG} = 10% was inkjet-printed on the O_2 plasma-treated Al_2O_3 surface and annealed with FUV+T at 150 °C for 180 min. The PEN substrate was kept in good thermal contact with the hot plate surface by a metallic vacuum plate. The TFT devices were completed with evaporated Al S/D-electrodes and postannealed at 150 °C in the oven. The TFTs on the PEN substrate, whose microscope image is shown in Figure 6(a), exhibit typically μ_{sat} ∼ 1 cm^2/(Vs), enhancement-mode operation (V_t > 0 V), a low hysteresis in the transfer curve (<1 V), as seen in Figure 6(b), and a saturating output curve as in Figure 6(c). Notably, the devices annealed for 240 or 300 min with FUV+T at 150 °C showed low gate modulation and negative turn-on voltage (V_{on} < −20 V), indicating too high charge carrier concentration for TFT operation. Further optimization of the electrical performance of the TFT devices on plastic using a refined annealing process is under study.

Although the maximum processing temperature at 150 °C is well below the maximum temperature tolerance of the PEN

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substrate, we frequently observe cracking of the Al gate electrode in some of the devices. This indicates that the main concern in the process on the plastic substrate is the thermally generated strain that causes cracks in the gate electrode metal rather than in the oxide films. The mechanical properties of sputtered MO TFTs have been reported to be improved with the selection of highly ductile gate electrode material[51] and by using a thinner substrate (<10 μm).[52] These approaches could also be exploited to prevent the cracking of the gate electrode of the inkjet-printed In_2O_3 devices on PEN.

4. CONCLUSIONS

The addition of ethylene glycol as a cosolvent in In nitrate dissolved in 2-methoxyethanol allowed establishing a stable, repeatable inkjet-printing process that could be used to fabricate In_2O_3 semiconductor layers. A low-temperature precursor-to-metal oxide conversion of these inkjet-printed layers was achieved at 150 °C using a combined thermal treatment and far-ultraviolet exposure at ∼160 nm. The conversion process was studied in detail using FTIR and X-ray measurements which showed that the most notable improvement obtained by prolonging the low-temperature process at 150 °C was seen in the slightly increased average density of the resulting In_2O_3 films. Using 180 min processing time at 150 °C led to enhancement-mode In_2O_3 TFT devices with saturation mobility of 4.3 $cm^2/(Vs)$ and ∼1 $cm^2/(Vs)$ on Si/SiO_2 and PEN plastic substrates, respectively. We expect the presented low-temperature batch process to provide a baseline for further TFT device performance optimization.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.6b14654.

Metrics for the stability of the inkjet-printing process, thickness of inkjet-printed In_2O_3 films and their electrical properties as TFTs with varied ethylene glycol content, XRR curves and data from fitting of two layer model for various In_2O_3 films, output curves of inkjet-printed In_2O_3 TFTs annealed using the combined FUV exposure and thermal treatment, and the dielectric properties of ALD-processed Al_2O_3 grown at 150 °C (PDF)

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Author Contributions

K.E. and J.L. developed the inkjet-printing process and fabricated the devices. J.L. planned and performed the experiments and analyzed the data. H.M. and A.A. supervised the project. All authors contributed to the writing of the manuscript.

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Notes

The authors declare no competing financial interest.

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Publication IV

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In_2O_3 Thin-Film Transistors via Inkjet Printing for Depletion-Load nMOS Inverters

J. Leppäniemi, K. Eiroma, H. S. Majumdar, and A. Alastalo

***Abstract*— Ability to digitally control the amount of a deposited material is one of the many advantages of inkjet printing. In this letter, we demonstrate the applicability of inkjet printing for the fabrication of depletion-load nMOS inverters based on metal oxide thin-film-transistors (TFTs) from printed metal oxide precursors where the threshold voltage of the TFTs is controlled by adjusting the thickness of the deposited semiconductor layer. Enhancement- and depletion-mode n-type In_2O_3 TFTs were fabricated from In-nitrate precursor using two printing strategies: 1) multilayer multinozzle printing and 2) single-layer single-nozzle printing in perpendicular or parallel to the TFT channel. TFTs with saturation mobility up to ∼2.4 $cm^2/(V \cdot s)$ and the ON/OFF-ratio of 10^7 were obtained after annealing at 300 °C. Devices connected as depletion-load nMOS inverters showed gain up to ∼26 on a Si/SiO_2 substrate, and an inverter on a flexible polyimide substrate with atomic layer deposited Al_2O_3 dielectric was demonstrated with a maximum gain of ∼45.**

***Index Terms*— Depletion load nMOS, inkjet printing, metal oxide, thin-film transistor.**

I. Introduction

SOLUTION processing can enable the low-cost fabrication of *n*-type metal oxide (MO) semiconductor films such as ZnO, In_2O_3, InZnO (IZO), and InGaZnO (IGZO) and such films have been utilized in high-performance thin film transistors (TFTs) [1], [2]. In addition to the commonly used spin- and spray-coating methods, the precursor solutions for the MO films can be deposited using various printing methods such as inkjet, gravure and flexographic printing, which allow direct patterning and help to avoid etching processes [3], [4]. Several precursor routes for the MO semiconductor films have been reported based on metal alkoxides and metal salts such as nitrates, acetates and halides [1]. Nitrates are of special interest for printed MO layers as they can be processed in air and converted at low-temperature using several novel scalable annealing methods [1], such as UV-assisted annealing [5].

Recently, complementary circuits adopting architectures of CMOS electronics but based on all organic TFTs (OTFTs) [6] and circuits that combine *n*-type MO-based TFTs with *p*-type OTFTs [7] or carbon nanotube (CNT) [8] TFTs have been proposed using the paradigm of printable electronics. However, as the mobility of solution processed *p*-type OTFTs is typically lower than that of the *n*-type MO TFTs [2], high areal footprint is required for the *p*-type devices to conduct similar currents as the *n*-type devices in complementary logic. Furthermore, different processing conditions for MO TFTs and OTFTs can pose limitations to the fabrication and increase the number of the process steps. Therefore, unipolar circuits are still of central interest in flexible electronics. nMOS circuits can be implemented e.g. by using only enhancement-mode *n*-type MO TFTs. Such approach suffers, however, from low gain of logic inverters caused by the enhancement TFT used as the load element. Realizing both enhancement and depletion-mode TFTs and by using depletion-loads as the inverter pull-up, nMOS inverter gains could be improved owing to the concurrent large output resistances of the driver and load elements [9].

In this letter, by utilizing thickness-dependent threshold voltage of thin *n*-type MO semiconductor films [10]–[15], we show nMOS inverters with a depletion-mode TFT as pull-up load and enhancement-mode TFT as driver that exhibit high gains of ∼26 on Si/SiO_2 and ∼45 on flexible polyimide-type substrate with Al_2O_3 gate dielectric. For this novel concept, inkjet-printed In_2O_3 films of controlled thickness were realized both using multiple printed layers and directional single-nozzle printing. The latter method allowed the effective In_2O_3 thickness to be controlled using a single printed layer. The concept could be generalized to other inkjet-printed MO TFTs.

II. Experimental

The details of the In_2O_3 precursor ink preparation (0.2 M In-nitrate dissolved in 2-methoxyethanol) and characteristics are reported elsewhere [4]. The viscosity of the obtained ink (∼3 cP at 10 k/s) was lower than optimal for inkjet printing (IJP) but reasonable droplet formation was obtained without the use of additives that can lower the electrical performance of the MO semiconductor. IJP was performed with (i) PiXDRO LP50 for multilayer samples using 8-10 adjacent nozzles at 200 dpi resolution at 30 °C substrate temperature and (ii) Fujifilm Dimatix DMP-2831 using a single 10 pl nozzle with 50 μm drop spacing. Pre-cleaned Si/SiO_2 substrates (100 nm oxide) with areal gate capacitance of $C_i \approx 35 nF/cm^2$ were activated prior to IJP with 1 min O_2 plasma (200 W) which was found to improve the wetting and help to stabilize the devices during storage. For the devices on flexible polyimide-type substrate with high thermal stability, 38 μm thick Xenomax (Toyobo, Japan) was used with evaporated Al-gate and 120 nm thick Al_2O_3 gate dielectric ($\varepsilon_r \approx 8.3$) grown with atomic layer deposition (ALD). The characteristics of the Al_2O_3 layer are given

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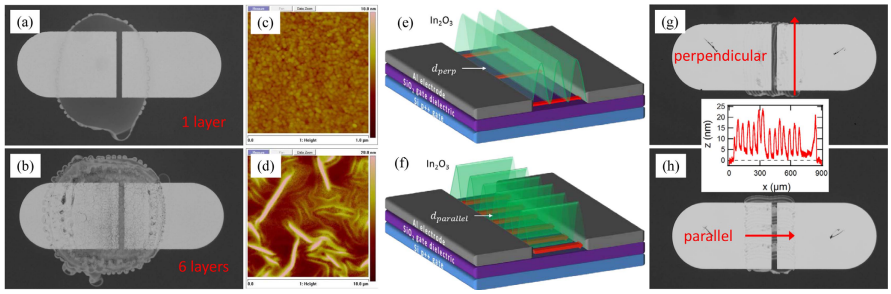

Fig. 1. Optical microscope images In_2O_3 TFTs IJP with multiple nozzles as (a) single and (b) six subsequent layers. AFM: (c) 1×1 μm scan of single layer and (d) 10 × 10 μm scan of threefold layer. Schematic image of TFT device fabricated using a single nozzle IJP (e) in perpendicular and (f) in parallel to the current flow in the channel and the corresponding optical microscope images of the devices (g) and (h). Inset: profilometer scan of area IJP with 50 μm droplet spacing.

in [4]. The drying and the thermal conversion of the precursor were performed in air at 90 °C for 15 min and at 300 °C for 30 min, respectively. The details of the annealing process are reported in [4]. Al top electrodes were evaporated through a shadow mask with 1 mm and 80 μm for channel width (W) and length (L), respectively. The devices were post-annealed at 150 °C in air for 30 min to control the turn-on voltage of the TFTs [4], [16], and stored in plastic boxes in the dark for 6 months. The thickness (d) and roughness average (R_a) of In_2O_3 were measured using stylus profilometer and atomic force microscope (AFM). Electrical characterization was performed with Keithley 4200 SCS in the dark both for fresh and stored devices. The TFT characteristics (all data here from stored devices) were calculated as in ref. [2], except for the threshold voltage (V_T) which was estimated from a linear fit to $\sqrt{I_d}$ in $V_g = 2 - 15$ V range at $V_d = 20$ V.

III. Results and Discussion

IJP of the In-nitrate precursor ink using multiple nozzles led into a uniform nanocrystalline (NC) In_2O_3 layer, as shown in Fig.1 (a) and (c). The number of layers was varied from single layer up to six layers which resulted in an increase in d and, subsequently, in variation in the operation of the TFTs. The saturation mobility (μ_{sat}) in Fig.2 (a) is heavily peaking for $d \sim 25$ nm In_2O_3 layer. The initial increase in μ_{sat} from the thinnest devices with $d \sim 13$ nm can be assigned to reduced scattering of the charge carriers at the top interface, i.e. back-channel, and to the NC nature of the In_2O_3 film which allows enhanced charge carrier percolation with thicker films. The onset of the decrease in μ_{sat} concurs with an increase in R_a, which was substantial for three or more layers as shown in Fig.2 (b). Based on AFM and optical microscope images, the rapid increase in R_a is accompanied by a shift from homogenous and transparent to opaque films, where the NC In_2O_3 bottom layer is under a porous top layer with a thread-like microstructure, as in Fig.1 (d). Such observations indicate deteriorating quality of the thicker films and the presence of pore sites that can contribute to charge trapping and scattering [17]. A slightly peaking, $d-$ dependent mobility has also been reported for sputtered [12], [14] and inkjet-printed [13] a-IGZO. The turn-on voltage (V_{on}) in Fig.2 (c)

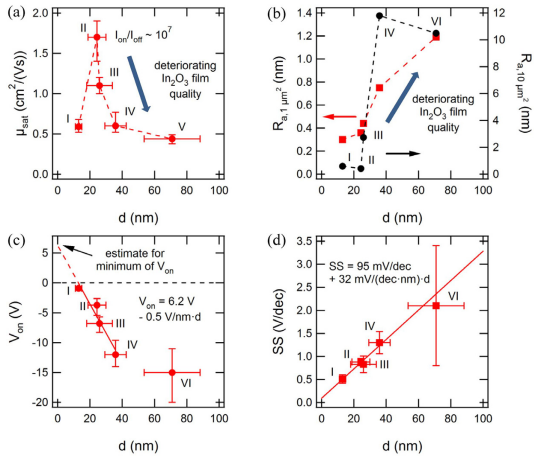

Fig. 2. Electrical characteristics and layer roughness of printed In_2O_3 TFTs ($n \geq 5$) with layer amount denoted with roman numbers. Dashed lines in (a) and (b) are for eye-guide only whereas solid lines in (c) and (d) are line-fits.

shifts linearly towards more negative values with increasing d, which can be understood as an increase in the charge carrier concentration (n_e). From a linear fit to the V_{on} data for 1-4 layers, we get, as a minimum estimate, $V_{on} \rightarrow\sim 6.2$ V for $d \rightarrow 0$. This indicates that a definitive enhancement-mode is expected only for the ultra-thin In_2O_3 devices with $d < 10$ nm, similarly as for ultra-thin sputtered amorphous IGZO (a-IGZO) [11], [12], [14]. The subthreshold swing (SS), which is related to the trap density in the bandgap [12], [14], increases linearly with d in Fig.2 (d). The trends in V_{on} and SS can arise from several possible causes. In the depletion-type devices, the total amount of bulk donor traps, such as oxygen vacancies, that contributes to the n_e is expected to increase along with d. Also, non-passivated MO TFT devices can have a depletion layer on the back-channel due to adsorbed O_2 molecules which will help to control the n_e in the thinnest devices [18], [19]. Such conditions in n_e and, hence, in V_{on}, need to be retained with a suitable encapsulation [2], [20].

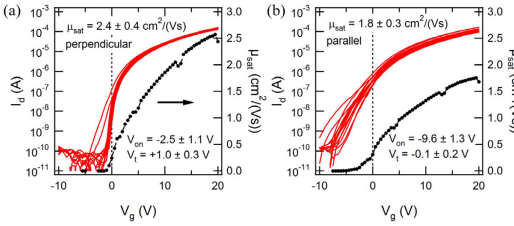

Fig. 3. Transfer characteristics of In_2O_3 TFTs ($n = 7$) inkjet printed with single nozzle in (a) perpendicular and (b) parallel to the channel on Si/SiO_2 substrate. Saturation mobility is shown for a selected device.

In addition, the operation of the NC In_2O_3 is affected by the depletion-regions at the boundaries of the NCs [4], [10].

The printed films had notable "coffee-ring" at the edges of the layer which contributed to the variation in d of the thicker films. In general, the device properties improved during the storage with the thinner devices being more stable than the thicker. The research on process optimization, such as the addition of co-solvents, annealing step between the layers and device encapsulation, is on-going. One strategy to improve the properties was directional single-nozzle IJP, as discussed next.

A single 10 pl droplet spreads on the substrate to ~100 μm diameter and shows a pronounced "coffee-ring". When printing a larger area using a single nozzle in multiple passes with a drop spacing of 50 μm, a structured area is obtained with alternating peaks of ~15 nm and valleys of ~3-5 nm in thickness with a period of ~50 μm, as shown in the inset of Fig.1. The striped line pattern forms as the ink dries, at least partly, before the next line is printed. By controlling the direction of the stripes, i.e. peaks and valleys, the effective channel thickness can be tuned as shown in Fig. 1 (e) and (f) by d_{perp} and $d_{parallel}$, where $d_{parallel} > d_{perp}$. As shown in Fig.3, a set of TFTs with In_2O_3 printed in perpendicular and in parallel to the channel show enhancement- and depletion-mode operation, respectively. The low variation among the TFTs indicates that films of similar area were obtained.

A. Depletion-Load Inverters

The transfer characteristics are shown in Fig.4 (a) for double and sixfold layer devices that operate nearly in enhancement- and in depletion-mode, respectively. When these TFTs are connected as a depletion-mode inverter, the inverter shows a sharp switching property in the voltage transfer characteristics (VTC) shown in Fig.4 (b) and a high gain of ~26 at $V_{dd} = 20$ V and gain of ~8 at $V_{dd} = 10$ V. The switching occurs at input voltage of $V_{inv} = 3.3$ V, which can be estimated from the characteristics of the constituting TFTs as follows. The I_d in saturation is given by [9]

$$I_{d,sat}\left(V_g\right) = \mu_{sat}\left(V_g\right) C_i \left(W/2L\right)\left(V_g - V_t\right)^2, \qquad (1)$$

where $\mu_{sat}\left(V_g\right)$ is gate-dependent saturation mobility. By assuming that both the driver and the load TFT have the same W and L and that they operate at saturation at $V_g = V_{inv}$ with equal I_d, we get from (1)

$$V_{inv} = V_{t,driver} - V_{t,load}\sqrt{\mu_{load}\left(V_{inv}\right)/\mu_{driver}\left(V_{inv}\right)}, \qquad (2)$$

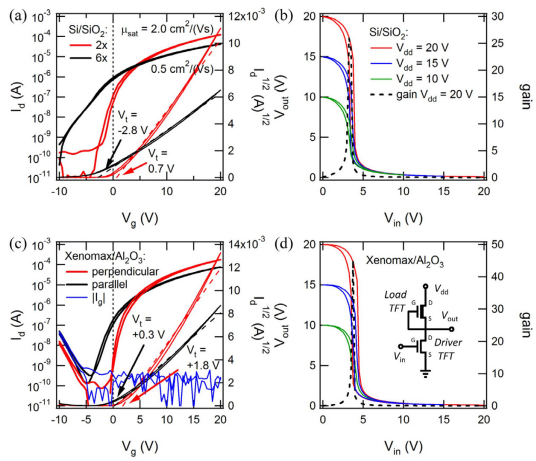

Fig. 4. (a) Transfer characteristics of In_2O_3 TFTs with 2 layers and 6 layers inkjet printed on Si/SiO_2 and (b) VTC and calculated gain for the corresponding inverter. (c) Transfer characteristics of In_2O_3 TFTs printed using single nozzle directional printing on plastic Xenomax substrate with Al_2O_3 gate dielectric and (d) VTC and calculated gain for the corresponding inverter. Inset in (d) shows the depletion-mode nMOS inverter circuit.

where $V_{t,driver}$ and $V_{t,load}$ are the threshold voltage for the driver and load TFT, respectively.

Calculation with (2) results in $V_{inv} = 2.4$ V, where the deviation from the measured value arises from the fact that V_t cannot be unambiguously determined [2]. As (2) suggests, V_{inv} could be tuned closer to $V_{dd}/2$ by the optimization of the channel dimensions or by tuning the d of the TFT devices.

We also fabricated In_2O_3 TFT devices on flexible substrate using the directional single-nozzle IJP. The transfer characteristics for a driver TFT printed perpendicular to the channel with $\mu_{sat} = 2.0$ cm^2/(Vs) and for a load TFT printed in parallel to the channel with $\mu_{sat} = 0.7$ cm^2/(Vs) are shown in Fig.4 (c) at $V_d = 20$ V. The resulting depletion-load NMOS inverter in Fig.4 (d) has a high gain of ~45 at $V_{dd} = 20$ V and gain of ~10 at $V_{dd} = 10$ V. The limitations in the V_t assessment likely cause the V_{inv} calculated with (2) ($V_{inv} = 1.6$ V) to deviate clearly from the $V_{in} = 3.7$ V of Fig. 4 (d).

IV. Conclusion

The thickness-dependent μ_{sat} and V_{on} (or V_t) of thin In_2O_3 films allows the controlled fabrication of depletion- and enhancement-mode TFTs by inkjet-printing. By connecting TFTs as depletion-load nMOS inverters, high gains up to ~45 were obtained even with un-optimized device geometry. The concept could be utilized for other inkjet-printed MOs and used e.g. in printed sensor signal amplification.

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